EECS 16B Designing Information Devices and Systems II
Spring 2016 Anant Sahai and Michel Maharbiz **Homework 7**

This homework is due March 14, 2016, at Noon.

1. **Homework process and study group**

   Who else did you work with on this homework? List names and student ID's. (In case of hw party, you can also just describe the group.) How did you work on this homework?

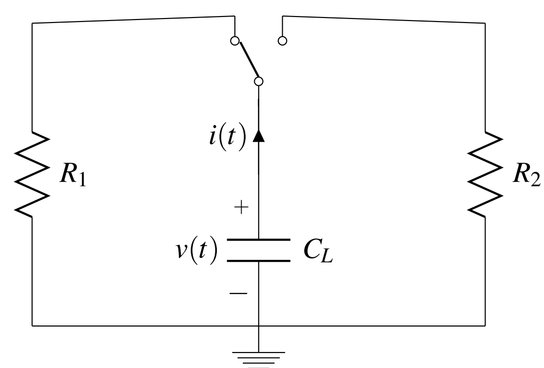
2. **Lecture Attendance**

   Did you attend live lecture this week? (the week you were working on this homework) What was your favorite part? Was anything unclear? Answer for each of the subparts below. If you only watched on YouTube, write that for partial credit.

   (a) Monday lecture
   (b) Wednesday lecture
   (c) Friday lecture

3. **An irresistible current**

   Consider the following circuit which consists of a switch which drains current between one of two resistors:



The initial voltage across the capactor initially is given as $v(t=0) = V_0$.

The switch shown in the circuit changes position every T seconds. You could consider its switching mechanism as connecting to R_1 for $k = 0,2,4,6,\ldots$ and to R_2 otherwise for any time interval in $kT < t \leq (k+1)T$ for $k \in \mathbb{N}$ where $\mathbb{N} = 0,1,2,3,\ldots$ are the natural numbers.

In other words, the switch is connected to the R_1 branch for the first T seconds, then switches to the R_2 branch for the next T seconds, then back to R_1 for the next T seconds, ad infinitum.

(a) What does the resulting waveform $v(t)$ for the voltage across the capacitor look like? Determine and sketch the resulting waveform, being sure to label all important points in the time domain.

(b) What does the resulting waveform $i(t)$ for the current draining out of the capacitor look like? Determine and sketch the resulting waveform, being sure to label all important points in the time domain.

4. Complex algebra

In this question, we will review our understanding of complex numbers.

(a) Express the current waveform

$$i(t) = -0.2\cos(6\pi \times 10^9 t + 60^\circ) \text{ mA}$$

in the standard cosine form and then determine its amplitude, frequency and phase angle and $i(t)$ at $t = 0.1$ ns. (The standard cosine form has the form of $\alpha\cos(\omega t + \theta)$, where α is positive and θ is an angle between 0 and 2π in radians or 0 and 360 in degrees.)

(b) A 4k-Hz sinusoidal voltage waveform $v(t)$, with a 12 V amplitude, was observed to descend through the value of 6 V at $t = 1$ ms. Determine the standard cosine form of $v(t)$.

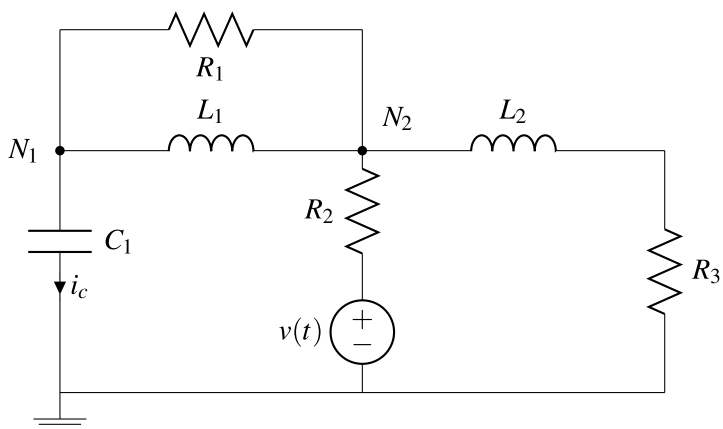
(c) Express $z_1 = (-1 + j)^{\frac{1}{2}}$ in polar form. Is the answer unambiguous?

(d) Given $z = 1.2 - j2.4$, determine e^{z^*+1} in polar form.

(e) Transform $i(t) = 18\cos(6t - 45^\circ) - 5\sin(6t)$ into the single complex number that is its phasor counterpart.

5. Phasor-Domain Circuit Analysis

The analysis techniques you learned previously for resistive circuits are equally applicable for analyzing AC circuits (circuits driven by sinusoidal inputs) in the phasor domain. In this problem, we will walk you through the steps with a concrete example. Consider the circuit below.



The components in this circuit are given by:

Voltage source:

$$v(t) = 12\cos(400t - 30^\circ)$$

Resistors:

$$R_1 = 5\Omega, \quad R_2 = 5\Omega, \quad R_3 = 5\Omega$$

Inductors:

$$L_1 = 20 \text{ mH}, \quad L_2 = 20 \text{ mH}$$

Capacitor:

$$C_1 = \frac{1}{1.6} \text{ mF}$$

(a) To begin with, transform the given circuit to the phasor domain.

(b) Write out KCL for node N_1 and N_2 in the phasor domain.

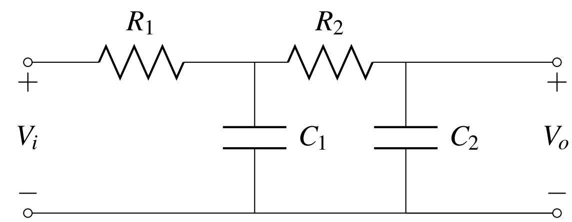
(c) Use KVL to express the currents in terms of node voltages in the phasor domain. The node voltages V_1 and V_2 are the voltage drops from N_1 and N_2 to the ground.

(d) Write the equations you derived in part (b) and (c) in a matrix form, i.e., $A \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = b$

(e) Solve the systems of linear equations you derived in part (d) with any method you prefer, and then find $i_c(t)$.

6. Transfer function

Consider the circuit below.



The circuit has an input phasor voltage V_i at frequency ω rad/sec applied at the input terminals shown in the illustration above, causing an output phasor voltage V_o at output terminals.

(a) Obtain an expression for $H = V_o/V_i$ in terms of $Z_{R1}, Z_{R2}, Z_{C1}, Z_{C2}$ (they are the impedance of R_1, R_2, C_1, C_2, respectively).

(b) Obtain an expression for $H(\omega) = V_o/V_i$ in the form of

$$H(\omega) = \frac{V_o}{V_i} = \frac{1}{1 + j2\xi(\omega/\omega_c) + (j\omega/\omega_c)^2},$$

given that $R_1 = 1\Omega$, $R_2 = 2\Omega$, $C_1 = 1F$, and $C_2 = 2F$. What are the values of ξ and ω_c?

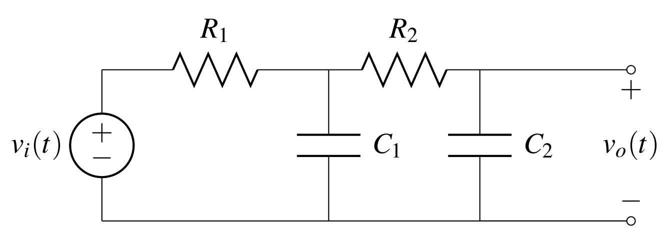
(c) We can express the transfer function $H(\omega)$ in the polar form. That is,

$$H(\omega) = M(\omega)e^{j\phi(\omega)}$$

The functions $M(\omega)$ and $\phi(\omega)$ are the magnitude and the phase angle of $H(\omega)$, respectively. Write down $M(\omega)$ and $\phi(\omega)$ using the transfer function you derived in part (b).

(d) Compute the phasors of $H(0)$, $H(\omega_c)$, and $H(\infty)$ using the results in part (b) and (c).

(e) Consider the circuit below.



The voltage source is given by

$$v_i(t) = 12\sin(\frac{1}{2}t - \frac{\pi}{4})$$

The values of R_1, R_2, C_1, and C_2 are the ones given in part (b). Obtain an expression for $v_o(t)$ in the form of $\alpha\cos(\frac{1}{2}t+\theta)$.

7. Practice with Decibels

We express a ratio of powers using decibels. If we have a reference power P_0, we express a power P in decibels as

$$P_{dB} = 10\log_{10}\left(\frac{P}{P_0}\right). \tag{1}$$

(a) Compute P_{dB} in decibels for the following cases, rounding your answer to the nearest integer.

$$P = 2P_0, \qquad P = \frac{1}{2}p_0, \qquad P = 100P_0.$$

(b) Compute P in terms of P_0 for the following cases.

$$P_{dB} = -20, \qquad P_{dB} = 6$$

(c) Let P,Q be powers, and consider the sum

$$R_{dB} = P_{dB} + Q_{dB}$$

What is R in terms of P,Q,P_0?

(d) Let $n > 0$ be an integer. Consider the sum

$$nP_{dB} = S_{dB}$$

What is S in terms of P,P_0,n?

(e) Suppose we have a circuit where a current I flows across a resistor with resistance R. The voltage across the resistor is V. Let P be the power dissipated by the resistor, and let V_0 be the voltage across the resistor corresponding to the reference power P_0. Write Formula (1) in terms of V,V_0, in the same form but with a different constant multiple of the logarithm. (*Hint: remember the power dissipated by the resistor is related to the voltage and current: $P = IV$*)

8. Op-amps for Capacitance Measurement

It is the year 2050, and you are working at a company whose product, designed for interplanetary travelers, involves a newly-invented microelectromechanical transducer. This mechanical system measures the curvature of local spacetime, which appears to the circuitry as a variable capacitance C_s. You are in charge of the team developing the preamplifier circuitry which must turn that variable capacitance into an analog voltage that can be read by a microprocessor.

You remember from physics that capacitance is defined by the relationship between charge storage and voltage: $Q = CV$. Your partner suggests that this means you can charge the capacitor to a known voltage V, then discharge it and count how much charge flows out, and use this relation to calculate the capacitance. Current is the derivative of charge, so

$$C = \frac{1}{V}\int I \, \mathrm{d}t$$

Fortunately, you remember how to integrate in an analog circuit from when you took 16B decades ago, and you can turn current into voltage using a resistor, so you and your partner design the following circuit:

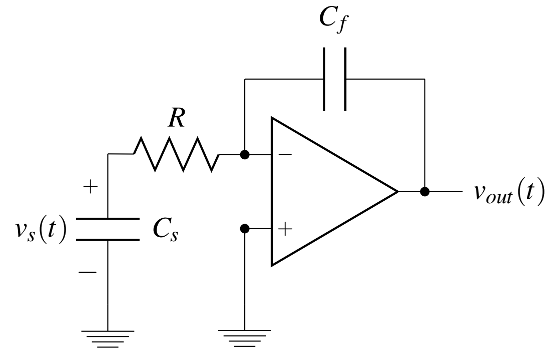


Figure 1: op-amp circuit to measure C_s

(a) What is the voltage $v_s(t > 0)$ across the transducer capacitor C_s as a function of time, if prior to $t = 0$ you charge the capacitor up so that $v_s(t \le 0) = V_{in}$?

(b) What is the current flowing through the feedback capacitor C_f?

(c) Assuming $v_{out}(t \le 0) = 0$, what is $v_{out}(t > 0)$?

So this design can get the job done, but is its performance adequate? You need not only to allow the capacitance to be calculated, but also to do so fast enough and with low enough power usage requirements to satisfy other design constraints. You don't get to choose your voltages or C_s because other physical considerations set those values, but you can choose the resistor. You are given $V_{in} = 1\,\text{V}$, and you know that on the surface of a planet with Earth's size and mass, $C_s = 1\,\text{nF}$.

(d) What resistor values R can you use if the 95% settling time of your system must be less than $1\,\mu\text{s}$? (In other words, the output must be within 5% of its final value within $1\,\mu\text{s}$ of the capacitor beginning to discharge.)

(e) The capacitive sensor has poor heat dissipation properties and may be damaged if it has to source or sink too much power. What resistor values R can you use to ensure that the power $P = IV$ supplied by the capacitor always stays below $1\,\text{mW}$?

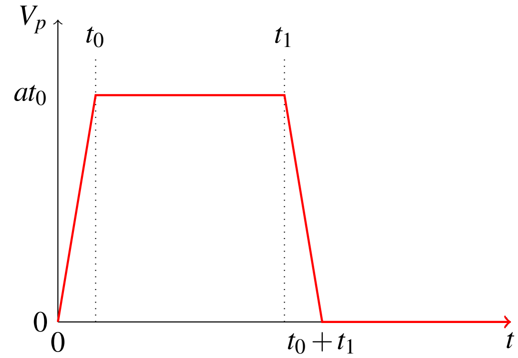
(f) Is it possible for this amplifier topology to satisfy both your power dissipation and time response specifications?

It turns out that whether or not your original design can satisfy the performance specifications, you won't be able to use it; the team in charge of voltage and current supplies tells you that there is no way to charge the capacitor to exactly V_{in} quickly enough for your circuit under their power constraints. What they *can* do is provide you with a voltage pulse $V_p(t)$ whenever the CPU requests a measurement, given by

$$V_p(t) = \begin{cases} at & 0 \le t < t_0 \\ at_0 & t_0 \le t < t_1 \\ at_0 - a(t - t_1) & t_1 \le t < t_1 + t_0 \\ 0 & t \le 0 \text{ or } t \ge t_1 + t_0 \end{cases}$$

Back at the drawing board, you realize that you can use your capacitors in a new way. You can simplify your circuit and improve its performance at once, using the following circuit:

(g) What current flows through C_s as the voltage pulse V_p is applied? (That is, what is the current I_s as a function of time?)



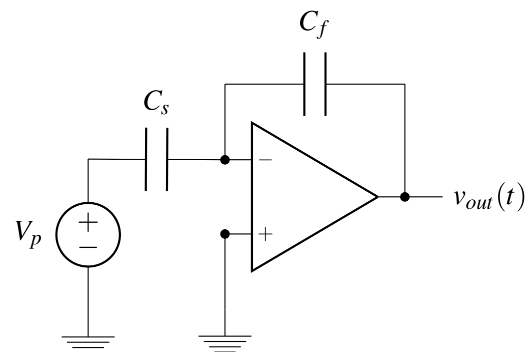


Figure 2: improved op-amp circuit to measure C_s

(h) What current flows through C_f?

(i) What is V_{out} as a function of time?

(j) When is there a stable reference voltage at the output that you can use to calculate the value of C_s?

(k) Now what is the maximal power supplied or sunk by C_s, using $t_0 = 1\,\mu s$, $t_1 = 4\,\mu s$, and an a such that the maximum value of V_p is 1 V?

(l) Can this design meet your performance specifications?

9. Your Own Problem

Write your own problem related to this week's material and solve it. You may still work in groups to brainstorm problems, but each student must submit a unique problem. What is the problem? How to formulate it? How to solve it? What is the solution?

Contributors:

- Edward Wang.
- Varun Mishra.
- Yuxun Zhou.
- Yen-Sheng Ho.
- Lynn Chua.
- Alex Spaeth.