EE16B Designing Information Devices and Systems II **Spring 2016**

Lecture Notes: 17

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1. MOSFET and Inverters

Recall last time we saw a circuit in figure 17.1. The circuit is an inverter. With the inputs A,B the output relationship was given by

$$V_{out} = \overline{AB}$$

Lets look at an another example in figure 17.2. We see that the pull down circuits have the general form seen in figure 17.3.

Remember that we can make any logic gate with just a NOR or a NAND gate. Take note at any point in time, the input of A, B be cannot be both connected to V_{out}

Analyzing the circuit in figure 17.2. we have the following output

A	B	out
0	0	1
0	1	0
1	0	0
1	1	0

This circuit is a NOR gate.

$$V_{out} = \overline{A + B}$$

Figure 17.1: NAND circuit with MOSFETS

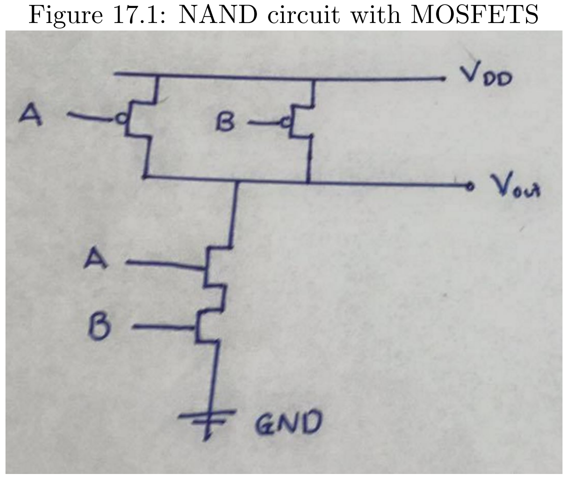


Figure 17.2: NOR circuit with MOSFETS

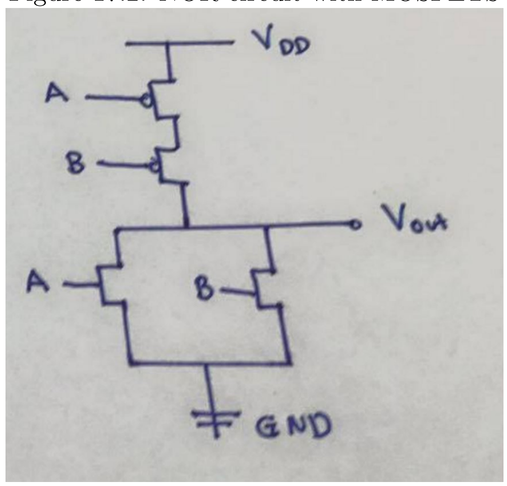
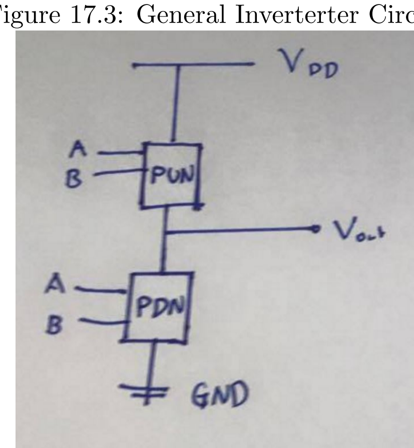


Figure 17.3: General Inverterter Circuit



The outputs here are given in boolean arithmetic. In boolean arithmetic if the airthmetic term evaluates to 0, the output is 0. If the arithmetic term is greater or equal to 1, the output is 1. Think of + as an OR[$\vee$] and $\times$ as an AND[$\wedge$].

Extra informations below are things discussed in class but are out of the scopes of this course. It will serve as a good intuition.

Extra information 1: Remember that the MOSFETS have gate pins denoted G, D, S that is often disregarded when drawing the circuit. The orientation of MOSFETS have to be directed so the the direction from S to D is towards V_{out}. This is because of the direction of the current that is allowed to flow in the MOSFETS.

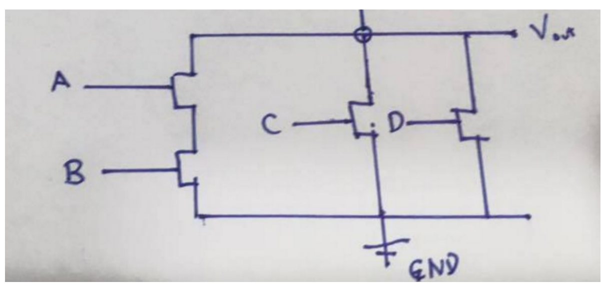
Extra information 2: In reality, there usually are capacitors everywhere between the MOSFETS except the source and the ground line. The placement of these capacitors determines the MOSFET swtich time.

Given a circuit logic, lets try to draw the circuit.

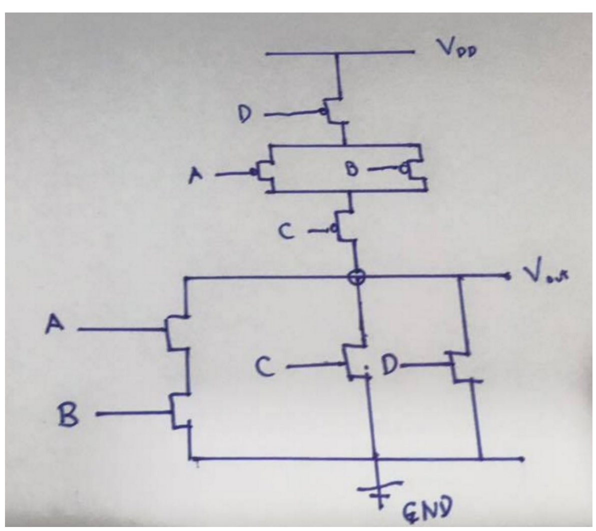
$$V_{out} = \overline{((AB + C) + D)}$$

1. First draw the circuit without the inversion

$$V_{out} = ((AB) + C) + D$$



2. Now we can add in the pull up network to invert the whole circuit

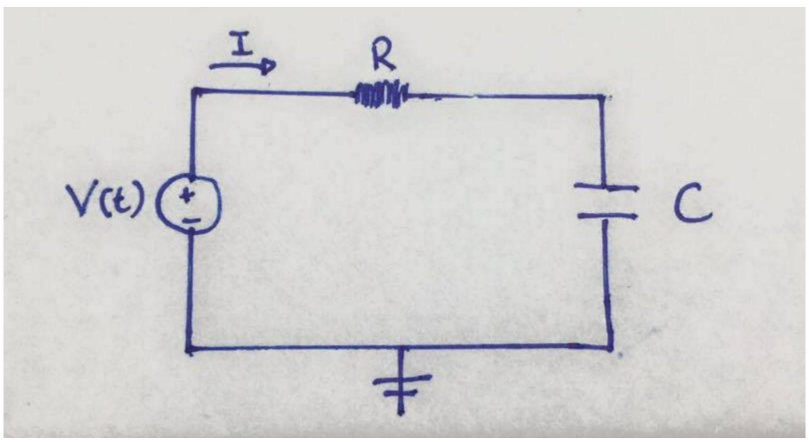


2. Introduction to Phasors

When we analyze circuits in the time domain we often have to deal with high order differential equations. Solving a high order differential equations are extremely difficult. Here we introduce a new way to solve circuit problems without having to deal with differential equations.

Remember the Fourier Transforms were useful because it allowed us to perform mathematical calculations in the frequency(complex) domain and transform it back into real signals. DFT bases were the frequency domain representation of the discretized time domain signals. Converting time domain signals to the DFT basis allowed processing and analyzing the signal to be done much easier. Similarly we want to do the same. Phasors are ways we can express the time domain AC signals into phasor(frequency) domain signals.

A signal has 3 variables. Amplitude, frequency and phase. Circuits we deal in this course are linear systems. In linear systems, the output can only be altered in magnitude and phase so in the phasor domain we are only interested in the phase and the magnitude. Lets do a quick run through of how this works. Do not worry if you do not understand the step below, we will be going more in depth in the next lecture.



Given $V_{in}(t) = 12\sin(\omega t - 45°)$ to the circuit above, lets compute the current

1. Adopt the cosine convention. Sins are just phase shifted cosines.
2. Transfer to phasor domain.

$$R \rightarrow R$$
$$V_{in}(t) \rightarrow V_s = 12e^{-j135°}$$
$$C \rightarrow \frac{1}{j\omega C}$$

3. Cast equation in phasor form. All circuit analysis methods such as node analysis still apply in the phasor form.

$$I(R + \frac{1}{j\omega C}) = V_s$$

4. Solve for the unknown.

$$I = \frac{V_s}{R + \frac{1}{j\omega C}}$$

5. Transform the solution back in to time domain.

$$Re(Ie^{j\omega t}) = 6\cos(\omega t - 105^{\circ})mA$$