EECS 16B Designing Information Devices and Systems II
Spring 2019 A. Sahai, J. Roychowdhury, K. Pister **Discussion 0A**

1 KVL/KCL Review

Kirchhoff's Circuit Laws are two important laws used for analyzing circuits. Kirchhoff's Current Law (KCL) says that the sum of all currents entering a node must equal 0. For example, in Figure 1, the sum of all currents entering node 1 is $I_1 - I_2 - I_3 = 0$. Assuming that I_1 and I_3 are known, we can easily obtain a solvable equation for V_x by applying Ohm's law: $I_1 - \frac{V_x}{R_1} - I_3 = 0$.

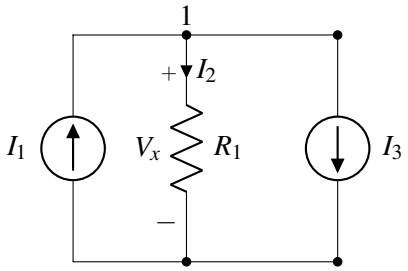

Figure 1: KCL Circuit

Kirchhoff's Voltage Law (KVL) states that the sum of all voltages in a circuit loop must equal 0. To apply KVL to the circuit shown in Figure 2, we can add up voltages in the loop in the counterclockwise direction, which yields $-V_1 + V_x + V_y = 0$. Using the relationships $V_x = i \cdot R_1$ and $i = I_1$, we can solve for all unknowns in this circuit. You can use these two laws to solve any circuit that is planar and linear.

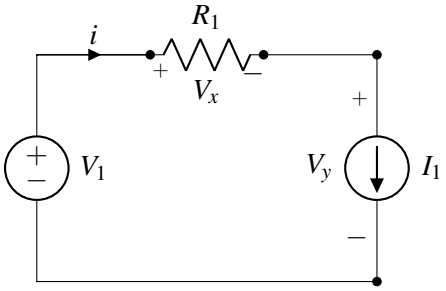

Figure 2: KVL Circuit

If you would like to review these concepts more in-depth, you can check out the EE16A spring 2018 course notes.

2 Transistor Introduction

Transistors (as presented in this course) are 3 terminal, voltage controlled switches. This means that, when a transistor is "on," it connects the Source (S) and Drain (D) terminals via a low resistance path (short circuit).

When a transistor is "off," the Source and Drain terminals are disconnected (open circuit).

Two common types of transistors are NMOS and PMOS transistors. Their states (shorted or open) are determined by the voltage difference across the Gate (G) and Source (S) terminals, compared to a "threshold voltage." Transistors are extremely useful in digital logic design since we can implement Boolean logic operators using switches.

Recall that in this class, V_{tn} denotes how much higher the gate needs to be relative to the source for the NMOS to be on, and that $|V_{tp}|$ denotes how much lower the gate needs to be relative to the source for the PMOS to be on.

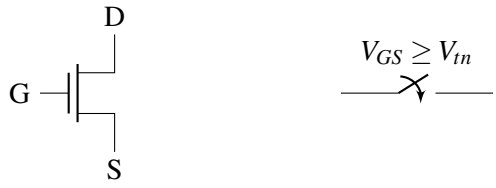

Figure 3: NMOS Transistor

Figure 4: PMOS Transistor

Transistors can be connected together to perform boolean algebra. For example, the following circuit is called an "inverter" and represents a NOT gate.

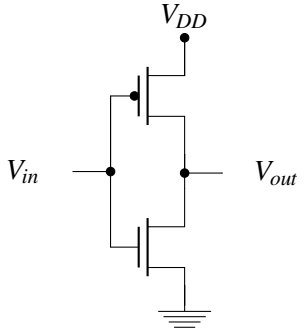

Figure 5: CMOS Inverter

When the input is high ($V_{in} \geq V_{tn}$, $V_{in} \geq V_{DD} - |V_{tp}|$), then the NMOS transistor is on, the PMOS transistor is off, and $V_{out} = 0$. When the input is low ($V_{in} \leq V_{tn}$, $V_{in} \leq V_{DD} - |V_{tp}|$), the NMOS transistor is off, the PMOS transistor is on, and $V_{out} = V_{DD}$. When working with digital circuits like the one above, we usually only consider the values of $V_{in} = 0, V_{DD}$. This yields the following truth table:

V_{in}	V_{out}	NMOS	PMOS
V_{DD}	0	on	off
0	V_{DD}	off	on

If you think of V_{DD} being a logical 1 and 0 V being a logical 0, we have just created the most elementary logical operation using transistors!

2.1 Resistor Switch Model

In the real world, transistors don't actually behave as perfect switches. Transistors have a small amount of resistance in the on state. This can be represented by a resistor in our transistor switch model.

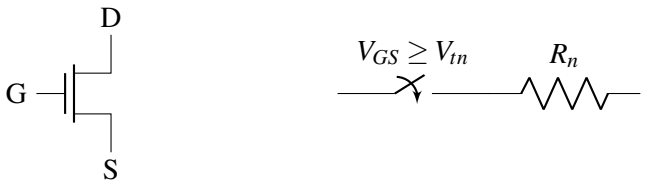

Figure 6: NMOS Transistor Resistor-switch model

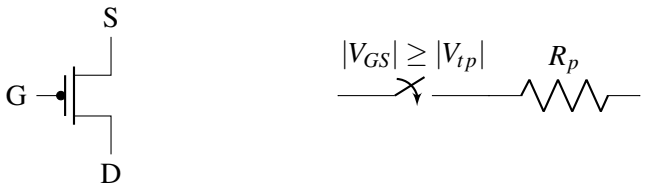

Figure 7: PMOS Transistor Resistor-switch model

1. KVL/KCL Review

Use Kirchhoff's Laws on the circuit below to find V_x in terms of V_{in}, R_1, R_2, R_3.

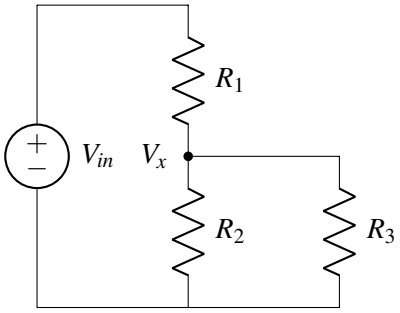

Figure 8: Example Circuit

(a) What is V_x?

(b) As $R_3 \to \infty$, what is V_x? What is the name we used for this type of circuit?

2. Transistor Introduction

Assume V_{tn} and V_{tp} are the threshold voltages for the NMOS and PMOS transistors, respectively. Also assume V_{DD} is always a positive number.

(a) In the two above NMOS transistors, label which node is the source and which is the drain.

(b) In the two above PMOS transistors, label which node is the source and which is the drain.

3. NAND Circuit

Let us consider a NAND logic gate. This circuit implements the boolean function $\overline{(A \cdot B)}$.

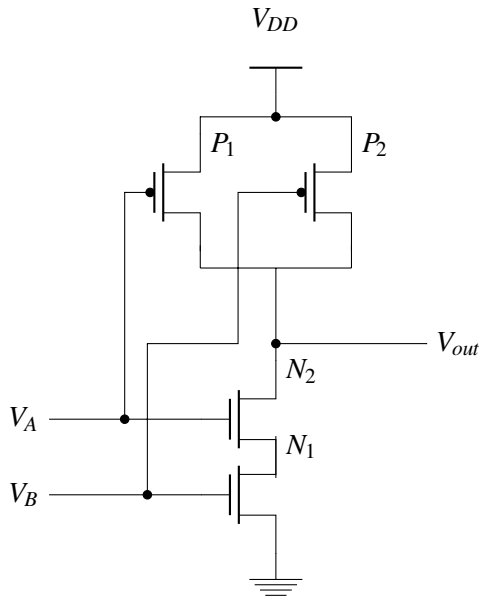

Figure 9: NAND

V_{tn} and V_{tp} are the threshold voltages for the NMOS and PMOS transistors, respectively. Assume that $V_{DD} > V_{tn}$ and $|V_{tp}| > 0$.

(a) Label the gate, source, and drain nodes for the NMOS and PMOS transistors above.

(b) If $V_A = V_{DD}$ and $V_B = V_{DD}$, which transistors act like open circuits? Which transistors act like closed circuits? What is V_{out}?

(c) If $V_A = V_{DD}$ and $V_B = 0V$, what is V_{out}?

(d) If $V_A = 0V$ and $V_B = V_{DD}$, what is V_{out}?

(e) If $V_A = 0V$ and $V_B = 0V$, what is V_{out}?

(f) Write out the truth table for this circuit.

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