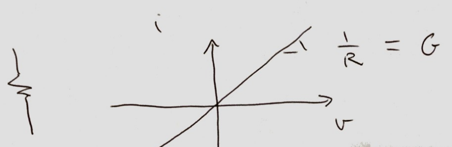
EECS16B Lecture notes jan 23 2020

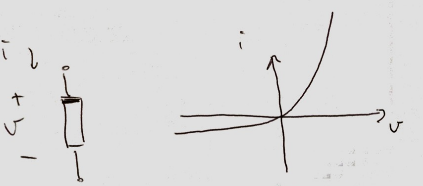
Thursday, January 23, 2020 6:55 PM

EECS 16B Jan 23 2020

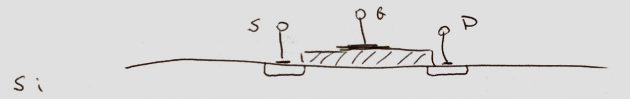
- New device Transistor



$\frac{1}{R} = G$

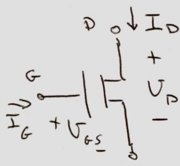


① MOSFET $\triangleq$ Metal Oxide Semiconductor Field Effect Transistor

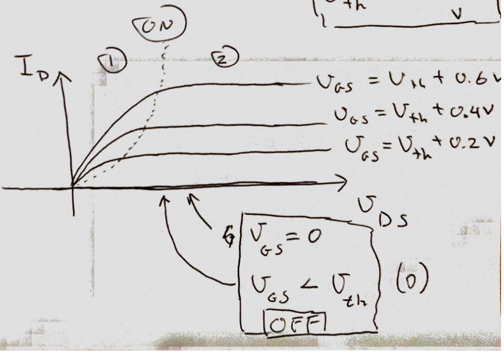


$\boxed{V_{th} = 0.2\text{–}0.3\ V}$

S = source
D = drain
G = gate


D
I_D
+
V_{DS}
−
G
I_G
$+V_{GS}$
−
S

$\boxed{I_G = 0}$



(0) OFF $V_{GS} < V_{th}$

(1) ON $V_{GS} > V_{th}$ region near origin "Linear Region"

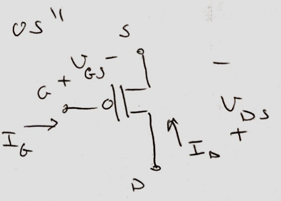
(2) ON $V_{GS} > V_{th}$ region to the right "Saturation"

- Regions (0) & (1) are good for implementing a switch
- Region (2) is good for implementing current source, amplifier, .., analog

② 1st MOSFET called "NMOS"

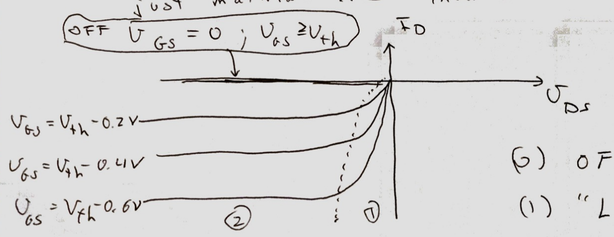
2nd MOSFET "PMOS"

$I_G = 0$


S
$+ V_{GS} -$
G
I_G
−
V_{DS}
+
I_D
D

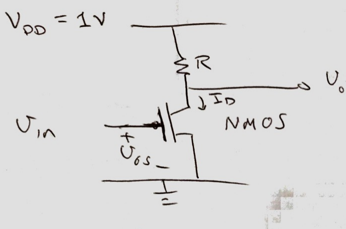
- cross-section same as NMOS, just materials are "inverted"

$V_{DS} \le 0$
$I_D \le 0$
$V_{th} = -0.2V$ to $-0.3V$



(0) OFF
(1) "Linear"
(2) Saturation

③ CMOS $\triangleq$ Complementary MOS means technology has NMOS & PMOS


$V_{DD} = 1V$
R
V_{out}
I_D
NMOS
V_{in}
$+ V_{GS} -$

$V_{in} = 0 \Rightarrow$ switch OFF
$V_{out} = V_{DD}$

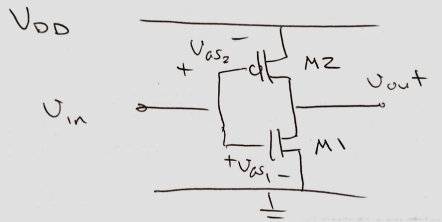
$V_{in} = V_{DD} \Rightarrow$ switch ON
$V_{out} = 0$

Example of Inverter

Input		Output	
$V_{in} = 0$	Low	$V_{out} = V_{DD}$	High
$V_{in} = V_{DD}$	High	$V_{out} = 0$	Low

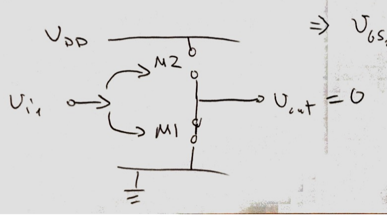
$V_{in} = V_{DD} \Leftrightarrow$ ON state
Current $I_D = \frac{V_{DD}}{R}$
Power $V_{DD} \frac{V_{DD}}{R}$

④ CMOS inverter


V_{DD}
V_{GS_2}
+
−
M2
U_{out}
U_{in}
M1
$+V_{GS_1}-$

i) $U_{in} = V_{DD}$ (high) $\Rightarrow U_{GS_1} = V_{DD} > V_{th}$ $\Rightarrow$ M1 ON

$\Rightarrow U_{GS_2} = 0$ $\Rightarrow$ M2 OFF


V_{DD}
M2
U_{in}
M1
$U_{out} = 0$

works ~~like~~ logically like prior example but all currents zero

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⑤ CMOS inverter – try $U_{in} = 0$

$U_{GS_1} = 0 \Rightarrow$ M1 OFF

$U_{GS_2} = -V_{DD} < V_{th} < 0 \Rightarrow$ M2 ON

$\Rightarrow U_{out} = V_{DD}$ [works as inverter]

$\Rightarrow$ all currents are zero! in model

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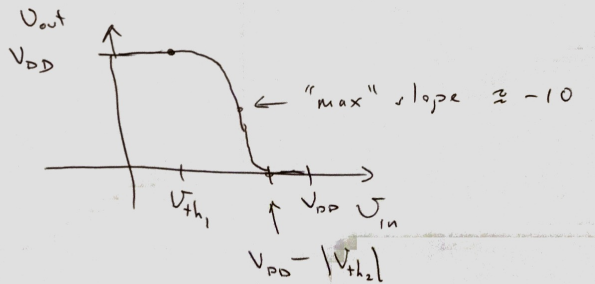
⑥ Overall input-output char.



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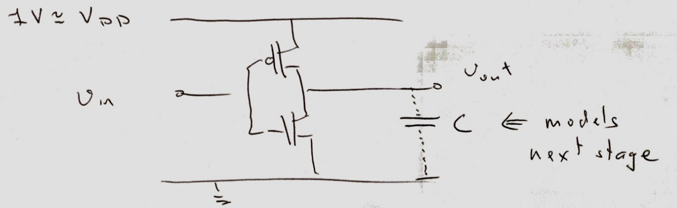
⑦ Inverter: Perfect Model $\Rightarrow$ zero current in CMOS inverter

- basic bldg block for all cells in modern computational electronics
- We know power consumption not zero!


$1V \simeq V_{DD}$
U_{in}
U_{out}
C ⇐ models next stage

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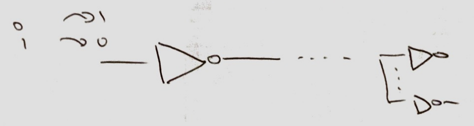
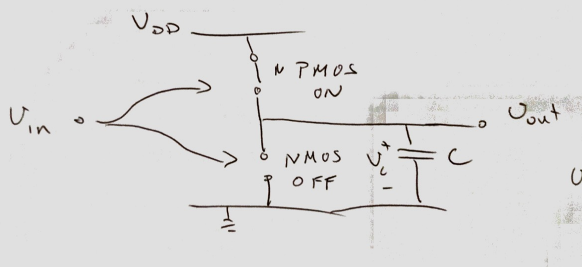
⑧




V_{DD}
PMOS ON
U_{in}
U_{out}
NMOS OFF
U_c
+
−
C

$U_c = U_{out} = V_{DD}$

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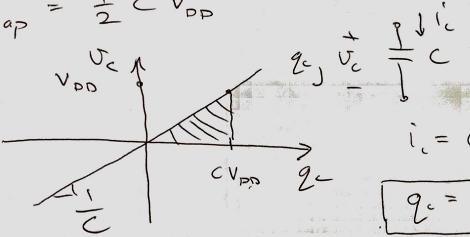
⑧

What is energy in cap if $U_c = V_{DD}$?

Cap value = C farads, likely pF; fF

$$E_{cap} = \frac{1}{2} C V_{DD}^2$$


v_c
V_{DD}
$-\frac{1}{C}$
CV_{DD}
q_c
q_c, v_c
i_c
C

$i_c = C \frac{d}{dt} v_c$

$\boxed{q_c = C v_c}$

$\boxed{\begin{array}{l} i_c = \frac{d}{dt} q_c \\ v_c = \frac{q_c}{C} \end{array}}$

- area under triangle is energy in cap

$$\int_0^{CV_{DD}} v_c \, dq = \int_0^{CV_{DD}} \frac{q_c}{C} \, dq = \frac{(CV_{DD})^2}{2C}$$

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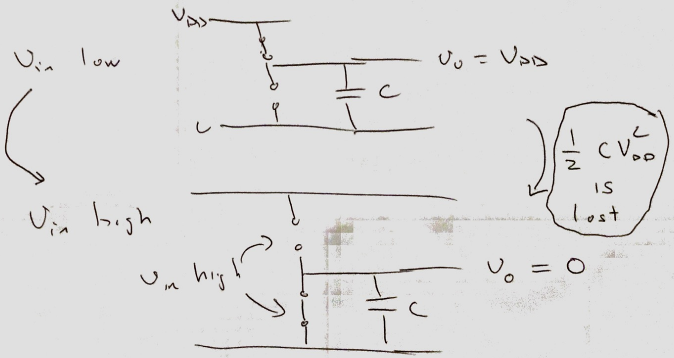
⑨ Inverter change state


V_{DD}
v_{in} low
$v_o = V_{DD}$
C
v_{in} high
$\frac{1}{2} CV_{DD}^2$ is lost
v_{in} high
$v_o = 0$
C

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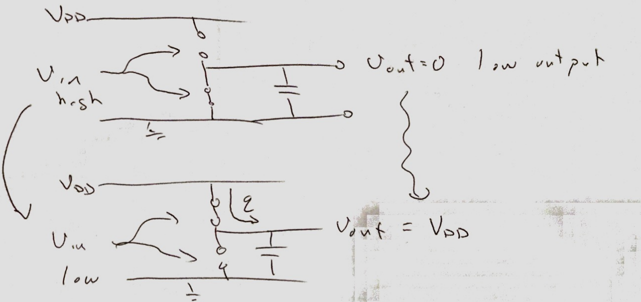
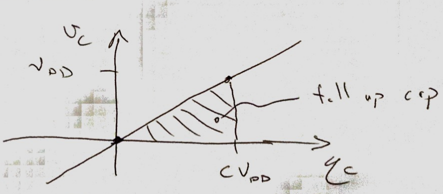
⑩ Output low to high

[Up & Down together costs CV_{DD}^2]


V_{DD}
v_{in} high
$v_{out} = 0$ low output
V_{DD}
v_{in} low
q
$v_{out} = V_{DD}$


v_c
V_{DD}
fill up cap
CV_{DD}
q_c

put $q = CV_{DD}$ onto the cap

$E_{V_{DD}} = q \cdot V_{DD} = CV_{DD}^2$

Causes of dissipations

1) $CV_{DD}^2 \cdot f_s$ f_s = frequency of clock
2) leakage : "Off" not really off
3) short-ckt current [smaller]