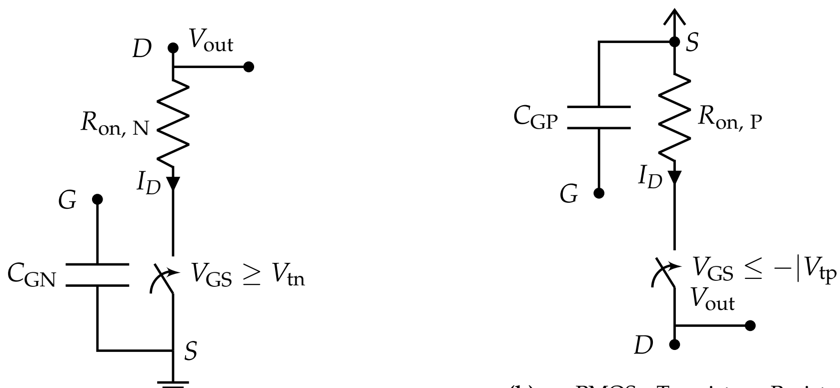
Discussion 1B

1. Transistor Switch Model

We can improve our resistor-switch model of the transistor by adding in a gate capacitance. In this model, the gate capacitances C_{GN} and C_{GP} represent the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.



(a) NMOS Transistor Resistor-switch-capacitor model

(b) PMOS Transistor Resistor-switch-capacitor model. Note we have drawn this so that it aligns with the inverter.

You have two CMOS inverters made from NMOS and PMOS devices. Both NMOS and PMOS devices have an "on resistance" of $R_{\text{on, N}} = R_{\text{on, P}} = 1\,\text{k}\Omega$, and each has a gate capacitance (input capacitance) of $C_{\text{GN}} = C_{\text{GP}} = 1$ fF (fF = femto-Farads = 1×10^{-15} F). We assume the "off resistance" (the resistance when the transistor is off) is infinite (i.e., the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V. Assume $V_{\text{DD}} > V_{\text{tn}}, |V_{\text{tp}}| > 0$. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (Figure 2).

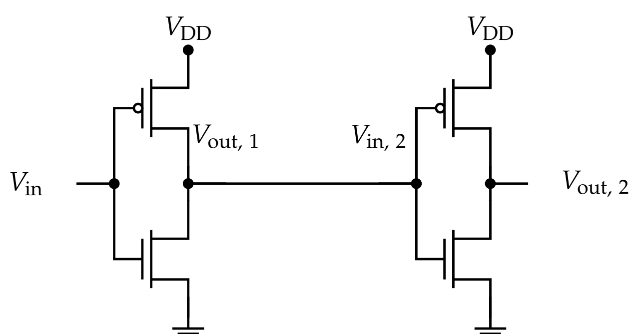


Figure 2: CMOS Inverter chain

(a) Assume the input to the first inverter has been low ($V_{\text{in}} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{\text{in}} = V_{\text{DD}}$).

Draw a simple RC circuit and write a differential equation describing the output voltage of the first inverter ($V_{\text{out, 1}}$) for time $t \geq 0$.

Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.

(HINT: Your simple RC circuit model will only have 3 elements; you only need to draw the elements that impact the behavior of $V_{\text{out, 1}}$ *and thus are relevant in this specific scenario. Also, for the first inverter, when* $V_{\text{in}} = V_{\text{DD}}$*, the NMOS transistor model's switch will be closed while the PMOS transistor model's switch will be open.)*

(b) **Solve for** $V_{\text{out, 1}}(t)$**.** The initial condition will be $V_{\text{out,1}}(0) = V_{DD}$ (this can be found by using the situation described in part (a)).

(c) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the asymptotic value, and (3) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.** *(HINT: For part (3), use the approximation that* $e^{-1} = \frac{1}{e} \approx \frac{1}{3}$*.)*

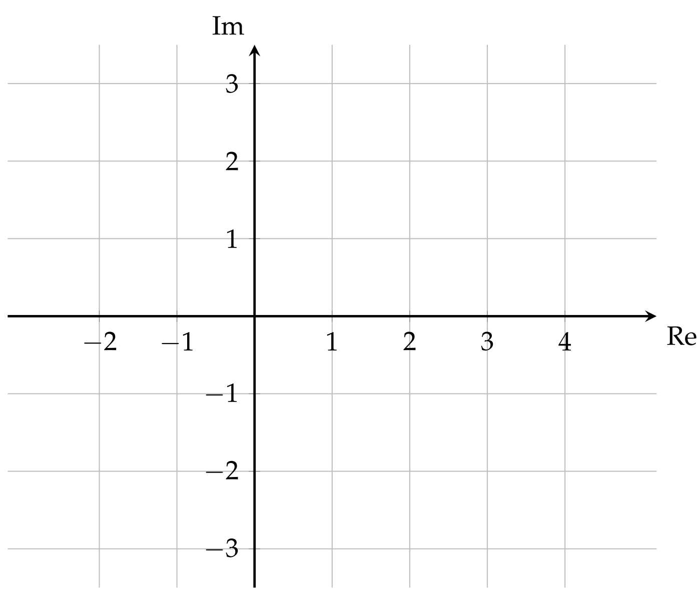
2. Complex Algebra (Review)

(a) **Express the following values in polar forms: -1, j, $-$j, $(\mathrm{j})^{\frac{1}{2}}$, and $(-\mathrm{j})^{\frac{1}{2}}$.** Recall $\mathrm{j}^2 = -1$, and the complex conjugate is defined as follows: for a complex number $z = x + \mathrm{j}y$, the complex conjugate $\overline{z} = x - \mathrm{j}y$. (Note: The complex conjugate is also sometimes notated as $z^* = x - \mathrm{j}y$, which is equivalent to $\overline{z} = x - \mathrm{j}y$.)

(b) Represent $\sin(\omega t + \theta)$ and $\cos(\omega t + \theta)$ using complex exponentials. (*Hint:* Use Euler's identity $e^{\mathrm{j}\phi} = \cos(\phi) + \mathrm{j}\sin(\phi)$.)

For the next parts, let $a = 1 - \mathrm{j}\sqrt{3}$ and $b = \sqrt{3} + \mathrm{j}$.

(c) Show the number a in complex plane, marking the distance from origin and angle with real axis.



(d) Show that multiplying a with j is equivalent to rotating the complex number by $\frac{\pi}{2}$ or 90° in the complex plane.

(e) **(Practice)** For complex number $z = x + \mathrm{j}y$ show that $|z| = \sqrt{z\overline{z}}$, where $\overline{z}$ is the complex conjugate of z.

(f) **(Practice)** Express a and b in polar form.

(g) **(Practice)** Find ab, $a\overline{b}$, $\frac{a}{b}$, $a + \overline{a}$, $a - \overline{a}$, $\overline{ab}$, $\overline{a}\overline{b}$, and $(b)^{\frac{1}{2}}$.

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