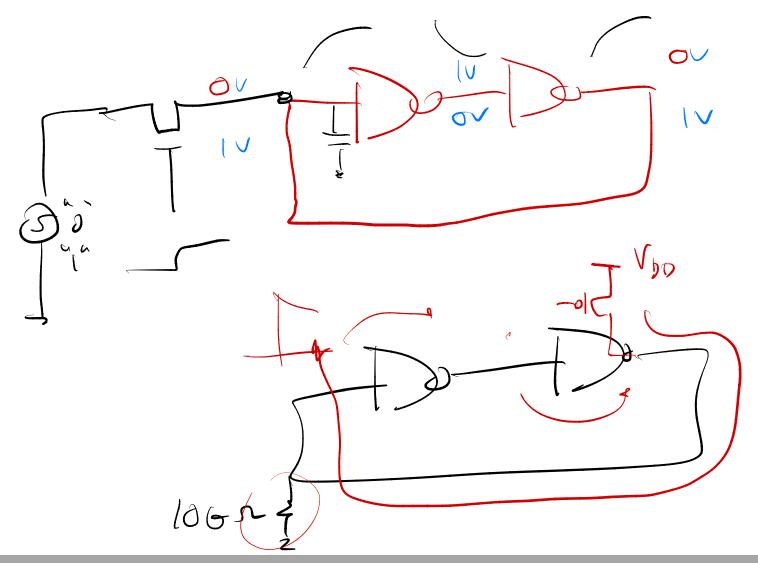
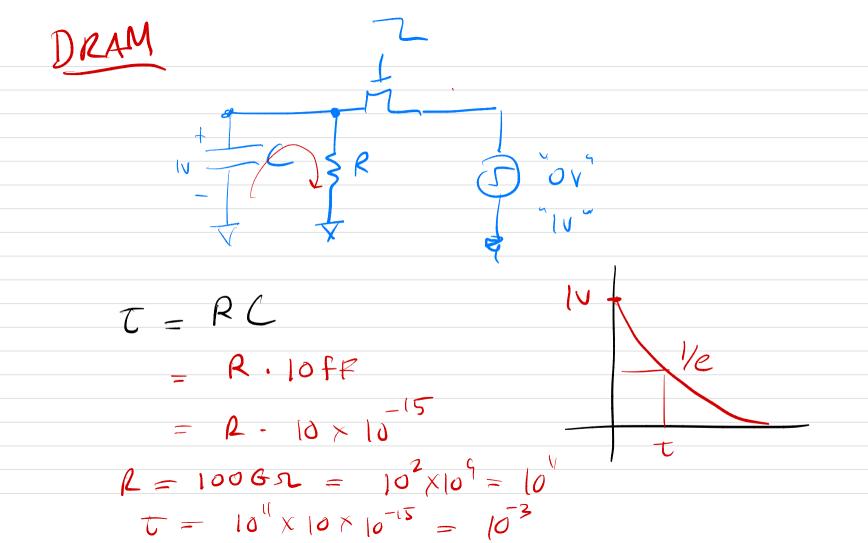
# Module 3: CMOS Models and Digital Logic Gates and Applications

EECS 16B

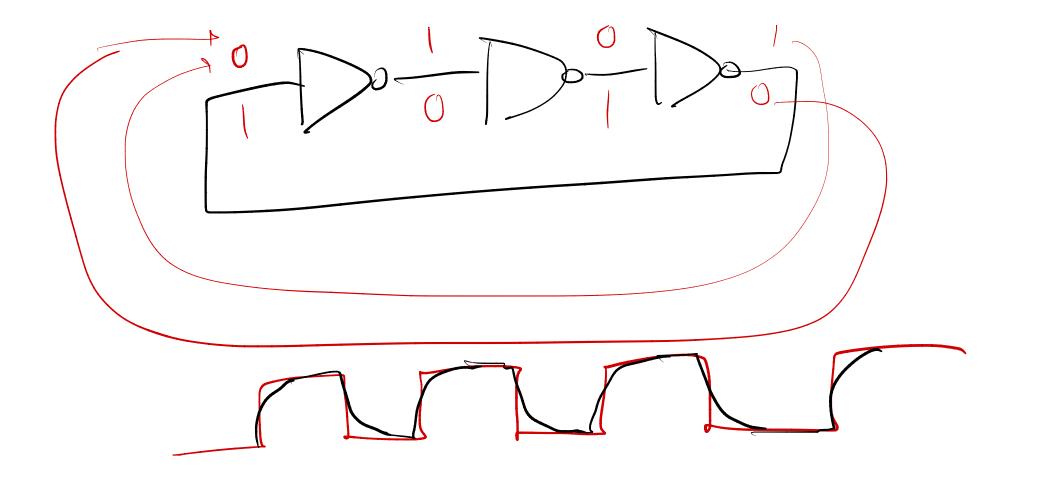
# Static RAM (SRAM)

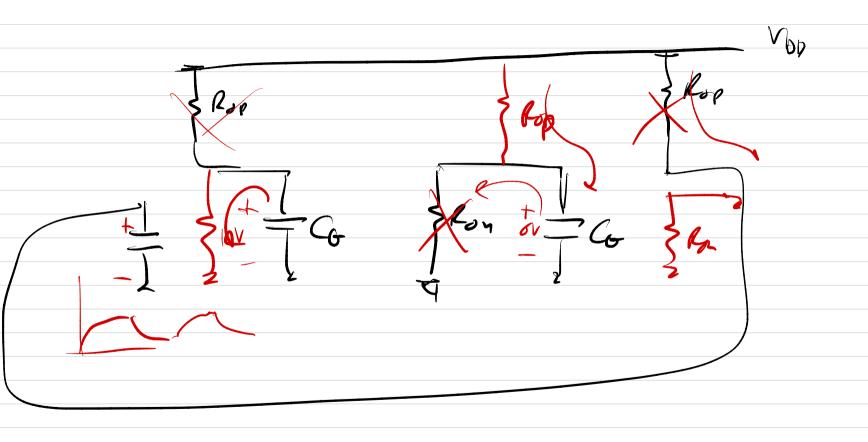


#### BISTASLE



# **Ring Oscillator**

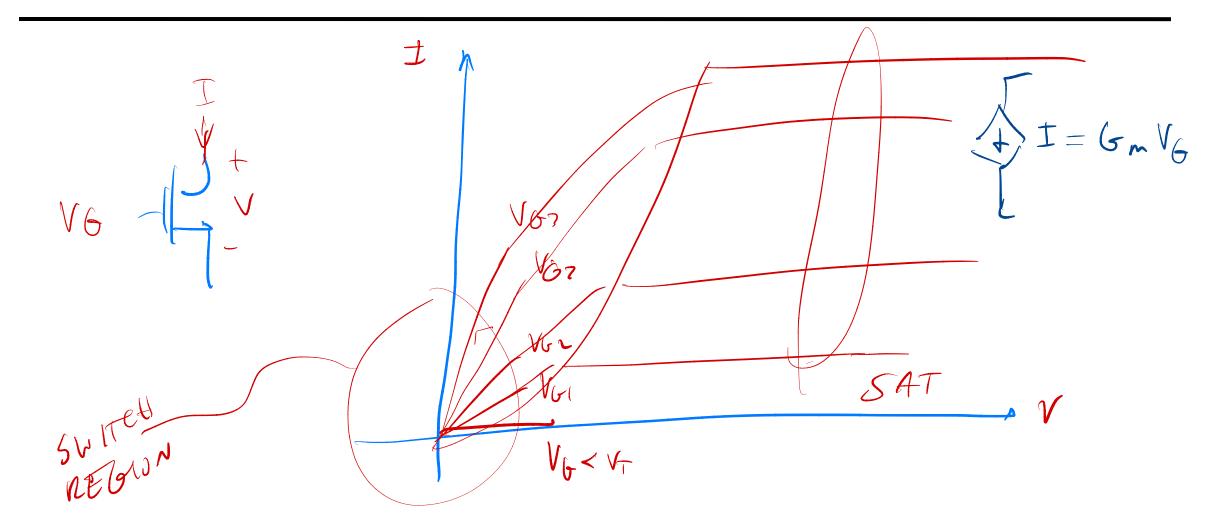




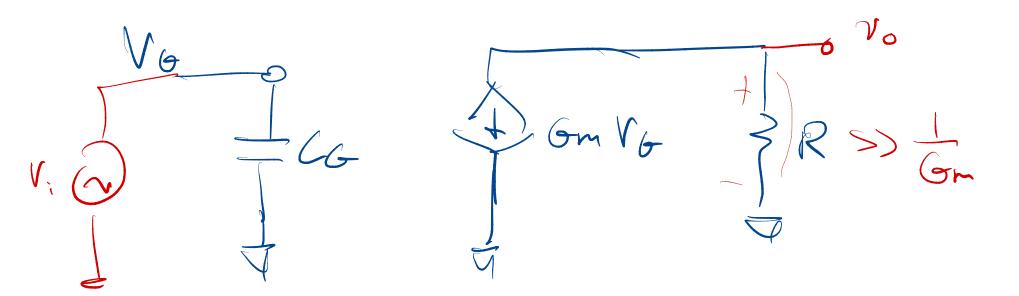
### **Differential Equations for Inverter**

HW & DISC

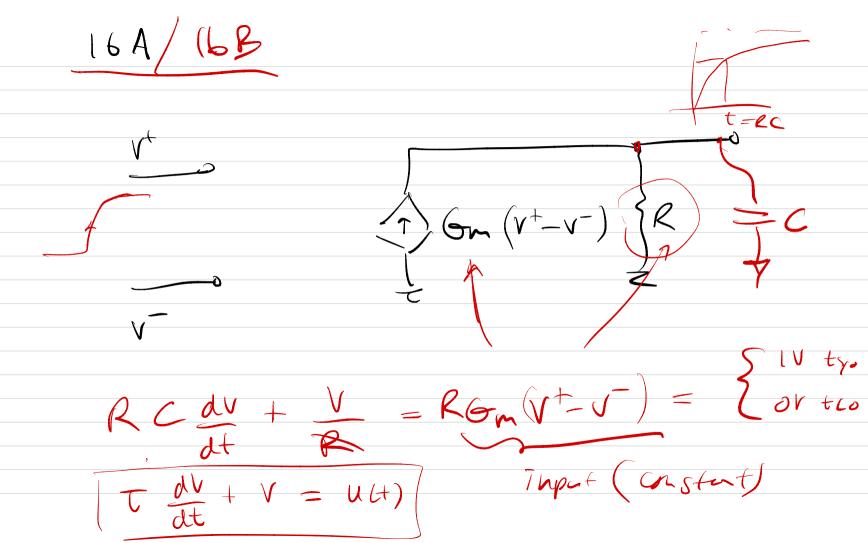
# I-V Curve Again



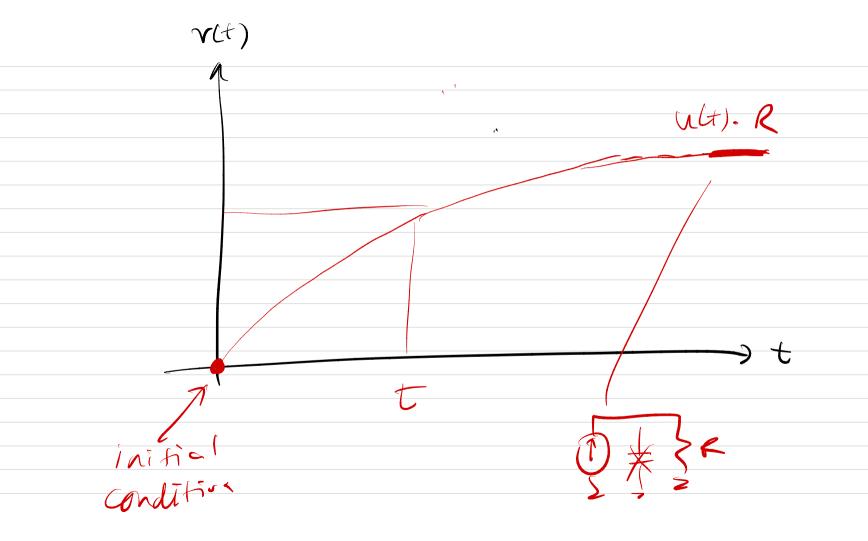
Amp Model with RC

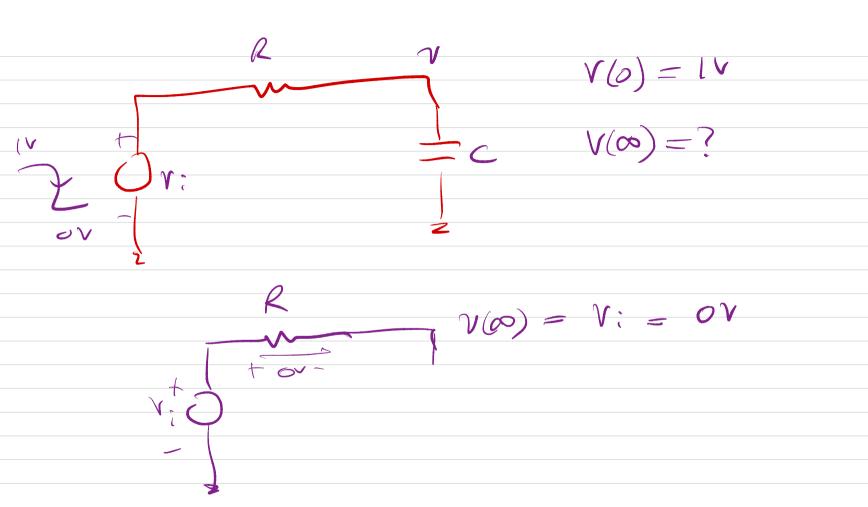


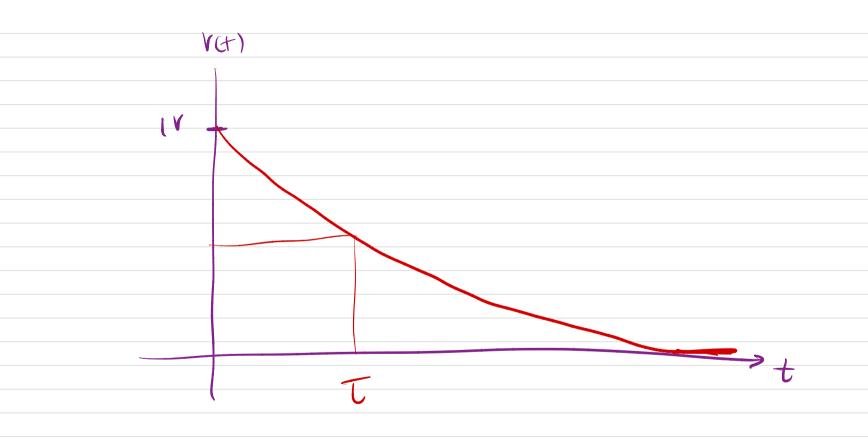
 $v_o = (-G_m V_b) \cdot R = -G_m R V_i$ Ar= - 6mR >>1



Solution 134 Inpee Y(o) = OV Capacitors R UCH ára-Solution prodict Steady -State V~ Constant UH) + $\in \mathcal{O}$ 



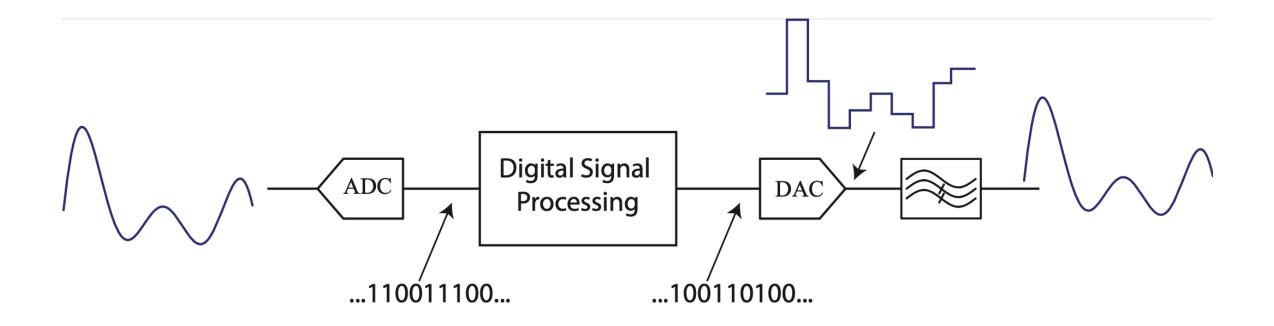




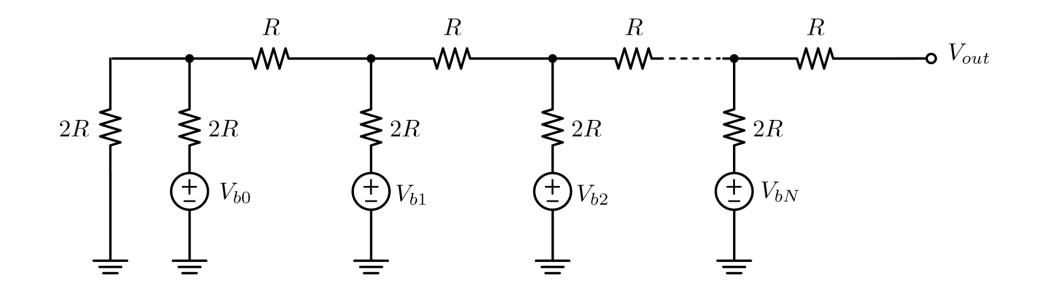
### **Amplifier Settling Time**

# **Applications**

#### **ADCs and DACs**



# **R-2R Ladder Digital-to-Analog Converter**

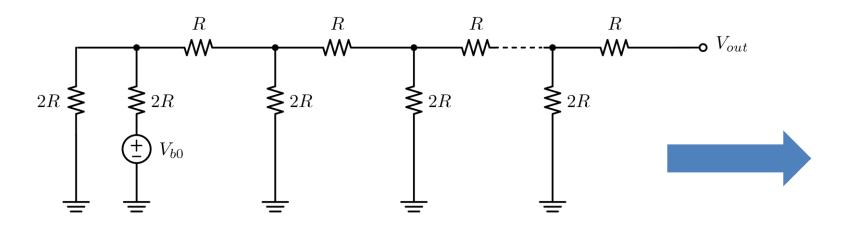


# How to set all these "digital" voltages?

### **Remember Superposition and Equivalence?**

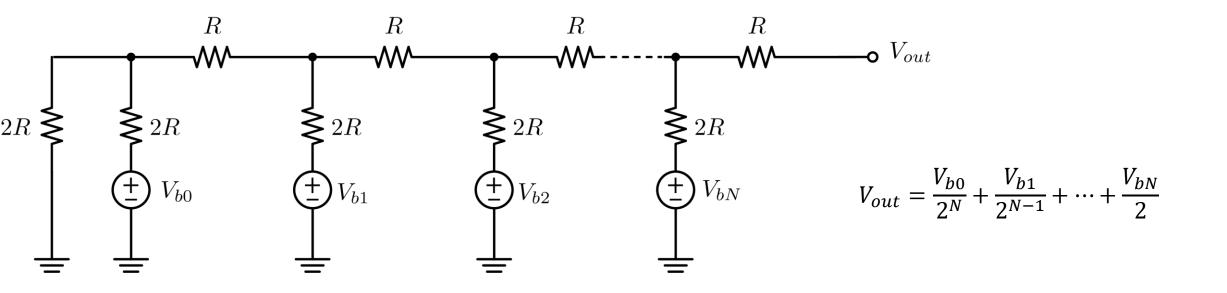
## **R-2R Ladder Digital-to-Analog Converter**

Use superposition: Start with first voltage source:

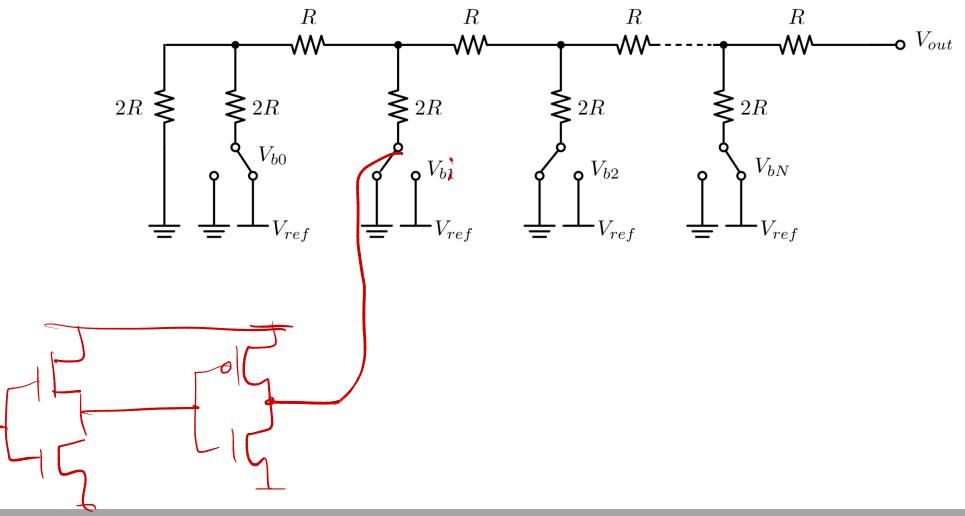


# **R-2R Ladder Digital-to-Analog Converter**

Adding all contributions from the sources



### **Switches**



EECS 16B Spring 2023

b

Lecture 1, Slide 30

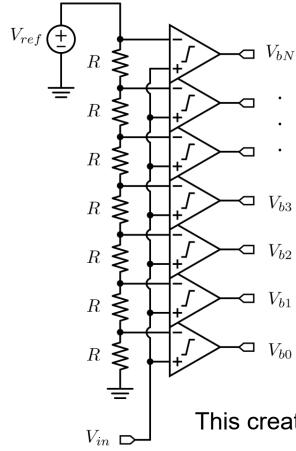
Instructors: Prof. Niknejad/Ramchandran

#### **CMOS Gates**

### How fast can we "convert"?

• If there were no capacitors, we could do it instantly !

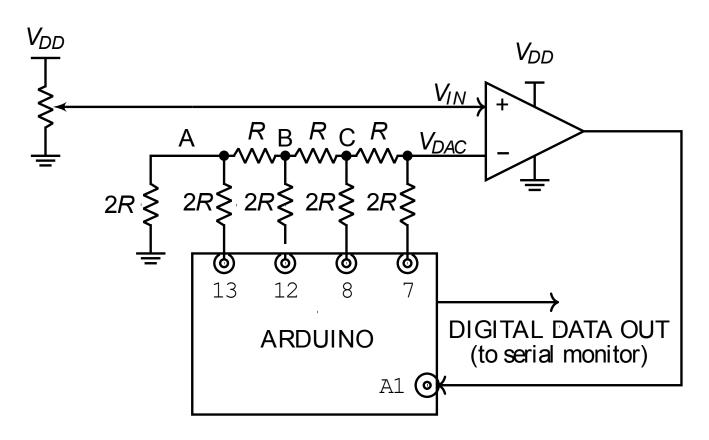
# **Analog to Digital Conversion**



- Very fast massively parallel architecture
- Requires 2^N comparators (specialized op-amps)
- Op-amps have input capacitance
- Power consumption is high for fast operation

This creates a "Thermometer" digital code. Need to convert to binary for most applications:

# Lab 2: SAR (Successive Approximation Resistor) ADC

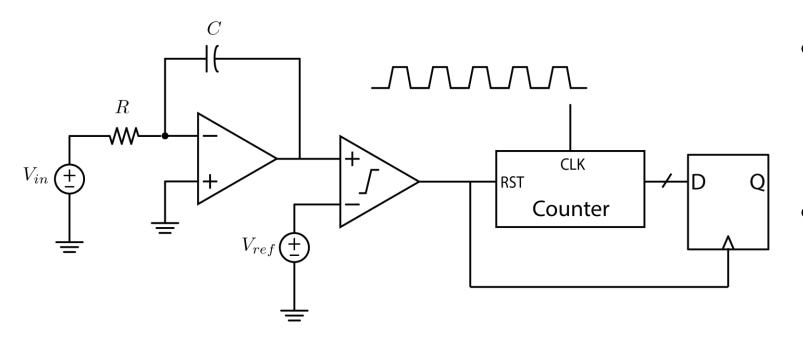


 Use a DAC to guess signal and find best digital

representation

 Can do this in log(N) steps ("guessing game")

# **RC Integrator Idea**



- RC + op-amp creates a ramp with slope proportional to input
- Count how long it takes to reach a reference value
- Counter is digital representation