Lecture 4 Key Concepts

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KC: Key Concepts.

1 Lecture 4, Module 3

1.1 Slide 4-5

KC: A MOS transistor is built from a MOS capacitor ! A MOS capacitor is like a regular parallel plate capacitor, except one metal plate is made from a semiconductor instead of a regular conductor. Think of the "gate" as a normal conductor and the transistor "body" as a semiconductor. To make a MOS-C a MOS-FET (Field Effect Transistor), we need to make contacts to the two sides of the capacitor, the "source" and "drain".

Let's start with an NMOS transistor. The "N" means that electrons conduct current. **KC:** To allow the MOSFET to conduct current, we need to apply a sufficiently positive voltage to the gate, or the voltage between the gate-source needs to exceed a *threshold voltage*:

$$V_{GS} > V_T$$

Below the threshold voltage, no current can flow from the drain to the source (remember electrons go in the opposite direction, from the "source" to the "drain"). That's because a semiconductor acts like an insulator. When we apply a sufficiently strong field to the structure, we create a "channel" or a place where electrons are free to move. In essence, we are taking electrons that are normally in bonding states in the crystal semiconductor and turning them into "free" electrons that can move about. They can only move in the vicinity of the gate where the field is strong. This is why we call it a "field-effect" transistor (forgot to mention that in lecture).

So our simplest model of a transistor is a switch. If the gate-source voltage is below V_T, the switch is open. If $V_{GS} > V_T$, the switch closes and there's an on-resistance R_{on} between the drain-source. The stronger the gate voltage, the larger conductivity between the gate/source, the smaller R_{on}.

1.2 Slide 6 and the slide before 6

These are the schematic symbols for transistors. **KC:** If we put an arrow in the schematic, the arrow points in the direction of conventional (positive) current flow. In an NMOS,

current flows from drain to source. If the arrow is missing, then you can determine if it's NMOS by inspecting the gate. If there's no bubble on the gate, it's an NMOS. **KC:** For a PMOS, we place a bubble on the gate to indicate that the polarity is the inverse of an NMOS.

1.3 Slide 7-8

KC: To turn on a PMOS transistor, we need to apply a gate-source voltage that is sufficiently negative, or

$$V_{GS} < V_T$$

The threshold voltage in a PMOS device is negative. The current is carried NOT by electrons but by HOLES.

KC: Holes are like electrons but they have positive charge. They are quasi-particles and require in depth knowledge of solid-state physics to fully understand ! For this class abstract that away and just pretend there are positive charges flowing. Even if you understand the physics, it's much easier to think about a hole flowing compared to motion of valence band electrons.

1.4 Slide 9

KC: An inverter is a fundamental and simple logic gate that inverts the signal to produce an inverted output. We can build it with a single transistor and a resistor, such as shown (NMOS + R), but the problem is that when the transistor is on, it draws a steady current from the supply.

KC: Having an NMOS and PMOS is a huge advantage because they are complementary, meaning that when we stack them and connect their gates to form an inverter, only one transistor will be on at a time if the voltage is in the normal logic levels (0V, 1V). If we apply a "0" to the gates (0V), then the NMOS is off but the PMOS is on. Likewise, if we apply a "1" to the gate (1V), the NMOS is on and the PMOS is off. This means there's never a DC conducting path between the supply and ground for this transistor stack, which means it does not burn static power.

KC: When NMOS and PMOS are both fabricated in the same process, we call the technology CMOS.

1.5 Slide 10

KC: Turning on and off inverters (and logic gates in general) is just like the RC circuits we've been analyzing ! The resistance originates from the transistor R_{on}, the channel on-resistance. The capacitance is the MOS-C gate capacitor which is an intrinsic part of the transistor.

1.6 Slide 11

KC: The I-V curve of a transistor is shown. Note the V is the drain-to-source voltage and the I is the drain-to-source current. A straight line I-V curve through the origin is a resistor

(or conductor), which is how the transistor behaves when it's "on", $V_{GS} > V_T$ for the NMOS.

Why a family of curves? **KC:** Because the conductivity of the transistor depends on the gate voltage. The higher V_{GS}, the more conductive, the steeper the slope.

KC: The curves flatten out if the drain-to-source voltage is too large. When this happens, the transistor no longer acts like a switch but more like a dependent current source. Dependent because the current depends on the gate voltage.

Out of scope but interesting: But why do the curves flatten out ? Using an NMOS for reference, the curves flatten out or saturate because if the drain voltage is too large, it negates the gate-to-channel field that produces the channel in the first place. So the channel near the drain end goes away and the current saturates because the drain-to-source voltage inside the channel remains essentially constant, at the peak value prior to saturation. The additional drain voltage gets dropped between the drain and channel where very high fields shoot carriers (electrons and holes) through a region that behaves like a vacuum.

1.7 Slide 15

The model of the transistor in saturation is a voltage-controlled current source.

1.8 Slide 17

We can build logic gates out of transistors. This is covered in CS 61C but a quick example shows how you build a NAND circuit, or an AND followed by a NOT.

Out of scope but interesting: To build any logic gate, place NMOS transistor in series to "NAND" them and put NMOS transistor in parallel to "NOR" them. To realize the PMOS network, use De Morgan's Law to synthesize the complementary network. In practice, NAND NMOS transistor turn into parallel PMOS transistors and parallel NMOS transistors turn into series PMOS transistors. Then you have a network that pulls the output to ground and a complementary network that pulls the output to V_{DD} based on the inputs.

Practice: Draw the schematic of a 3-input AND gate. Note that a NAND followd by a NOT (inverter) is a good way to realize this.