EECS 16B Designing Information Devices and Systems II
Spring 2019 UC Berkeley

Midterm 1: V1

1. Solar Panel (6 pts)

A particular solar panel's IV curves (labeled by irradiance) are given by:

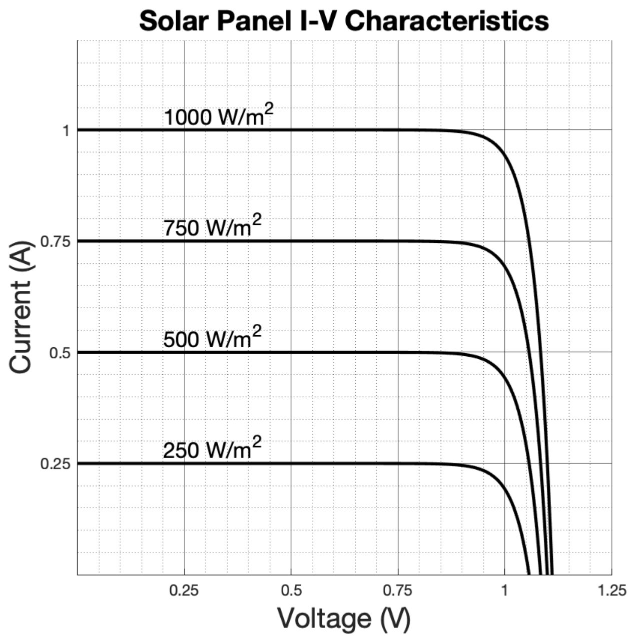
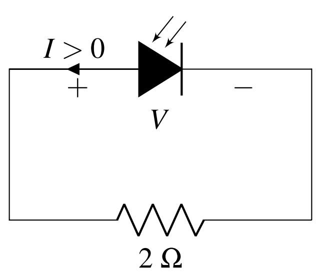


Figure 1: Solar Panel IV Curve

Your solar panel is connected to a load with resistance $R = 2\ \Omega$. The circuit diagram is given below, where the solar panel is depicted as a single pn-junction diode. Remember that current appears to flow "backward" out of the solar cell diode because it is *producing* power, rather than dissipating it.



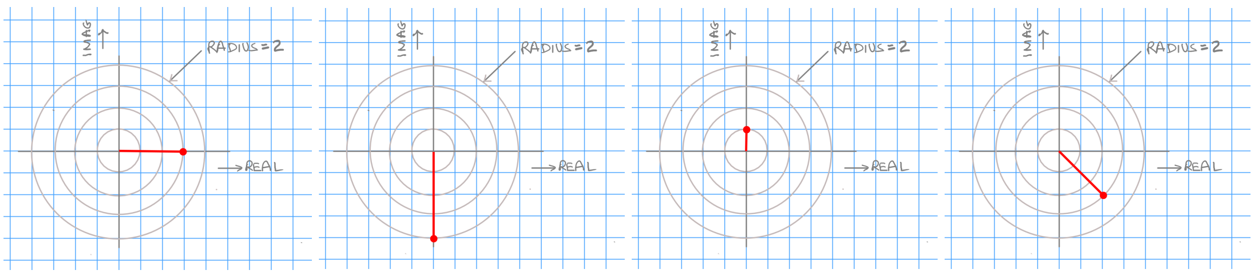
(a) (3 pts) **Draw the resistor's IV curve on the plot which includes the solar panel IV curves above.** The intersection between your resistance curve and a particular IV curve tells you where the solar panel will end up operating given a particular irradiance.

(b) (3 pts) **If the irradiance were 250 W/m^2, what would the power dissipated across the resistor be?**

2. Phasors (30 pts)

(a) (3 pts) Consider a resistor ($R = 1.5\Omega$), a capacitor ($C = 1$F), and an inductor ($L = 1$H) connected in series. **Give expressions for the impedances of Z_R, Z_C, Z_L for each of these elements as a function of the angular frequency ω.**

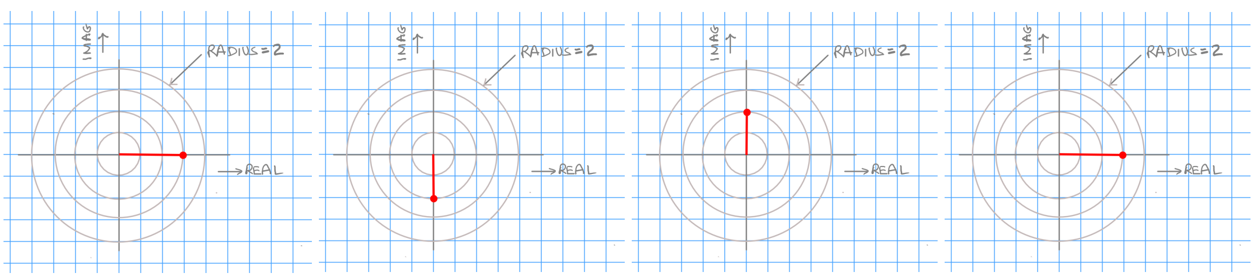
(b) (3 pts) **Draw the individual impedances as "vectors" on the same complex plane for the case $\omega = \frac{1}{2}$ rad/sec. Also draw the combined impedance Z_{total} of their series combination. Give the magnitude and phase of Z_{total}.** A logically sound graphical argument is sufficient justification.



a $Z_R(@\omega = 0.5)$ b $Z_C(@\omega = 0.5)$ c $Z_L(@\omega = 0.5)$ d $Z_{total}(@\omega = 0.5)$

Figure 2: Impedances at $\omega = 0.5$.

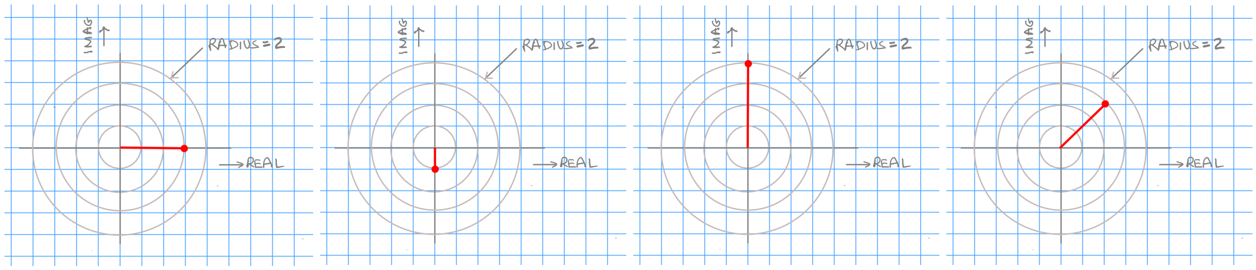
(c) (3 pts) **Draw the individual impedances as "vectors" on the same complex plane for the case $\omega = 1$ rad/sec. Also draw the combined impedance Z_{total} of their series combination. Give the magnitude and phase of Z_{total}.** A logically sound graphical argument is sufficient justification.



a $Z_R(@\omega = 1)$ b $Z_C(@\omega = 1)$ c $Z_L(@\omega = 1)$ d $Z_{total}(@\omega = 1)$

Figure 3: Impedances at $\omega = 1$.

(d) (3 pts) **Draw the individual impedances as "vectors" on the same complex plane for the case $\omega = 2$ rad/sec. Also draw the combined impedance Z_{total} of their series combination. Give the magnitude and phase of Z_{total}.** A logically sound graphical argument is sufficient justification.



a $Z_R(@\omega = 2)$ b $Z_C(@\omega = 2)$ c $Z_L(@\omega = 2)$ d $Z_{total}(@\omega = 2)$

Figure 4: Impedances at $\omega = 2$.

(e) (3 pts) **For the previous series combination of RLC elements, what is the "natural frequency" ω_n where the series impedance is purely real?**

(f) (15 pts) Suppose that we have the two-dimensional system of differential equations expressed in matrix/vector form:

$$\frac{d}{dt}\vec{x}(t) = A\vec{x}(t) + \vec{b}u(t) \tag{1}$$

where for this problem, we assume that $u(t)$ has a phasor representation $\widetilde{U}$. In other words, $u(t) = \widetilde{U}e^{+j\omega t} + \overline{\widetilde{U}}e^{-j\omega t}$. Suppose further that all the eigenvalues of A are such that any impact of an initial condition has completely died out by now. (i.e. the system is in steady-state.)

Assume that the vector solution $\vec{x}(t)$ to the system of differential equations (**??**) can also be written in phasor form as

$$\vec{x}(t) = \vec{\widetilde{X}}e^{+j\omega t} + \overline{\vec{\widetilde{X}}}e^{-j\omega t}. \tag{2}$$

Derive an expression for $\vec{\widetilde{X}}$ involving $A, \vec{b}$, $j\omega$, $\widetilde{U}$, and the identity matrix I.

(HINT: Plug (**??**) *into* (**??**) *and simplify, using the rules of differentiation and grouping terms by which exponential $e^{\pm j\omega t}$ they multiply.)*

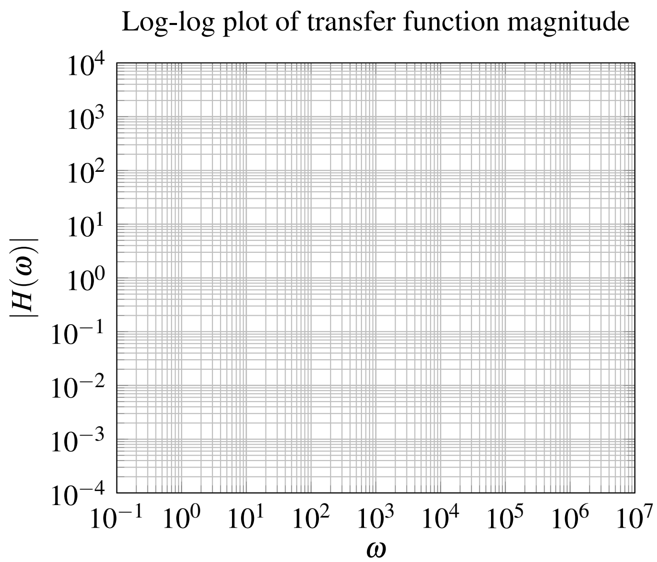
3. Low-pass Filter (34 pts)

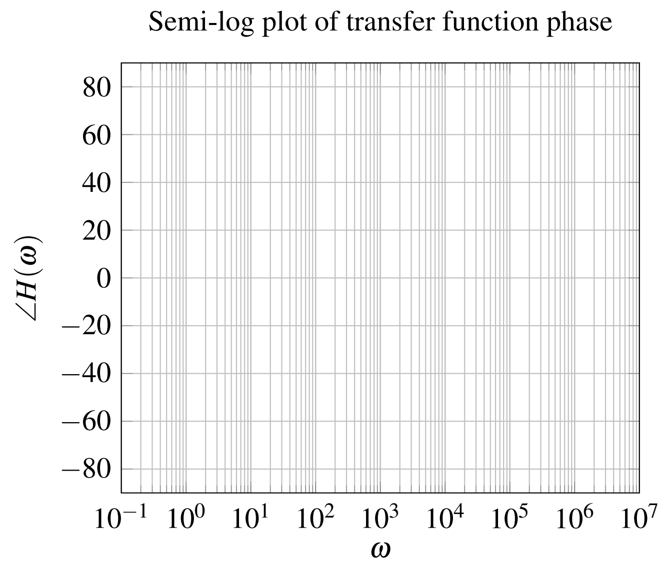
You have a 1 kΩ resistor and a 1 µF capacitor wired up as a low-pass filter.

(a) (4 pts) **Draw the filter, labeling the input node, output node, and ground.**

(b) (6 pts) **Write down the transfer function of the filter, $H(\omega)$.** Be sure to use the given values for the components.

(c) (6 pts) **Draw a straight-line approximation to the Bode plot (both magnitude and phase) of the filter on the graph paper below.**





(d) (6 pts) **Annotate your Bode plot with three circles, each representing where the straight line approximation has its worst errors.** One circle should be on the magnitude plot, and two should be on the phase plot and corresponds to an absolute error. **Label each circle with the error at that point** (multiplicative error in the case of the magnitude plot, and absolute error in terms of the phase plot). For the phase plot, feel free to use trigonometric functions if you want.

(e) (3 pts) **Write an exact expression for the *magnitude* of $H(\omega = 10^6)$, and give an approximate numerical answer.**

(f) (3 pts) **Write an exact expression for the *phase* of $H(\omega = 1)$, and give an approximate numerical answer.**

(g) (6 pts) **Write down an expression for the time-domain output waveform $V_{out}(t)$ of this filter if the input voltage is $V(t) = 1\sin(1000t)$ V.** You can assume that any transients have died out — we are interested in the steady-state waveform.

4. What Is The Use of a Ferrite Bead? (32 pts)

You've probably noticed how most laptop chargers have a short, thick section near the end that plugs into the laptop.

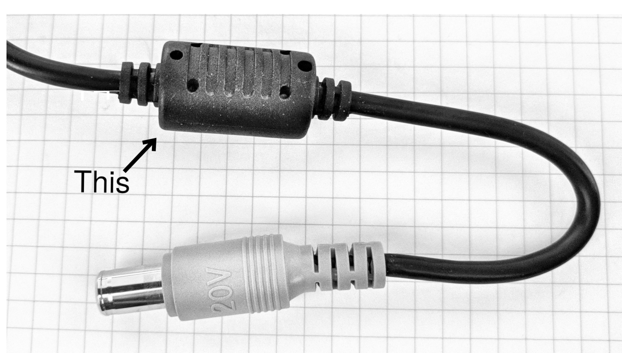


Figure 5: The short, thick section in question.

It's called a *ferrite bead*. It's a small shell of magnetic material called *ferrite*, and it makes the section of the wire that it surounds into **more** of an inductor (all wires have some inherent inductance, and in long wires, this is not negligible). Its purpose is to help filter out power supply noise. In circuit terms, the setup looks like this:

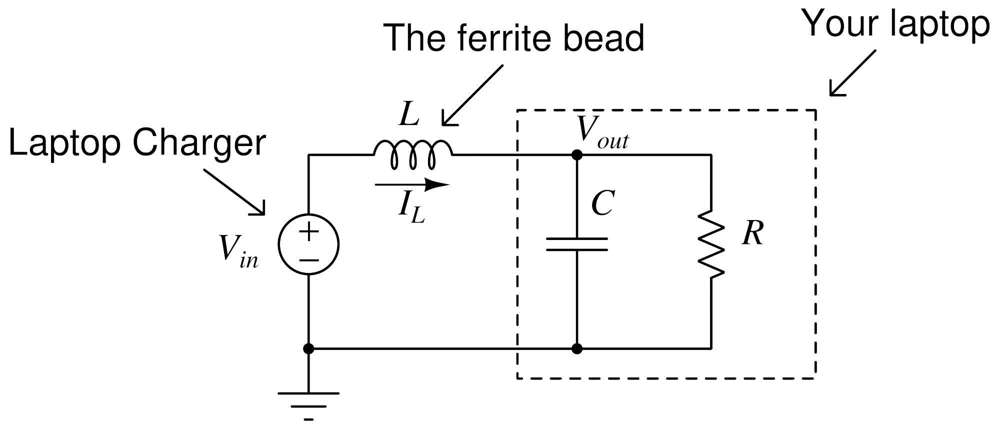


Figure 6: The ferrite bead in its natural habitat. L includes the wire inductance as well.

Here, V_{in} is the voltage produced by the charger, and V_{out} is the voltage that reaches the laptop. The resistor models the power consumption of the laptop, and the capacitor is part of an internal power supply filter.

In power supply filter design, the *time-domain* behavior of the filter is just as important as the *phasor-domain* behavior. However, because of exam-length limitations, we will just do the time-domain part here.

(a) (15 pts) Using $x_1(t) = I_L(t)$ and $x_2(t) = V_{out}(t)$ as state variables, **construct a matrix differential equation**

$$\frac{d}{dt}\vec{x}(t) = A\vec{x}(t) + \vec{b}V_{in}(t) \tag{3}$$

where $\vec{x}(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix}$. i.e. What are A and $\vec{b}$ for this circuit?

(b) (8 pts) **What are the eigenvalues of the matrix** A **you found in the previous part?** Your answer should be in terms of R, L, and C.

(c) (6 pts) The reason that we care about the time-domain behavior of this circuit is that *we must prevent resonance*. Although LC resonance is often useful, in a power supply it must be avoided to prevent dangerous high-voltage oscillations from occurring.

How can we tell if the filter we design will resonate or not? Well, any imaginary component to the eigenvalues can induce oscillation. Using the eigenvalues you found in the previous part, **find the smallest value for** L **such that the system will not oscillate. Your answer should be in terms of** R **and** C**.**

(d) (3 pts) Suppose $R = 4\,\Omega$, $C = 10\,\mu\text{F}$. Using these values, **choose the smallest value for** L **that does not allow for LC resonance.**

5. Transistor Switch Model (30 pts)

You have two CMOS inverters made from NMOS and PMOS devices. Both NMOS and PMOS devices have an "on resistance" of $R_{on} = 1\text{ k}\Omega$, and each has a gate capacitance (input capacitance) of $C = 1$ fF (femto-Farads = 10^{-15}). We assume the "off resistance" (the resistance when the transistor is off) is infinite (*i.e.*, the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter.

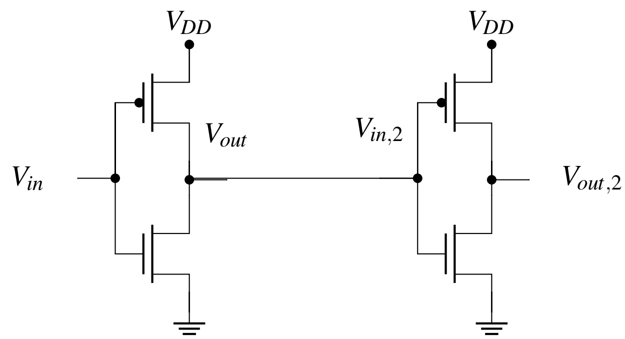


Figure 7: CMOS Inverter

(a) (14 pts) Assume the input to the first inverter has been low ($V_{in} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{in} = V_{DD}$). **Draw a simple RC circuit and write a differential equation describing the output voltage of the first inverter for time $t \geq 0$.** Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.

(b) (6 pts) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the initial slope, (3) the asymptotic value, and (4) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.**

(c) (6 pts) A long time later, the input to the first inverter switches low again. **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the initial slope, and (3) the asymptotic value.**

(d) (4 pts) For each complete input cycle described in the two steps above, **how much charge is pulled out of the power supply?** Give both a symbolic and numerical answer.

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