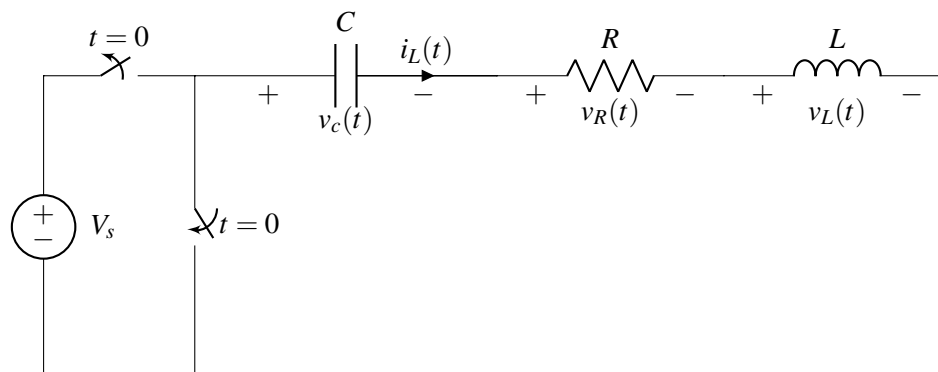EECS 16B   Designing Information Devices and Systems II
Summer 2020 UC Berkeley   Circuits Review

1. Circuits State Space (X pts)

Consider the following series RLC circuit from homework.

We used the state vector $\vec{x}(t) = \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix}$ to derive the following state equation for the circuit:

$$\frac{d}{dt}\vec{x}(t) = A\vec{x}(t) = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \vec{x}(t)$$

The eigenvalues of A are

$$\lambda = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

(a) Let's define a new state vector $\vec{\tilde{x}}(t) = \begin{bmatrix} i_L(t) + v_c(t) \\ v_L(t) \end{bmatrix}$.

Find an invertible matrix T, such that $\tilde{x}(t) = T\vec{x}(t)$. Assume that $R \neq 1\,\Omega$.

Solution:
We can write out the states $\tilde{x}_1$ and $\tilde{x}_2$ to realize that

$$\tilde{x}_1 = i_L + v_c = x_1 + x_2$$
$$\tilde{x}_2 = v_L = -v_c - v_r = -v_c - i_L \cdot R$$
$$= -Rx_1 - x_2$$

Therefore we conclude by saying that

$$T = \begin{bmatrix} 1 & 1 \\ -R & -1 \end{bmatrix}$$

(b) **Find the matrix $\tilde{A}$, such that $\frac{d}{dt}\vec{\tilde{x}}(t) = \tilde{A}\vec{\tilde{x}}(t)$.**

Solution:

$$\frac{d}{dt}\vec{x}(t) = A\vec{x}(t)$$

$$\frac{d}{dt}T^{-1}T\vec{x}(t) = AT^{-1}T\vec{x}(t)$$

$$\frac{d}{dt}T\vec{x}(t) = TAT^{-1}T\vec{x}(t)$$

$$\frac{d}{dt}\vec{\tilde{x}}(t) = \underbrace{TAT^{-1}}_{\tilde{A}}\vec{\tilde{x}}(t)$$

(c) **What are the eigenvalues of $\tilde{A}$?**

Solution:

The eigenvalues of $\tilde{A}$ are identical to the eigenvalues of A since

$$\det(\tilde{A} - \lambda I) = \det(TAT^{-1} - \lambda TT^{-1}) = \det(T(A - \lambda I)T^{-1}) = \det(A - \lambda I)$$

(d) Now let $\vec{\tilde{x}}(t) = \begin{bmatrix} i_L(t) \\ v_C(t) \\ v_L(t) \end{bmatrix}$.

Find a 3×3 matrix $\tilde{A}$ such that $\frac{d}{dt}\vec{\tilde{x}}(t) = \tilde{A}\vec{\tilde{x}}(t)$. Also, what are the eigenvalues of $\tilde{A}$?

Solution:

States $\tilde{x}_1$ and $\tilde{x}_2$ are identical to x_1 and x_2 in the original RLC example given above. Therefore, it remains to compute $\frac{d}{dt}\tilde{x}_3$ in terms of the other state variables.
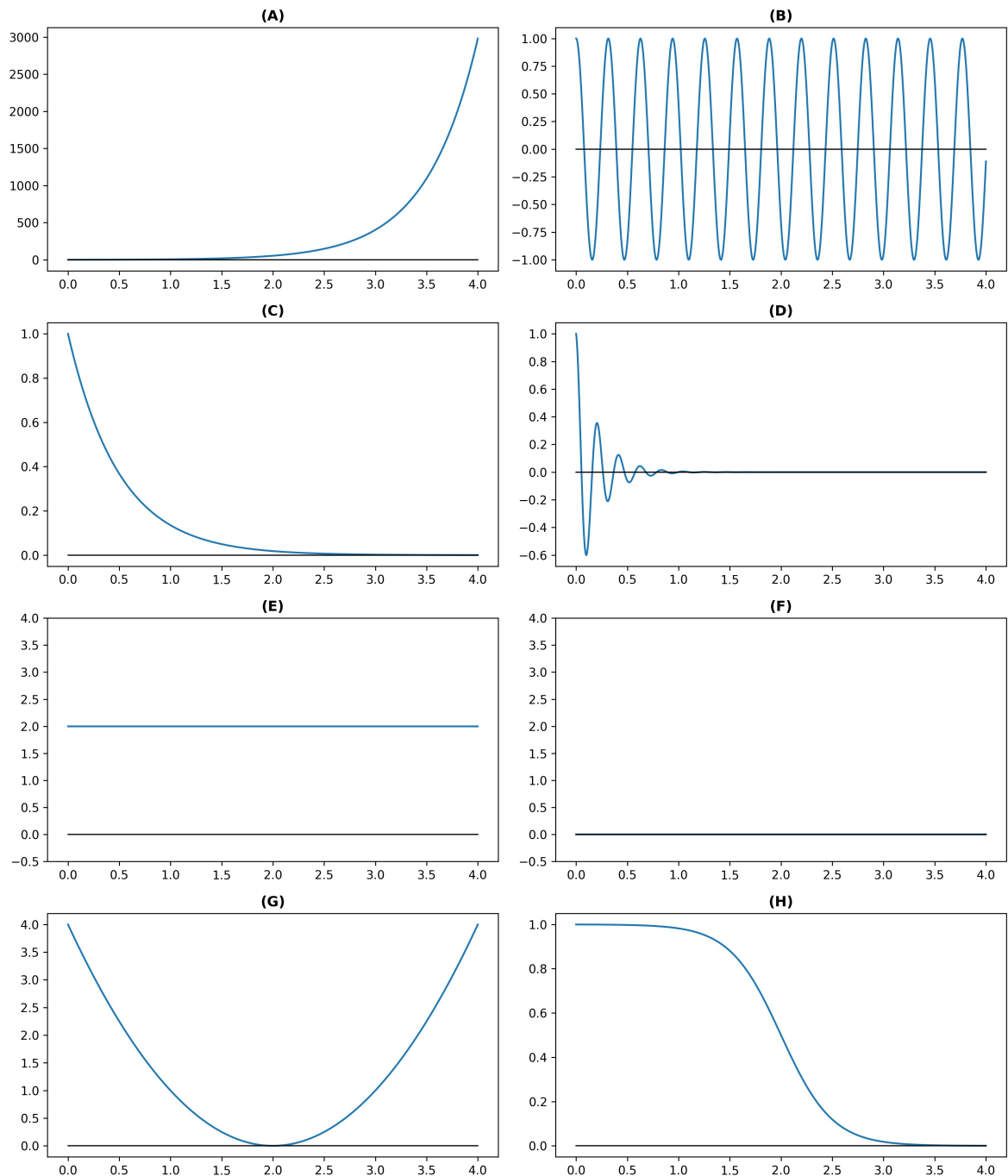
$$\tilde{x}_3 = -Rx_1(t) - x_2(t) \implies \frac{d\tilde{x}_3}{dt} = -R\frac{d\tilde{x}_1}{dt} - \frac{d\tilde{x}_2}{dt}$$

$$\frac{d\tilde{x}_3}{dt} = -R\left(-\frac{R}{L}x_1(t) - \frac{1}{L}x_2(t)\right) - \frac{1}{C}x_1(t) = \left(\frac{R^2}{L} - \frac{1}{C}\right)x_1(t) + \frac{R}{L}x_2(t)$$

We can therefore write out our state equations as

$$\frac{d}{dt}\vec{\tilde{x}}(t) = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} & 0 \\ \frac{1}{C} & 0 & 0 \\ \frac{R^2}{L} - \frac{1}{C} & \frac{R}{L} & 0 \end{bmatrix} \vec{\tilde{x}}(t)$$

$$\lambda = 0, -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

Intuitively, we can think of $\tilde{x}_3$ as a redundant state that gives no extra information to the system.

(e) Assume that we measure $v_c(t)$. **Which of the following are possible graphs of $v_c(t)$?**

Solution: The general solution must be of the form $\alpha e^{\lambda_1 t} + \beta e^{\lambda_2 t}$.

A: Not possible, since $\lambda \leq 0$ and there are no inputs into the system.

B: Possible if $R = 0$.

C: Possible if λ is real and less than 0.

D: Possible if λ is complex.

E: Not possible, since the steady of $v_c(t)$ must be zero.

F: Possible if $v_c(0) = 0$.

G: Not possible, since the response blows up and is parabolic.

H: Not possible, since the convexity of $v_c(t)$ cannot change.

2. Derive the Integrator (X pts)

Consider the following circuit:
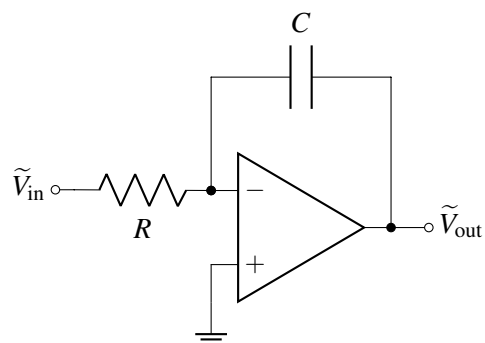
(a) **Find the transfer function of this circuit** $H(\omega) = \frac{\tilde{V}_{\text{out}}}{\tilde{V}_{\text{in}}}$.
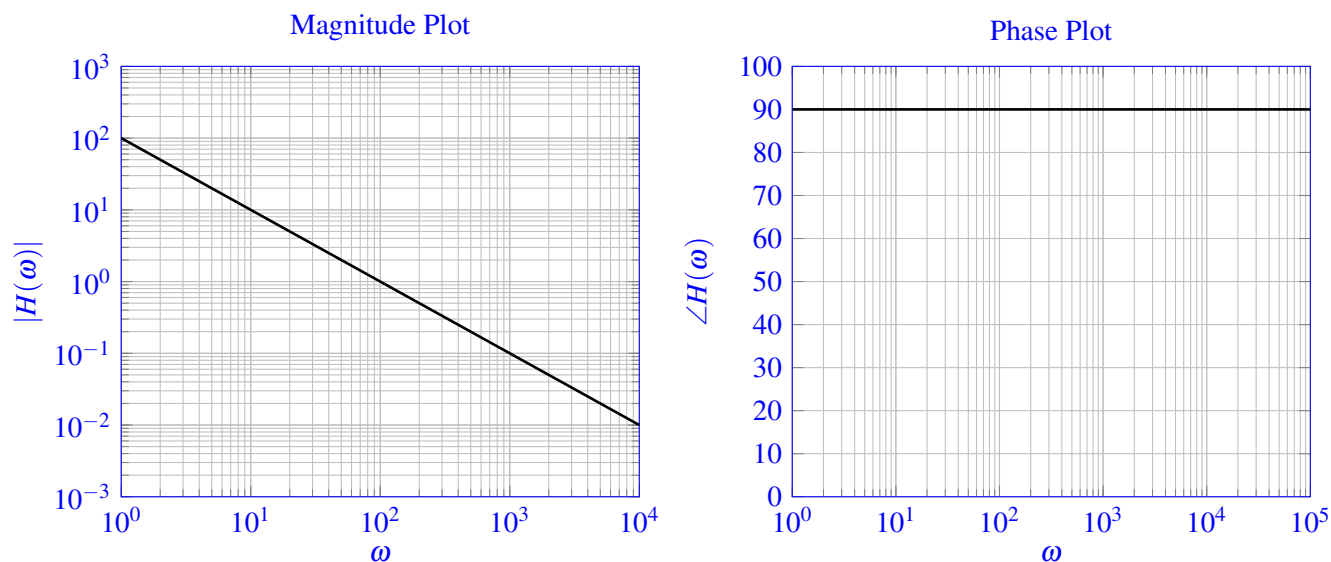
Solution:

$$H(\omega) = -\frac{1}{j\omega RC}$$

(b) **Draw the Bode magnitude and phase plots of the transfer function.** Assume that $RC = 10^{-2}$.

Hint: Try plotting the magnitude and phase for $\omega = 1, 10, 100, \dots$ and look for a pattern.

Solution:

$$\left|H(\omega)\right| = \frac{1}{\omega RC} \qquad \angle H(\omega) = \frac{\pi}{2}$$

(c) **Find** $v_{\text{out}}(t)$ **for the following inputs** $v_{\text{in}}(t)$. You can assume that any transients have died out.

    i. $v_{\text{in}}(t) = 10\sin(100t)$

    ii. $v_{\text{in}}(t) = -5\cos\left(10^3 t + \frac{\pi}{2}\right)$

Solution:

i.
$$\omega = 10^2, \left|H(10^2)\right| = 1, \angle H(10^2) = \frac{\pi}{2} \implies v_{out}(t) = 10\sin\left(100t + \frac{\pi}{2}\right)$$

ii.
$$\omega = 10^3, \left|H(10^3)\right| = 0.1, \angle H(10^3) = \frac{\pi}{2} \implies v_{out}(t) = 0.5\cos\left(10^3 t\right)$$

(d) **Find $v_{\textbf{out}}(t \to \infty)$ if $v_{\textbf{in}}(t) = 5\,\text{V}$.** *Hint:* What is ω?

Solution:

Since $\omega = 0$, $H(0) \to -\infty$. Therefore, $v_{out}(t \to \infty) \to -\infty$.

(e) Assume that $v_{\text{out}}(0) = 0\,\text{V}$ and that $v_{\text{in}}(t) = 5\,\text{V}$. **Find an expression for $v_{\textbf{out}}(t)$ for $t \geq 0$.**
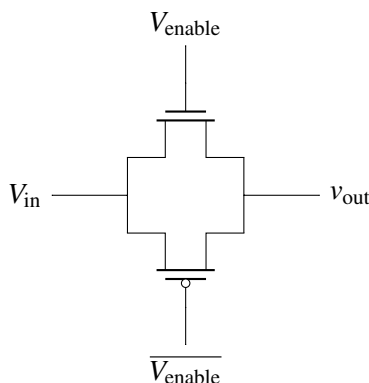
Solution:

$$\frac{v_{in}}{R} = -C\frac{dv_{out}}{dt}$$

$$v_{out}(t) = -\frac{1}{RC}\int_0^t v_{in}\,d\tau = -\frac{1}{RC}\int_0^t 5\,d\tau = -\frac{5t}{RC}$$

3. The Old Switcheroo (X pts)

Consider the following circuit that implements a switch using transistors.

V_{enable} and V_{in} are digital signals that can be either at 0 V or 1 V. If $V_{enable} = 1$ V, the switch is closed and V_{in} is connected to V_{out}. Otherwise, if $V_{enable} = 0$ V, the switch is open.

The threshold voltage of the NMOS is $V_{t,n} = 0.3$ V, and the threshold voltage of the PMOS is $V_{t,p} = -0.3$ V. You may approximate $0.3 \approx e^{-1}$.

Assume that at time $t = 0$, $V_{in} = 1$ V, $v_{out}(0) = 0$ V, and $V_{enable} = 1$ V. We want to know how $v_{out}(t)$ behaves over time for $t \geq 0$.

(a) **Draw the equivalent circuit of the switch for $t \geq 0$ using the resistor-capacitor model of the transistor. Determine which transistors are on and off.**

**Solution:** After labelling the Gate, Source, and Drain, we realize both PMOS and NMOS transistors are on.
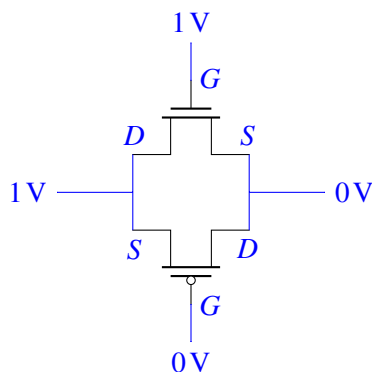
An equivalent circuit model is
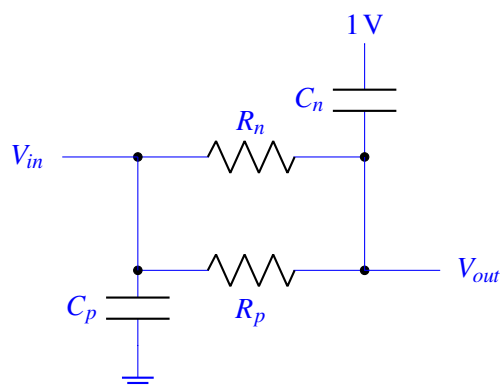
(b) **Write down a differential equation for $V_{\textbf{out}}(t)$ that describes the behavior for some time after $t \geq 0$.** Assume that both the NMOS and PMOS transistors have an on-resistance of R_{on} and a gate-source capacitance of C_{gs}.

Solution: We can redraw the circuit as
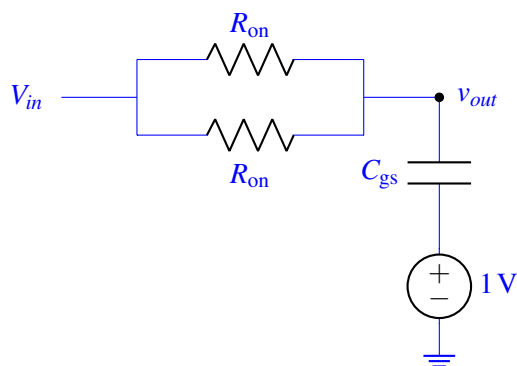
This yields the differential equation

$$\frac{dv_{out}}{dt} = -\frac{2}{R_{\text{on}}C_{\text{gs}}}(V_{out} - V_{in})$$

(c) **Solve for $V_{\textbf{out}}(t)$. Assume that $R_{\text{on}}C_{\text{gs}} = 1 \times 10^{-9}$ s.**

Solution: This is a first-order differential equation with a constant input which has solution

$$V_{out}(t) = 1 - e^{-\frac{2}{R_{\text{on}}C_{\text{gs}}}t} = 1 - e^{-2 \times 10^9 t}$$

(d) **Until what time $T \geq 0$ is your differential equation valid?**

Solution: The differential equation will only be valid when both transistors are on. When V_{out} reaches 0.7 V, the NMOS turns off.

$$1 - e^{-2 \times 10^9 T} = 0.7\,\text{V}$$
$$e^{-2 \times 10^9 T} = 0.3\,\text{V} \approx e^{-1}$$
$$-2 \times 10^9 T = -1$$
$$T = \frac{1}{2 \times 10^9\,\text{s}} = 0.5\,\text{ns}$$

8

4. Simulated Inductor - Gyrator (X pts)

Resistors, capacitors, inductors, and transistors make up the basic building blocks for many interesting and useful circuits. However, for certain applications, the size of the inductance would require very large inductors which may not feasibly fit on a small chip.

One way to work around this constraint is to simulate an inductor using a circuit called a gyrator. A simulated inductor can be implemented using a capacitor, two resistors, and one op-amp connected as in Fig. 1.
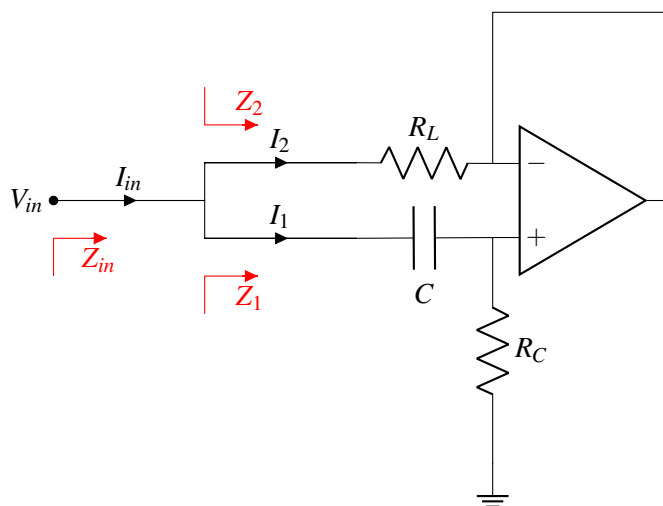

Figure 1: Gyrator

We will show that at low frequencies the simulated inductor in Fig. 1 behaves the same as the equivalent RL circuit in Fig 2.
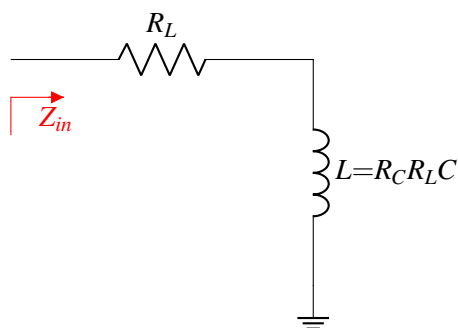

Figure 2: Gyrator - Equivalent RL circuit

The input impedance for the RL circuit in Fig. 2 is given by

$$Z_{in} = R_L + j\omega R_C R_L C = R_L + j\omega L_{eq} \tag{1}$$

where $L_{eq} = R_C R_L C$ is the desired effective inductance of the gyrator circuit.

We will work through the steps to see that these two circuits are equivalent by showing that, under certain conditions, their impedances are the same. In addition, we will show some cases where the gyrator fails.

We can determine the total input impedance Z_{in} in Fig. 1 by solving for the impedance of each branch (Z_1 and Z_2) separately. We then will find Z_{in} by recognizing that the two branches appear in parallel, and thus the input impedance is the parallel of the two branch impedances.

(a) **First, determine the impedance Z_1, which is the impedance of the lower branch**.

Solution: By the op-amp 'golden rules', the input impedance into the $+$ terminal is infinite, so no current will flow into the $+$ terminal of the op-amp. As such, C and R_C appear in series, and we can write

$$I_1 = \frac{V_{in}}{\frac{1}{j\omega C} + R_C}$$

and we get

$$Z_1 = \frac{V_{in}}{I_1} = R_C + \frac{1}{j\omega C}$$

(b) **Determine the impedance Z_2**. Hint: Use the properties of an op-amp you have learned. You should find that your answer is of the form $Z_2 = a + b \cdot L_{eq}$ (recall $L_{eq} = R_C R_L C$ is the desired effective inductance).

Solution: To find Z_2, we need to find the current I_2, and then use $Z_2 = \frac{V_{in}}{I_2}$. To determine I_2, we need to find the voltage across R_L.

Because the op-amp is in negative feedback, by the 'golden rules', we know $V_- = V_+$.

We can find V_+ (and thus V_-) by recognizing that the lower branch (C and R_C) forms a voltage divider. Hence,

$$V_+ = V_- = V_{in} \frac{R_C}{Z_1}$$

Now we can solve for the current I_2

$$I_2 = \frac{\Delta V}{R_L} = \frac{V_{in} - V_-}{R_L} = \left(V_{in} - V_{in} \frac{R_C}{Z_1} \right) \frac{1}{R_L} = V_{in} \frac{Z_1 - R_C}{Z_1 R_L}$$

Now that we know I_2, we get that

$$Z_2 = \frac{V_{in}}{I_2} = \frac{Z_1 R_L}{Z_1 - R_C} = \frac{\left(R_C + \frac{1}{j\omega C} \right) R_L}{\left(R_C + \frac{1}{j\omega C} \right) - R_C}$$

$$= (R_C + \frac{1}{j\omega C}) \cdot R_L \cdot j\omega C$$

$$= R_L + j\omega C R_L R_C$$

Hence,

$$Z_2 = R_L + j\omega C R_L R_C = R_L + j\omega L_{eq}$$

(c) For the impedance

$$Z_{in} = Z_1 || Z_2$$

what is the approximate effective impedance of Z_{in} if $Z_1 \gg Z_2$? Keep the answer in terms of the variables Z_1 and Z_2.

Solution:

$$Z_{in} = Z_1 || Z_2 = \frac{Z_1 Z_2}{Z_1 + Z_2}$$

$$= Z_2 \frac{Z_1}{Z_1 \left(1 + \frac{Z_2}{Z_1}\right)}$$

$$\approx Z_2 \frac{Z_1}{Z_1 \cdot 1}$$

$$= Z_2$$

(d) We would ideally like to design the gyrator circuit so that its impedance is given by equation:

$$Z_{in,desired} = R_L + j\omega L_{eq} \tag{2}$$

However, we note that Z_{in} is the parallel of Z_1 and Z_2. Using the intuition above, **what design choices can we make for components C, R_C, and/or R_L to ensure that $Z_{in} \approx R_L + j\omega L_{eq}$? What component values can we still freely choose to set the desired L_{eq}?**

Solution: We note that Z_2 is our desired input impedance. We would thus like to have that $Z_{in} \approx Z_2$. Because $Z_{in} = (Z_1 || Z_2)$, we would like to make Z_1 large, so that its impedance is negligible in the overall parallel expression.

How do we make Z_1 large? Note that

$$Z_1 = R_C + \frac{1}{j\omega C} \qquad\qquad Z_2 = R_L + j\omega L_{eq}$$

We see that R_C and C appear only in Z_1. Thus, if we make R_C very large or C small (or both) we can guarantee that $Z_1 \gg Z_2$, and thus $Z_{in} \approx Z_2 = R_L + j\omega L_{eq}$.

We then note that $L_{eq} = R_C R_L C$. Even though we must choose R_C to be large or C to be small, we still have the freedom of choosing R_L to set our desired value for L_{eq}.

(e) Now, let us check under which conditions the two circuits are equivalent (i.e. under which conditions the approximation that $Z_{in} \approx Z_2$ holds). Let V_{in} be a DC voltage, i.e. its frequency is 0. **Are the input impedances for the two circuits equivalent? If not, what is the input impedance for each circuit?**

Solution: The input impedance are the same.
We find that $Z_1 = R_C + \frac{1}{j\omega C} = R_C + \frac{1}{0} = \infty$, and that $Z_2 = R_L + j\omega L_{eq} = R_L + 0 = R_L$. Thus, $Z_{in} = (Z_1 || Z_2) = (\infty || R_L) = R_L$, which is the value of the desired $Z_{in,desired}$ at $\omega = 0$.

(f) Let V_{in} be an oscillating cosine with an infinitely large frequency. **Are the input impedances for the two circuits equivalent? If not, what is the input impedance for each circuit?**

Solution: The impedances are different.
We find that $Z_1 = R_C + \frac{1}{j\omega C} = R_C + \frac{1}{\infty} = R_C$, and that $Z_2 = R_L + j\omega L_{eq} = R_L + \infty = \infty$. Thus, $Z_{in} = (Z_1 || Z_2) = (R_C || \infty) = R_C$.

However, the desired Z_{in} is $Z_{in} = R_L + j\omega L_{eq} = R_L + j\infty L_{eq} = \infty$.

Thus the impedances are not the same. **This is one of the restrictions of using a gyrator to simulate an inductor. It only works if the frequency is 'low enough' that the approximation we made above is valid.**

Another more 'intuitive' way of finding the impedance for the gyrator circuit is to note that at very high frequencies, the capacitor acts as a short. Thus, $V_+ = V_- = V_{in}$ so no current flows through R_L. All the current will flow through R_C

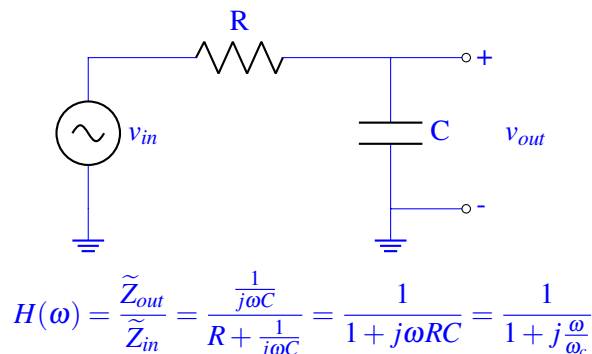Hence, the impedance for the first circuit would be R_C.

5. Biomedical Filter Design (X pts)

Maxwell has been hired to design a biomedical sensor that can detect and output recordings of Alpha brain-waves in the frequency range 8 Hz to 12 Hz. Unfortunately, our sensor is faulty: it is also picking up Gamma brainwaves in the frequency range 40 Hz to 100 Hz, interfering with our ability to get clean recordings of alpha brainwaves. Therefore, he wants to create a new design for our sensor that can remove this interference, giving us a clearer signal.
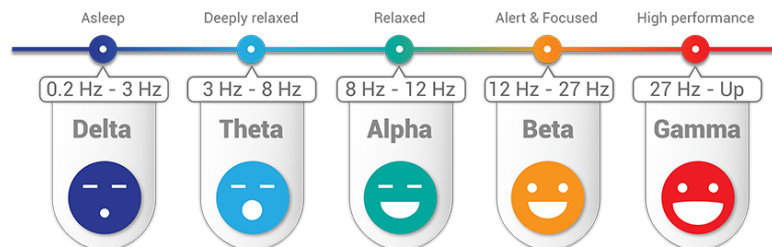
(a) Assuming Max only has access to resistors and capacitors, let us design a filter to remove the Gamma brainwave interference. **Sketch the corresponding circuit and write out its transfer function.**

Solution: We should use a low-pass filter. The interference is at a higher frequency than our desired signal, so we filter out the higher frequencies and keep the lower frequencies.

$$H(\omega) = \frac{\tilde{Z}_{out}}{\tilde{Z}_{in}} = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} = \frac{1}{1 + j\omega RC} = \frac{1}{1 + j\frac{\omega}{\omega_c}}$$

.

(b) Max can set the cutoff frequency to 10 Hz, 20 Hz, 32 Hz, 100 Hz, or 120 Hz. Which is the best cutoff frequency, and why?

Solution: We should minimize the cutoff frequency. The transfer function will start filtering frequencies sooner, meaning that we maximize the amount by which higher frequencies are attenuated. We however, do not want to risk cutting off the desired signal.

Therefore, 20 Hz is the best cutoff-frequency we can choose; the Gamma brainwaves will be attenuated more if we choose 20Hz than 32Hz because the transfer function will start filtering at a lower frequency. 10Hz is too low and risks cutting off Alpha brainwaves.

(c) There is only a 3.3 kΩ resistor in our workstation. **What capacitor value should Max use for our filter?**

Solution: If we want a cutoff frquency of 20Hz, then $f = \frac{\omega_c}{2\pi} = \frac{1}{2\pi RC} = 20Hz$. As a result,

$$C = \frac{1}{2\pi \cdot 33 \cdot 10^3 \Omega \cdot 20Hz} = 2.41\,\mu F$$

(d) Plot the magnitude and phase response of this filter. **How much have we attenuated the Gamma waves at $f = 40\,\text{Hz}$?**

Solution: Note that we are not plotting on a log-log scale due to how close the frequencies are.

Magnitude plot:

Phase plot:
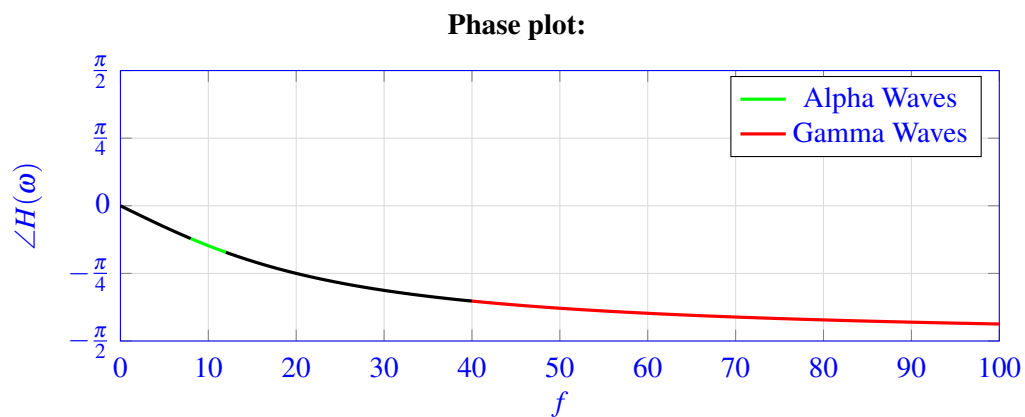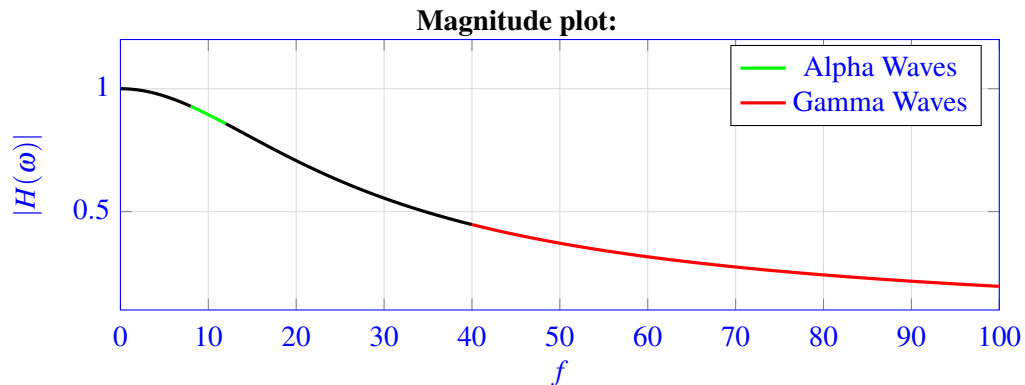
At $f = 40\,\text{Hz}$, the Gamma waves have been attenuated by a factor of around 0.5. Note that the filter's performance is quite poor since the cutoff frequency is spaced so close to the frequencies we need to attenuate. We also cannot lower the cutoff frequency since we would be attenuating our desired Alpha brainwaves from 8 to 12 hertz.

(e) Max consults his friend Taejin for some advice and he suggests to cascade two low-pass filters with the same resistor and capacitor values, with a buffer as shown below:
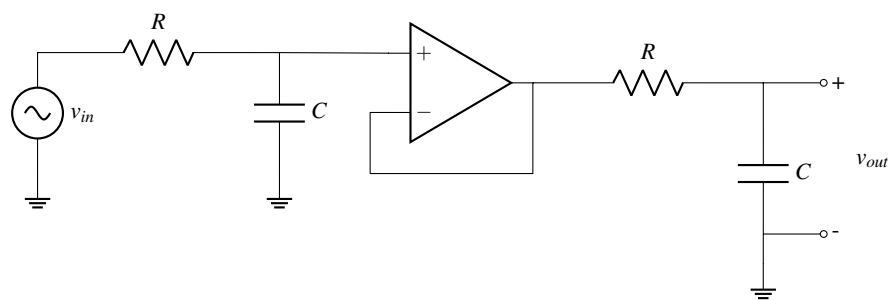
What is the magnitude of the transfer function $H(\omega)$? In addition, what would happen if we cascaded a large number of filters together?

Solution: The transfer function of this circuit would be the product of two low-pass transfer functions.

$$H(\omega) = \frac{1}{1 + j\omega RC} \cdot \frac{1}{1 + j\omega RC} = \frac{1}{(1 + j\omega RC)^2}$$

Its magnitude will be

$$\left|H(\omega)\right| = \frac{1}{1 + (\omega RC)^2}$$

This will also have low-pass behavior, and will have a faster rate of cutoff after the cutoff frequency since there is a double pole at $\omega = \frac{1}{RC}$.

Magnitude Plot (One Buffer):
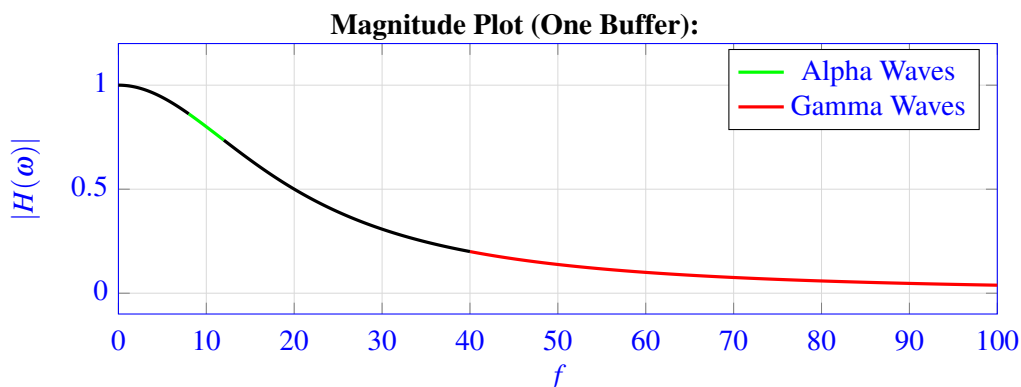
In fact we can cascade, a series of filters, to get an even better rate of dropoff. The plots for 5 and 10 cascaded filters are shown below. However, notice that as n gets larger, $\left|H(\omega)\right|$ drops off, and we may have to use an amplifier to restore the gain:

14

Magnitude Plot (Five Buffers):

Magnitude Plot (Ten Buffers):

Magnitude Plot (Ten Buffers G = 5):
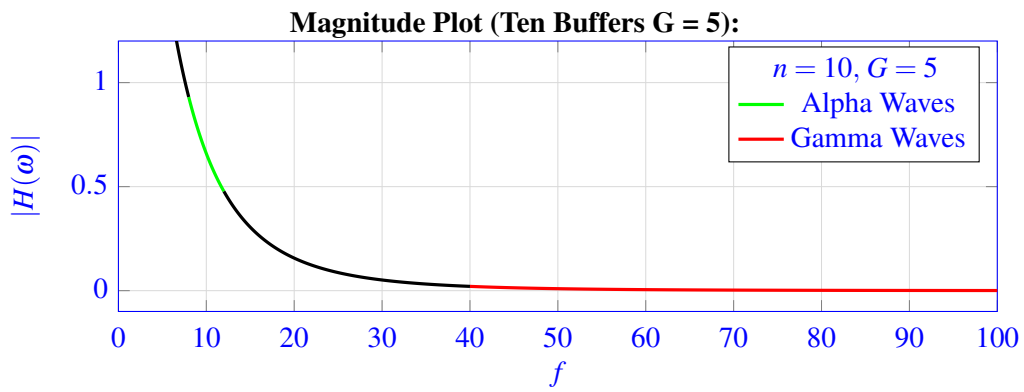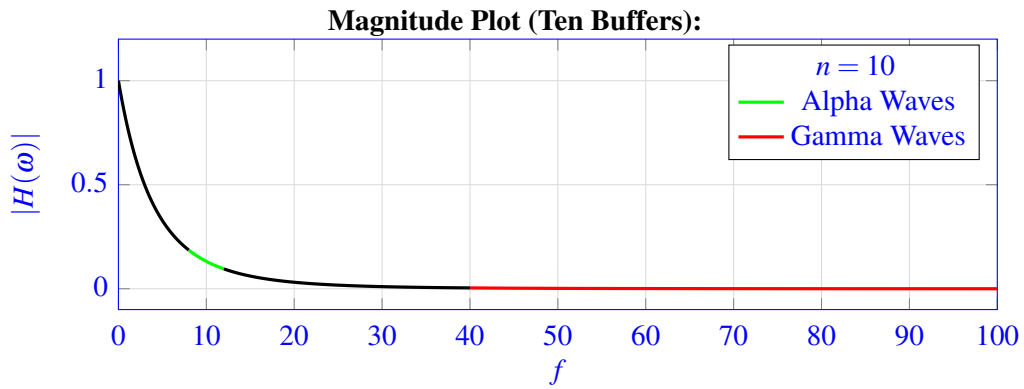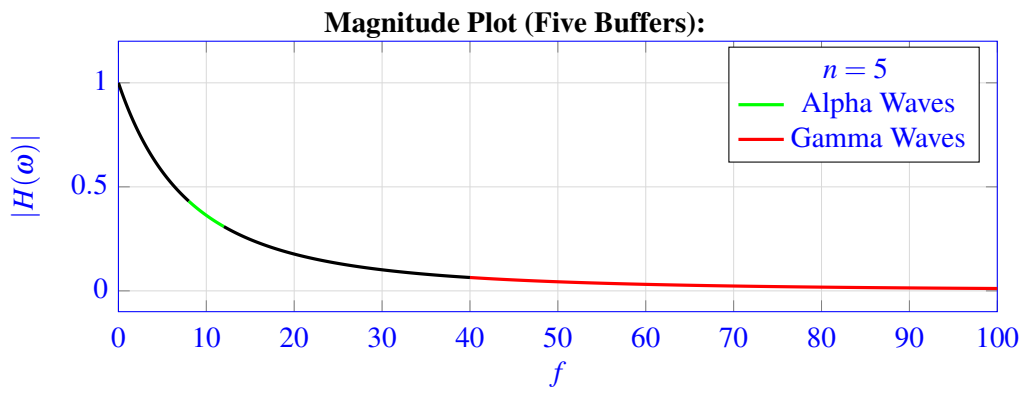
6. Attack of the Deltas

Maxwell successfully designed his Biomedical sensor to capture the Alpha brainwaves while filtering out the Gamma waves. However, he now notices that there is a another source of interference–Delta brainwaves–in the frequency range 0.5Hz to 4Hz. To combat this, he decides to use a resonance filter.
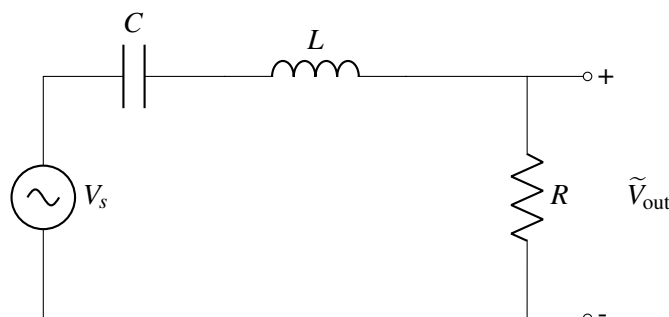
(a) **What is the transfer function of this filter?**

Solution: Using previous phasor analysis techniques, we can see this as a voltage divider by taking the capacitor and inductor as one impedance in series.

$$H(\omega) = \frac{R}{R + j\omega L + \frac{1}{j\omega C}} = \frac{j\omega RC}{1 + j\omega RC + (j\omega)^2 LC}$$

(b) **Where should Max set the cutoff frequencies?**

Solution: We currently want to capture Alpha brainwaves running at 8 to 12 Hz, while filtering out Gamma brainwaves at 40 to 100 Hz, and Delta brainwaves at 0.5 to 4 Hz. We want to space our cutoff frequences as far apart as possible, but also try to put the center frequency as the average of the desired frequency range. Therefore, to space away the Deltas while keeping the Alphas, the low frequency should be set to 6 Hz. The high frequency can vary, You can pick a high cutoff of 14 Hz, to put 10 Hz in the center, or you can also choose 26 Hz in between 12 and 40 to create a much larger bandwith.

(c) **What are the cutoff frequencies of this filter in terms of $R, L,$ and C?**

Solution: Remember that in order to find the cutoff frequencies, we find the frequencies at which $|H(\omega)| = \frac{1}{\sqrt{2}}$.

$$|H(\omega)| = \frac{\omega RC}{\sqrt{(1 - \omega^2 LC)^2 + (\omega RC)^2}} = \frac{1}{\sqrt{2}}$$

Squaring both sides, we get:

$$\left(\frac{\omega RC}{\sqrt{(1 - \omega^2 LC)^2 + (\omega RC)^2}}\right)^2 = \frac{(\omega RC)^2}{(1 - \omega^2 LC)^2 + (\omega RC)^2} = \frac{1}{2}$$

Cross multiplying, we get:

$$(1 - \omega^2 LC)^2 + (\omega RC)^2 = 2(\omega RC)^2 \quad \text{or} \quad (1 - \omega^2 LC)^2 = (\omega RC)^2$$

We take the square root of both sides, and taking the negative case into account,

$$(1 - \omega^2 LC) = \pm \omega RC$$

Now, we can use the quadratic formula twice, and note that we'll have four solutions, but we will only consider the positive valued ones.

$$\omega = \pm \frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}$$

(d) Let's pick values of $R, L,$ and C to set our cutoff frequencies to those picked in part (b) Suppose you have a $500\,\Omega$ resistor. **What values should you pick for your capacitior and inductor?**

Solution: From the previous part, our cutoff frequencies are:

$$\omega_h = \frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}, \text{ and } \omega_l = -\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}.$$

This means that our bandwith is $\Delta\omega = \omega_h - \omega_l = \frac{R}{L}$.

From here onward, there are multiple ways to design our resonance bandpass filter all of which have bandwidth $\Delta\omega = 2\pi\Delta f$. We can start by picking a low cutoff-frequency, $f_\ell = 6\,\text{Hz}$ since that will give us the most bandwith possible and is equidistant from the Alpha and Delta waves.

(1) **Option 1:** Pick a high frequency $f_h = 14\,\text{Hz}$, to put the center frequency at $10\,\text{Hz}$. meaning our bandwith will be $8\,\text{Hz}$ or $16\pi\,\frac{\text{rad}}{\text{s}}$.

(2) **Option 2:** Pick the resonance frequency at $10\,\text{Hz}$ so that the magnitude of $H(\omega)$ peaks at $10\,\text{Hz}$. The choice of f_h isn't quite arbitrary but we'll pick $f_h = 16\,\text{Hz}$ to simplify our calculations.

(3) **Option 3:** Give ourselves a wider bandwidth by picking a high cutoff of $f_h = 26\,\text{Hz}$. The bandwith will be $20\,\text{Hz}$ or $40\pi\,\frac{\text{rad}}{\text{s}}$.

In each option, we can can compute our inductor through the formula $L = \frac{R}{\Delta\omega}$.

(1) $L = \frac{500}{16\pi} = 9.95\,\text{H}$

(2) $L = \frac{500}{20\pi} = 7.95\,\text{H}$

(3) $L = \frac{500}{40\pi} = 3.98\,\text{H}$

We pick our capacitor values around either the center frequency $\omega_{center} = \frac{1}{2}(\omega_l + \omega_h) = \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}$ or the resonance frequency $\omega_0 = \frac{1}{\sqrt{LC}}$.

(1)

$$\left(\frac{R}{2L}\right)^2 + \frac{1}{LC} = 400\pi^2 \text{ so } C = \frac{1}{L(400\pi^2 - (\frac{R}{2L})^2)} = 30.3\,\mu\text{F}$$

(2)

$$\frac{1}{\sqrt{LC}} = 2\pi \cdot 10 \text{ so } C = \frac{1}{\omega_0^2 L} = 31.8\,\mu\text{F}$$

(3)

$$\left(\frac{R}{2L}\right)^2 + \frac{1}{LC} = 1024\pi^2 \text{ so } C = \frac{1}{L(1024\pi^2 - (\frac{R}{2L})^2)} = 40.8\,\mu\text{F}$$

(e) **Plot the frequency response of the filter designed above using the resistor, capacitor and inductor values picked in the previous part.**

Solution: We can plot this on a computer by plugging in our values for R, L, C into the magnitude equation:

$$|H(\omega)| = \frac{\omega RC}{\sqrt{(1 - \omega^2 LC)^2 + (\omega RC)^2}} \tag{3}$$

Notice that our signal is attenuated for values of f between 0.5 and 4, and it is also attenuated for values of f above 40. Lastly, for values of f between 8 and 12 Hz, the transfer function is close to 1.
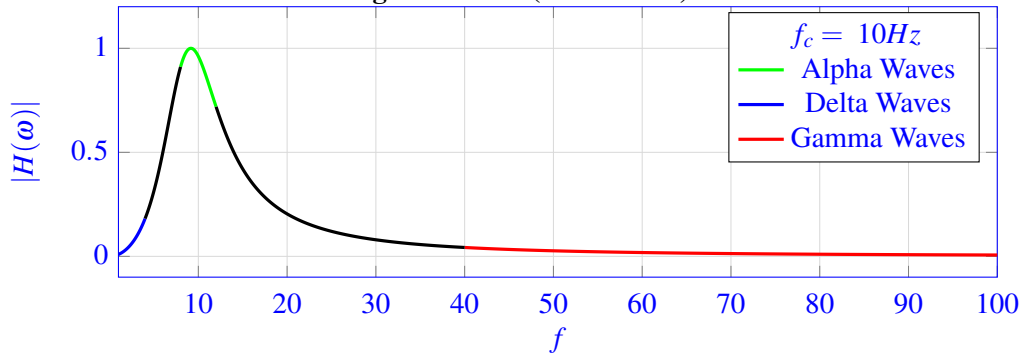
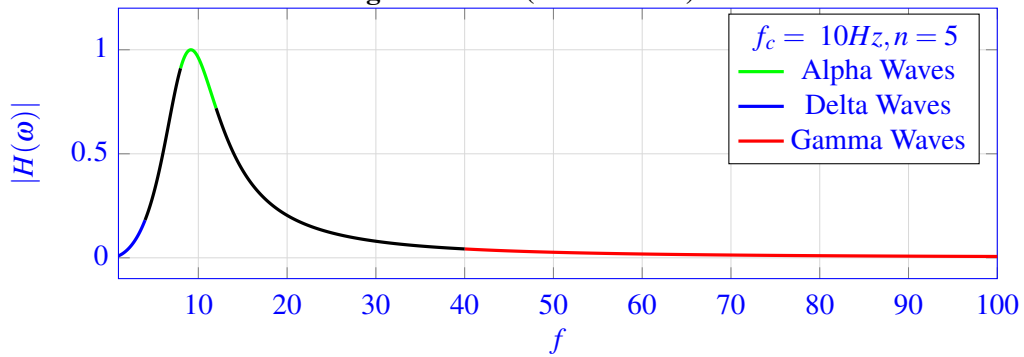The plot of $|H(\omega)|$ is below for both choices of R, L, C:
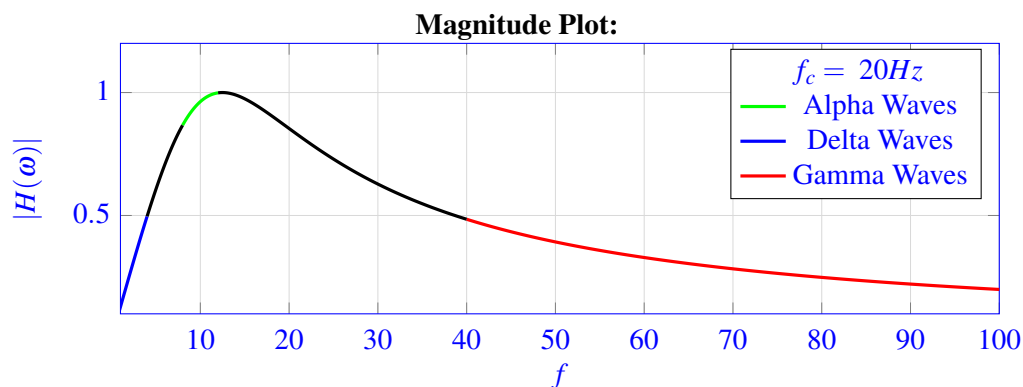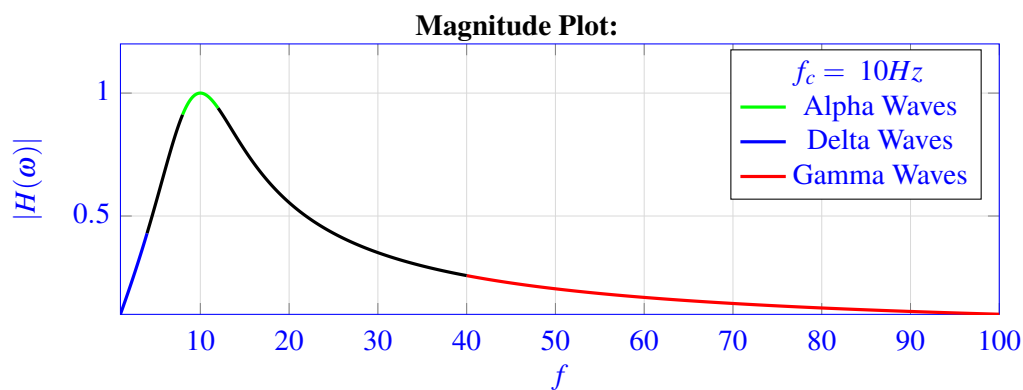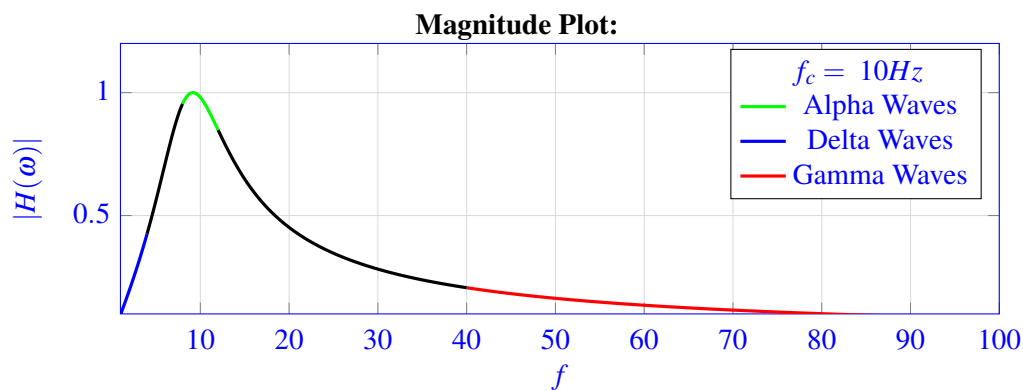
(f) Max notices again that while the filter is attenuating the necessary frequencies, it isn't doing that good of a job. **Try plotting the responses using Taejin's idea from the previous question of cascading multiple filters with buffers in between.**

Solution: We first plot the response with one buffer. Notice however, that if we increase the number of buffers, while we attenuate the Delta and Gamma waves, since we are taking the gain to the nth power, we lose a significant amount of gain. Therefore, a tradeoff of attenuating the noise vs getting a stronger gain must be made.
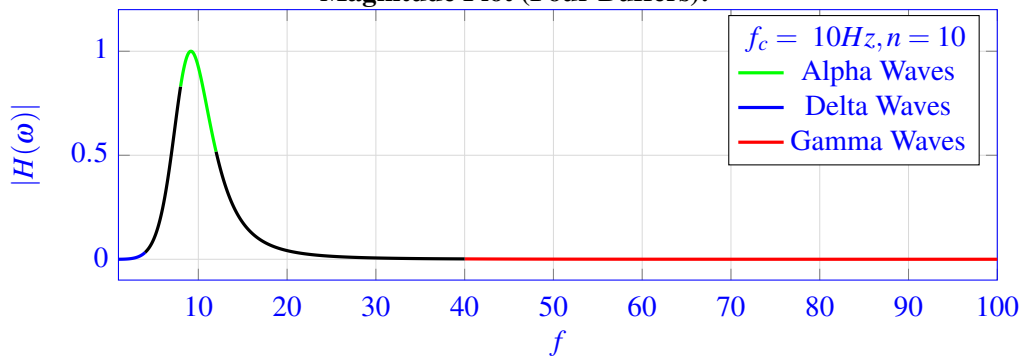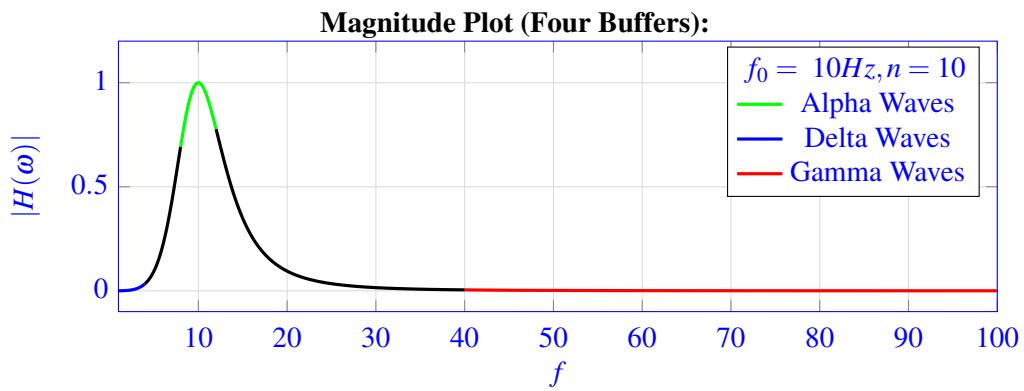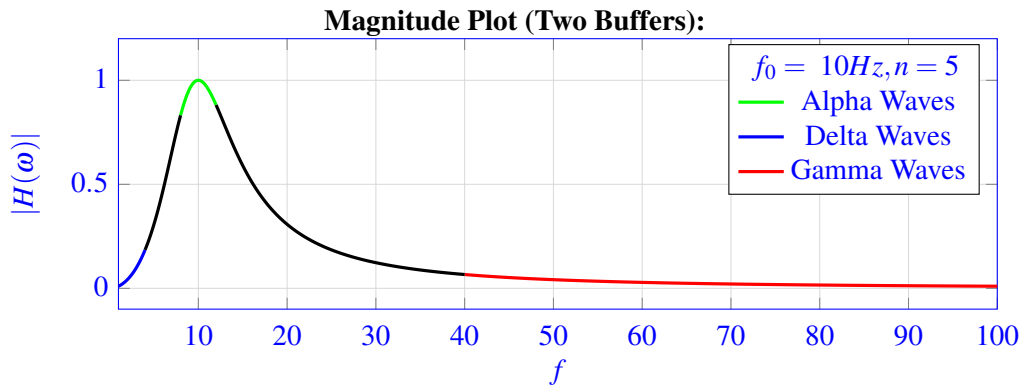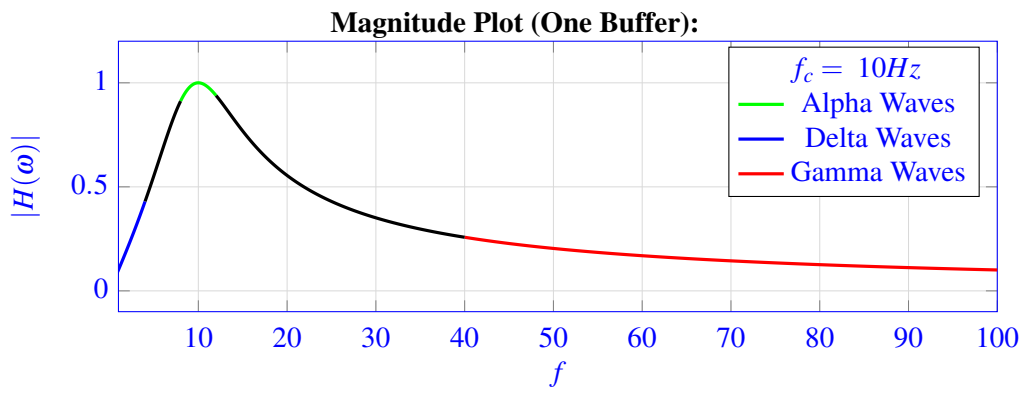
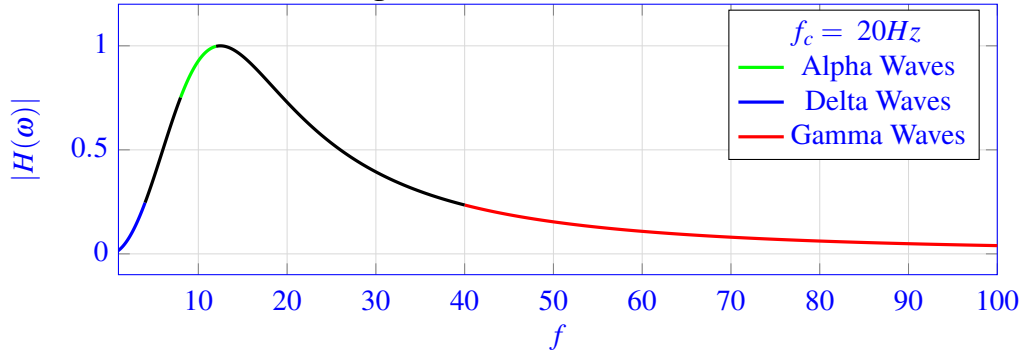**Magnitude Plot (One Buffer):**

Magnitude Plot (Two Buffers):

Magnitude Plot (Four Buffers):

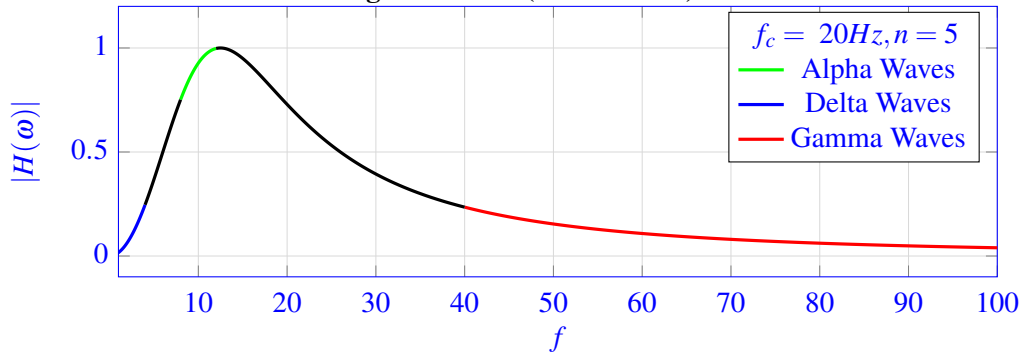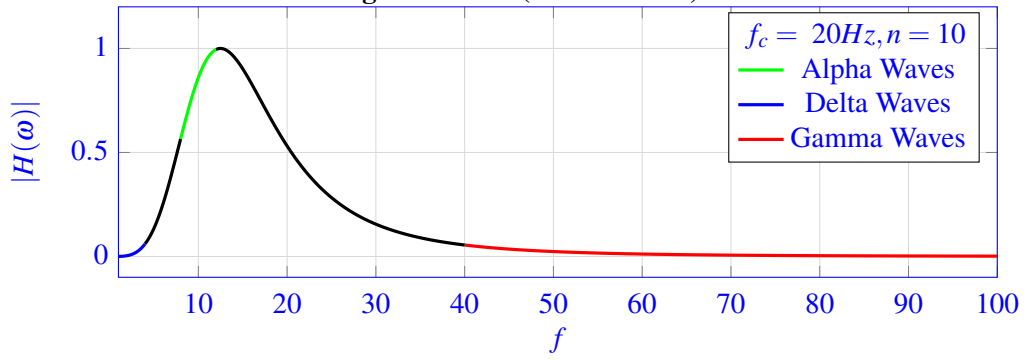**Magnitude Plot (One Buffer):**

$f_c = 10Hz$
Alpha Waves
Delta Waves
Gamma Waves

Magnitude Plot (Two Buffers):

$f_0 = 10Hz, n = 5$
Alpha Waves
Delta Waves
Gamma Waves

Magnitude Plot (Four Buffers):

$f_0 = 10Hz, n = 10$
Alpha Waves
Delta Waves
Gamma Waves

Magnitude Plot (One Buffer):

$f_c = 20Hz$
Alpha Waves
Delta Waves
Gamma Waves

Magnitude Plot (Two Buffers):

$f_c = 20Hz, n = 5$
Alpha Waves
Delta Waves
Gamma Waves

Magnitude Plot (Four Buffers):

$f_c = 20Hz, n = 10$
Alpha Waves
Delta Waves
Gamma Waves

7. **Powering a Clock**

Taejin is trying to design a clock using a series of inverters made up of transistors. He is currently thinking of two the approaches for a single inverter.
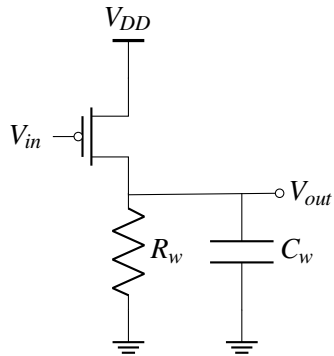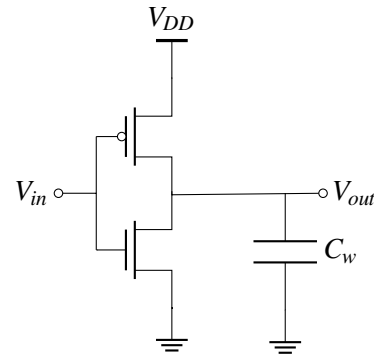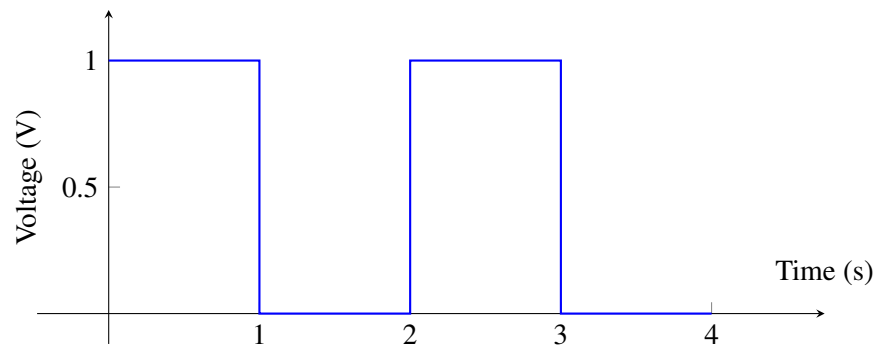

Figure 3: Single PMOS Model   Figure 4: CMOS Inverter Model

Unfortunately both models contain parasitic wire resistance and capacitance $R_w = 500\,\Omega$ and $C_w = 3\,\mu\text{F}$. Both PMOS and NMOS transistors have voltage threshold of $|V_{th}| = 0.7$ and $V_{DD} = 1\,\text{V}$.

To test both models, Taejin decides to give the following square wave input.

(a) Suppose Model A has switch resistance $R_p = 1\,\text{k}\Omega$ and gate capacitance $C_p = 5\,\mu\text{F}$. Assuming $v_{out}(0) = V_{DD}$, **solve for $v_{out}(t)$ for $T \in [0,2]$ and plot the response.**

Solution: We can break up the input into two segments in which $v_{in} = 1\,\text{V}$ and $v_{in} = 0\,\text{V}$. Looking at the first window, the PMOS transistor will be off since $V_{SG} = 0\,\text{V} < |V_{th}|$.
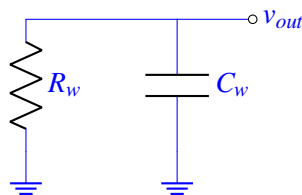
The equivalent circuit can be drawn as follows

Figure 5: PMOS "Off" State

This is a simple RC circuit with the following differential equation for $t \in [0,1)$.

$$\frac{dv_{out}}{dt} = -\frac{v_{out}}{R_w C_w}$$

The solution to this differential equation is of the form

$$v_{out}(t) = V_{DD}e^{-t/\tau} \text{ for } \tau = R_w C_w.$$

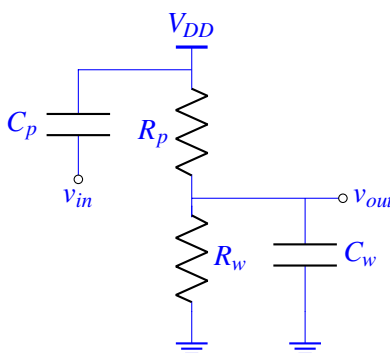Now let us look at the second window where the PMOS transistor is on since $V_{SG} = 1\,\text{V} > |V_{th}|$.

Figure 6: PMOS "On" State

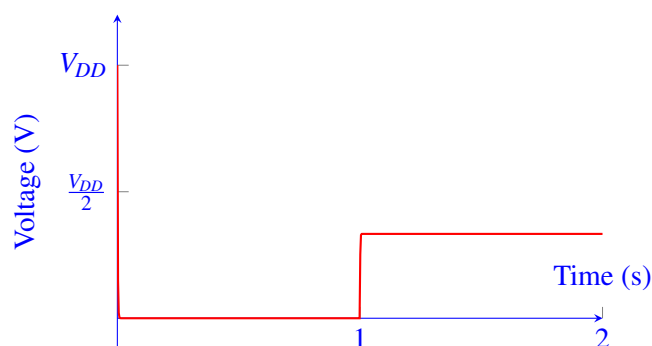Since $\tau = 6\,\text{ms}$, we can assume the capacitor fully discharges and $v_{out}(1) = 0\,\text{V}$.

The differential equation for $t \in [1,2)$ will be

$$\frac{V_{DD} - v_{out}}{R_p} = C_w \frac{dv_{out}}{dt} + \frac{v_{out}}{R_w}$$

$$\frac{dv_{out}}{dt} = -\frac{v_{out}(R_w + R_p)}{R_p R_w C_w} + \frac{V_{DD}}{R_w C_w}$$

The solution to this differential equation is

$$v_{out} = \frac{R_w}{R_p + R_w}V_{DD}\left(1 - e^{-(t-1)/\tau}\right) \text{ for } \tau = \frac{R_w R_p}{R_w + R_p}C_w.$$

The response for $t \in [0,2]$ is plotted below. Note how the output is unable to reach V_{DD} and will only reach $\frac{1}{3}V_{DD}$.

(b) Now suppose Model *B* has the same PMOS switch resistances and gate capacitances as model *A*. The NMOS transistor has switch resistance $R_n = 1\,\mathrm{k\Omega}$ and gate capacitance $C_n = 2\,\mathrm{\mu F}$. Assuming $v_{out}(0) = V_{DD}$, **solve for $v_{out}(t)$ for $T \in [0,2]$ and plot the response.**

Solution: Looking at the first window for $t \in [0,1)$ the PMOS is OFF and the NMOS is ON. The equivalent circuit will look identical to the single PMOS inverter
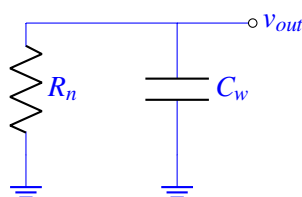

Figure 7: PMOS "Off" / NMOS "On" State

As a result, the solution for $t \in [0,1)$ should be

$$v_{out}(t) = V_{DD}e^{-t/\tau} \text{ for } \tau = R_nC_w.$$

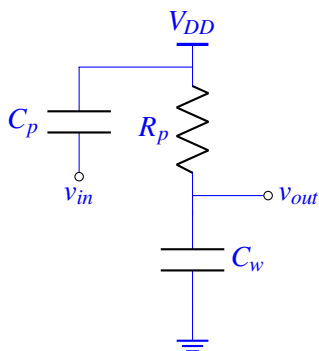Now let us look at the second window where the PMOS is ON and the NMOS is OFF.

Figure 8: PMOS "On" / NMOS "Off" State

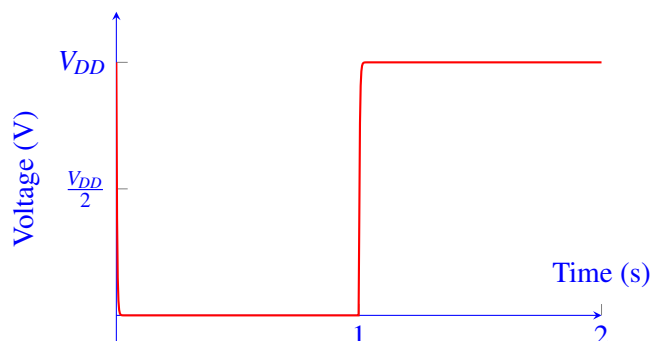Since $\tau = 6\,\mathrm{ms}$, we can assume the capacitor fully discharges and $v_{out}(1) = 0\,\mathrm{V}$. The differential equation for $t \in [1,2)$ will be

$$\frac{dv_{out}}{dt} = -\frac{v_{out}}{R_pC_w} + \frac{V_{DD}}{R_pC_w}$$

The solution to this differential equation is

$$v_{out}(t) = V_{DD}(e^{-(t-1)/\tau}) \text{ for } \tau = R_p C_w.$$

The response for $t \in [0,2]$ is plotted below

(c) Compare the energy dissipation of both models for $t \in [0,2)$. **Which model dissipates more energy?**

Solution: For the first phase when $t \in [0,1)$, the energy dissipation for both models is the same

$$U_{c,1} = \frac{1}{2}C_w V_{DD}^2 = 1.5 \times 10^{-6} V_{DD}^2$$

In the second phase, Model B will dissipate the same energy

$$U_{c,2} = \frac{1}{2}C_w V_{DD}^2 = 1.5 \times 10^{-6} V_{DD}^2$$

Model A in the second phase however will dissipate approximately

$$U_{c,2} = \frac{V_{DD}^2}{R_p + R_w} \cdot 1\,\text{s} = 0.33 \times 10^{-3} V_{DD}^2$$

Therefore, we conclude by saying Model A dissipates more energy.

(d) **Compare the individual delays of each inverter over one cycle ($t \in [0,2)$.)**

Solution:

(i) Model A:
- In the first window, it takes the output $\tau = R_w C_w = 1.5\,\text{ms}$ to switch from high to low.
- In the second window, it takes the output $\tau = \frac{R_w R_p}{R_w + R_p}C_w = 1\,\text{ms}$ to switch from low to high.

(ii) Model B:
- In the first window, it takes the output $\tau = R_n C_w = 3\,\text{ms}$ to switch from high to low.
- In the second window, it takes the output $\tau = R_p C_w = 3\,\text{ms}$ to switch from low to high.

Overall, Model A switches faster than B but Model A is dissipating more power and is unable to reach V_{DD}.

(e) Taejin now builds his clock by implementing a ring oscillator for both models. He starts both clocks by setting $V_{DD} = 1\,\text{V}$ and $V_{in}(0) = 0\,\text{V}$. For Model A however, he notices that his clock is stuck at a certain value. **Explain why this is the case and how he can fix his clock.**
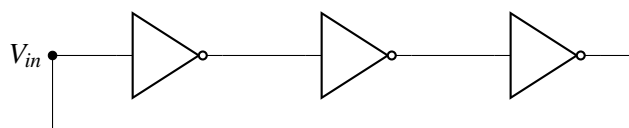
Figure 9: Ring oscillator with 3 inverters

Solution: If $V_{in}(0) = 0$, then the output of the first inverter will switch to $\frac{1}{3}V_{DD}$. However, this means V_{SG} for the second inverter is $V_{SG} = \frac{2}{3}V_{DD} < V_{th}$.

As a result, every PMOS transistor in the oscillator will be on and the clock will be stuck at $\frac{1}{3}V_{DD}$.

Taejin can fix his clock by increasing V_{DD} so that $V_{SG} = \frac{2}{3}V_{DD} \geq V_{th} = 0.7\,\text{V}$. However, this will come at the cost of more power dissipation.

Contributors:

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