The low power demo project supports the following boards:

Tower card:
- TWR-K25LN128 – Revision C

In order to run the project connect TWR module with a Serial Card in an elevator set. Assemble TWR-K25LN128 with SERIAL card and primary and secondary tower cards. If you use the tower serial card then set J24 and J26 to select the ELEV setting. Also power up the elevator with the switch on the primary elevator before connecting the power to the twr OPENSDA usb connector.

This project can also be run standalone using the com port instantiated by the OPEN SDA interface. The power select jumper J8 must be in it's default position[1-2]. If used with the tower elevators J8 can be set to [2-3] to select the input to regulator from the switched elevator supply. Leave the cable to debugger plugged in to maintain a good functioning system.

1. Connect the USB cable between your computer and the TWR-K25LN128 board's mini USB connector. Allow the drivers to install.

2. Connect 9 pin DB9 cable to the serial card DB9 connector.

3. If you are using an external debugger(JLINK or JLINK Lite) connect the JLINK 20 pin connector to the 10 pin header on the board(J10).

4. If using a JLINK-lite VDD must be 3.3 V - Move jumper on J3 to connect 1-3 for 3.3 V. If you have a full JLINK the jumper can be placed on 1-3 for 3.3V or 3-5 for 1.8 V.

5. To measure IDD of the MCU the shunt on the back side of J7 must be cut (not applicable to Rev. B or later hardware). After that to ensure VDD is supplied to the MCU placed jumper on J7 or measure IDD with current meter.

6. Open the low_power_demo.eww workspace with the IAR IDE tool.
Locate this in the ..build\iar\low_power_demo folder.

7. Under the workspace window pull down select the configuration low_power_demo_tower-FLASH_128KB

8. Select Project --> Clean

9. Select Project --> Build All

10. Select Project --> Download and Debug or the debug icon to program the demo code into the flash of the MCU.

11. When the Select Device window pops up select the "Cancel" button.

12. Open a terminal utility like Hyperterminal or Putty to communicate with the UART of the MCU. Configure for 19200 baud no Parity, No Flow Control.

13. Hit the Run button or F5 to start code execution or if no debug is needed select the X to close the debugger.

14. For some of the low power mode current measurements you must disconnect the JTAG(SWD) cable and Power Cycle the Tower kit. Do this using the switch on the side of the primary elevator.

15. Observe the menu options on the terminal window and enter the letter or number of the desired option.

```
This banner is referred to the "..... RESET BANNER ......"" below
---------------------------------------------------------------------
Power-on Reset
Low-voltage Detect Reset
KL2580pin      100pin
Low Power Line with Cortex M0+

SRAM Size:  16 KB
Silicon rev 15
 Flash parameter version 0.0.8.0
Flash version ID 6.0.1.0
Flash size:  128 KB program flash, 4 KB protection region
 LLWU configured pins PTC3/SCI1_RX/FTM0_CH2 is LLWU wakeup source
 LLWU configured modules as LLWU wakeup sources = 0x01,
*--------------D E B U G    D I S A B L E D------------------*
*-------Press SW4 then press Reset to re-enable debug---------*
*-----------------------------------------------------------*
*                    KL Low Power DEMO                      *
*                    Sep 13 2012 14:37:13                   *
*-----------------------------------------------------------*
  in Run Mode  !   in PEE mode now at 48000000 Hz

Select the desired operation
0 for CASE 0: Enter VLLS0 with POR disabled (Very Low Leakage STOP 0) NO POR
1 for CASE 1: Enter VLLS0 with POR enabled (Very Low Leakage STOP 0) with POR
2 for CASE 2: Enter VLLS1 (Very Low Leakage STOP 1)
3 for CASE 3: Enter LLS with LPTMR 1 second wakeup loop (Low Leakage Stop)
4 for CASE 4: Enter VLLS3 (Very Low Leakage STOP 3)
5 for CASE 5: Enter LLS(Low Leakage Stop)
6 for CASE 6: Enter VLPS(Very Low Power Stop)
7 for CASE 7: Enter VLPR(Very Low Power RUN) in BLPE (8 MHz Crystal)
8 for CASE 8: Exit VLPR(Very Low Power RUN)
9 for CASE 9: Enter VLPW(Very Low Power WAIT)
A for CASE 10: Enter WAIT from RUN or VLPW from VLPR
B for CASE 11: Enter Normal STOP from RUN or VLPS from VLPR
C for CASE 12: Enter PARTIAL STOP 1 with both system and bus clocks disabled
D for CASE 13: Enter PARTIAL STOP 2 with system clock disabled and bus clock enabled
```

E for CASE 14: Running coremark 2 times in RUN with CPO then without CPO
F for CASE 15: Running coremark 2 times in VLPR with CPO then without CPO
G for CASE 16: Enable LPTMR to wakeup every 5 seconds from any mode except VLLS0
H for CASE 17: Disable LPTMR wakeup
I for CASE 18: Enter VLPR in BLPI at Core Frequency of 4 MHz
J for CASE 19: Enter VLPR in BLPI at Core Frequency of 2 MHz
K for CASE 20: Enter Compute Mode run for(i=0;i<wait_count;i++)
L for CASE 21: To enable DEBUG
>

NOTES:

1. Note that the banner displays some significant information including the operational mode and the clock frequency of the system clock.

2. Do not remove the "IAR" or platform define ("TOWER") from the defined symbols list.

3. If you have the debugger connected and have started by hitting the "Go" button, entering some low power modes will cause you to exit debug mode. If this happens just abort the debug session.

4. If you want to test LLS mode exit you must choose the VDD of 1.8 V by moving the jumper on J3 to 3-5. This is due to an issue with the PMC during LLS mode exit. See errata list for Rev. 1.0 devices.

INTRODUCTION:

CLOCKING: The MCU always comes up out of reset in FEI mode. During the system initialization, the software in start.c and sysinit.c sets up the basic I/O and clocks to execute code in RUN mode with the clock mode PEE (PLL Engaged External). This clock mode is using the external 8 MHz crystal to clock the MCU. The on-chip PLL is set to generate the 48 MHz clock for MCU operation.

I/O:

UART0, the low power uart is being used to communicate with the terminal. The clock for the UART is the system clock. UART0 TXD is PTA14 and RXD is PTA15.

SWITCHES:

RESET - press the Reset button on the tower board to restart the code.
SW3 - PTA4 - This is a pin interrupt input. The code will acknowledge a press of this button with the PORT A ISR
"[porta_isr] porta4 ISF cleared" is displayed when you press SW3
SW4 - PTC3 - This is a Low Leakage Wakeup input. There will be NO response from the code when SW4 is pressed unless you are in VLLS0,VLLS1, VLLS3 or LLS low power modes. If you are in one of these modes SW4 is enabled to wake the MCU when this buttons is pressed.

LEDS: There are 4 LEDs on the Tower board, some of which have jumpers that connect the LED to the MCU. These LED are illuminated during the menu prompt but are turned off when an operation is selected.

CURRENT MEASUREMENT:

To make power measurements on the tower card use JP7. Measuring the voltage drop across a precision 10 OHM resistor is the optimal way of measuring MCU IDD. Place a low current DMM is another option, but care must be taken when measuring the current during mode transitions.
BOARD Modification: If you have Rev A of the TWR board then you must cut the shunt on the back of the PCB under JP7.

LOW POWER BOOT OPTIONS:

CAUTION: PLEASE TAKE CARE DURING THIS - or you might secure your MCU.
To enable low power boot options you must modify the vectors.h file to select the desired boot option. By default the 1st CONFIG_4 option is selected. To change simple comment out the first line and uncomment out the low power boot option you want.

```
-------------------------------------------------------------
#define CONFIG_4        (pointer*)0xfffffffe //b5=1,b4=1,b0=1 div1 fast
//#define CONFIG_4      (pointer*)0xfffff7fE //reset disabled div1 fast
//#define CONFIG_4      (pointer*)0xffffdffe //b5=0,b4=1,b0=1 div1 slow works
//#define CONFIG_4      (pointer*)0xffffcefe //b5=0,b4=0,b0=0;div8 slow
//#define CONFIG_4      (pointer*)0xffffeefe //b5=1,b4=0,b0=0 div8 fast
//#define CONFIG_4      (pointer*)0xffffcffe //b5=0,b4=0,b0=1;div4 slow
//#define CONFIG_4      (pointer*)0xffffeffe //b5=1,b4=0,b0=1;div4 fast
//#define CONFIG_4      (pointer*)0xfffffefe //b5=1,b4=1,b0=0;div2 fast
//#define CONFIG_4      (pointer*)0xffffdefe //b5=0,b4=1,b0=0;div2 slow
-------------------------------------------------------------------
```

Then configure the IAR IDE: By default, the IAR flash loader will ignore writes to the flash configuration field (0x40C-0x40F) in Kinetis flash devices. This prevents accidental securing of the device.

To write your own values to the flash configuration field, a simple parameter can be passed to the flash loader.

Step 1
Open the options window for your project which targets the flash.
Select Debugger … Download.
Click Edit…
Step 2
Select the first line.
Click Edit…
Step 3
In the Extra parameters: field, type “--enable_config_write”
Select OK to complete the edit
Select OK to close the option window.

The next time you download to the MCU the new LOW Power BOOT option will be used.

```
-----------------------------------------------------------------
*************   OPERATION DESCRIPTION:  ************************
-----------------------------------------------------------------
COMMAND DESCRIPTIONS: 0 through K
 > This is what is happening in these operations:
-----------------------------------------------------------------
-----------------------------------------------------------------


*****************************************************************
0 for CASE 0: Enter VLLS0 with POR disabled (Very Low Leakage STOP 0) NO POR
*****************************************************************
This is the lowest operational power mode of the MCU.  After a key press the MCU enters
VLLS0 - with the POR function disabled.  The Terminal output will look like this when in
the low power mode:
-------------------------------------------
Press any key to enter VLLS0 with POR disable
 Press SW4 to wake up from VLLS0
-------------------------------------------
After Wakeup the Terminal displays this:
-------------------------------------------

[outSRS]Wakeup bit set from low power mode VLLS0 exit
..... RESET BANNER ......
-------------------------------------------
NOTES:
Low voltage brown out: The VDD of the MCU is not monitored for brown out occurrences
since the POR comparator is disabled.

WAKEUP: the only wakeup sources are SW4 RESET and POWER OFF then ON. Normally the pin
input SW4, LLWU (Low Leakage Wakeup Unit) is used to wake up the MCU from this mode.

*****************************************************************
1 for CASE 1: Enter VLLS0 with POR enabled (Very Low Leakage STOP 0) with POR
*****************************************************************
This is the 2nd lowest operational power mode of the MCU.  After a key press the MCU
enters VLLS0 - with the POR function enabled.  The Terminal output will look like this
when in the low power mode:
-------------------------------------------
> 1
 > 0
Press any key to enter VLLS0 with POR disable
 Press SW4 to wake up from VLLS0
-------------------------------------------
After Wakeup the Terminal displays this:
-------------------------------------------
```

```
[outSRS]Wakeup bit set from low power mode VLLS0 exit
..... RESET BANNER ......
-------------------------------------------
NOTES:
Low voltage brown out: The VDD of the MCU is monitored for brown out occurrences since
the POR comparator is enabled.  If VDD falls below the POR limit a power on Reset will
occur.

WAKEUP: the only wakeup sources are SW4 RESET and POWER OFF then ON. Normally the pin
input SW4, LLWU (Low Leakage Wakeup Unit) is used to wake up the MCU from this mode.

*****************************************************************
2 for CASE 2: Enter VLLS1 (Very Low Leakage STOP 1)
*****************************************************************
This is the next lowest operational power mode of the MCU.  After a key press the MCU
enters VLLS1.  The Terminal output will look like this:
-------------------------------------------
> 2
Press any key to enter VLLS1
 Press SW4 to wake up from VLLS1
-------------------------------------------
After Wakeup the Terminal displays this:
-------------------------------------------
[outSRS]Wakeup bit set from low power mode VLLS1 exit
..... RESET BANNER ......
-------------------------------------------
NOTES:

WAKEUP: the wakeup sources are the LPTMR, SW4 RESET and POWER OFF then ON. Normally the
pin input SW4, LLWU (Low Leakage Wakeup Unit) is used to wake up the MCU from this mode.
Optionally the LPTMR can be used to wakeup up from the low power mode.  [See Operation G
and H]

*****************************************************************
3 for CASE 3: Enter LLS with LPTMR 1 second wakeup loop (Low Leakage Stop)
*****************************************************************
This is an operation testing the entry into LLS low power mode of the MCU.  After a key
press the MCU enters LLS then wakes up from the LPTMR every second for 10 times. The
Terminal output will look like this and then Select Operation Banner will display:
-------------------------------------------
 > 3
Press any key to enter LLS with LPTMR 1 Second wakeup loop

 LLWU configured modules as LLWU wakeup sources = 0x01,
 LPTMR Clock source is the LPOCLK
Press SW4 to wake up from VLLS2
   Entering LLS moVÚ11]UISR]
 [LLWU ISR] ****WUF3_MWUF0 IF  LPTMR  *****
```

```
            [demo_lptmr_isr]  Loop Count 0x00   Back in RUN mode
  Entering LLS moVÚ11]UISR]
.........
  Entering LLS moVÚ11]UISR]
 [LLWU ISR] ****WUF3_MWUF0 IF  LPTMR  *****
            [demo_lptmr_isr]  Loop Count 0x09   Back in RUN mode
  in Run Mode  !   in PEE mode now at 48000000 Hz

Select the desired operation
0 for ......
-------------------------------------------
CAUTION: Set J3 to 3-5 to operate the MCU at 1.8 VDC or this operation may fail.

WAKEUP:
Wake up from LLS is to the next instruction following the stop entry. The wakeup sources
are the LPTMR, SW4 RESET or POWER OFF then ON. Normally the LPTMR in conjunction with the
LLWU is used to wake up the MCU from this mode.Optionally the SW4 can be used to wakeup
up from the low power mode.

*************************************************************
4 for CASE 4: Enter VLLS3 (Very Low Leakage STOP 3)
*************************************************************
This is the next lowest power mode to VLLS1.  After a key press the MCU enters VLLS3.
The Terminal output will look like this
-------------------------------------------
 > 4
Press any key to enter VLLS3
 Press SW4 to wake up from VLLS3
-------------------------------------------
After Wakeup the Terminal displays this followed by the RESET BANNER:
-------------------------------------------
[outSRS]Wakeup bit set from low power mode VLLS3 exit
..... RESET BANNER ......
-------------------------------------------
NOTES:
Wakeup is through the MCU reset flow:

WAKEUP: the wakeup sources are the LPTMR, SW4 RESET and POWER OFF then ON. Normally the
pin input SW4, LLWU (Low Leakage Wakeup Unit) is used to wake up the MCU from this mode.
Optionally the LPTMR can be used to wakeup up from the low power mode.  [See Operation G
and H]

*************************************************************
5 for CASE 5: Enter LLS(Low Leakage Stop)
*************************************************************
This is the next lower power mode to VLLS3. After a key press the MCU enters LLS.  The
Terminal output will look like this.
-------------------------------------------
> 5
```

```
Press any key to enter LLS
 Press SW4 to wake up from LLS

-------------------------------------------
After Wakeup the Terminal displays this and then Select Operation Banner will display:
-------------------------------------------

  [LLWU ISR] ****WUF7 was set from PTC3 input  *****
  in Run Mode  !   in PEE mode now at 48000000 Hz

Select the desired operation
0 for ......
-------------------------------------------
CAUTION: Set J3 to 3-5 to operate the MCU at 1.8 VDC or this operation may fail.

WAKEUP:
Wake up from LLS is to the next instruction following the stop entry. The wakeup sources
are the LPTMR, SW4 RESET or POWER OFF then ON. Normally the LPTMR in conjunction with the
LLWU is used to wake up the MCU from this mode.Optionally the SW4 can be used to wakeup
up from the low power mode.

*************************************************************
6 for CASE 6: Enter VLPS(Very Low Power Stop)
*************************************************************
This is the next lower power mode to LLS. After a key press the MCU enters VLPS.  The
Terminal output will look like this.
-------------------------------------------
> 5
Press any key to enter VLPS
 Press SW3 to wake up from VLPS

-------------------------------------------
If entered from RUN mode - After wakeup the Terminal displays this and then Select
Operation Banner will display:
-------------------------------------------
  [porta_isr] porta4 ISF cleared
  in Run Mode  !
   in Run Mode  !   in PEE mode now at 48000000 Hz

Select the desired operation
0 for ......
-------------------------------------------
WAKEUP:
Wake up from VLPS is to the next instruction following the stop entry. The wakeup sources
are the LPTMR, SW3 RESET or POWER OFF then ON. Normally SW3 is used to wake up the MCU
from this mode. Optionally the LPTMR can be used to wakeup up from the low power mode.
[See Operation G and H]

*************************************************************
```

```
7 for CASE 7: Enter VLPR(Very Low Power RUN) in BLPE (8 MHz Crystal)
*****************************************************************
This is lowest code execution RUN mode available for the MCU.  After a key is pressed the
MCU enters VLPR mode and the Select Operation Banner will display.
-----------------------------------------------
 > 7
Press any key to enter VLPR
 Configure clock frequency to 4MHz core clock and 1MHz flash clock

 in PEE clock mode moving to BLPE clock mode

 Now moved to BLPE clock mode
  in VLPR Mode !
   in VLPR Mode !   in BLPE mode now at 8000000 Hz

Select the desired operation
0 for.........
-----------------------------------------------

*****************************************************************
8 for CASE 8: Exit VLPR(Very Low Power RUN)
*****************************************************************
Use this operation to exit VLPR mode back to RUN Mode.
After a key is pressed the MCU returns to RUN mode and the Select Operation Banner will
display.
NOTES:
If VLPR was entered from RUN mode with a clock BLPE mode, the exit VLPR operation returns
to RUN mode in the same BLPE clock MODE.
-----------------------------------------------
 > 8
Press any key to exit VLPR

 in BLPE mode
  in Run Mode  !
   in Run Mode  !   in BLPE mode now at 8000000 Hz

Select the desired operation
0 for........
-----------------------------------------------
If  VLPR is entered into in clock mode BLPI(see case 18 or 19), the exit VLPR operation
returns to RUN mode in FEI mode running 48 MHz
-----------------------------------------------
 > 8
Press any key to exit VLPR

 in BLPI mode with fast IRC
                              in Run Mode  !
   in Run Mode  !   in FEI mode now at 48000000 Hz
```

```
Select the desired operation
0 for ......
--------------------------------------------

*****************************************************************
9 for CASE 9: Enter VLPW(Very Low Power WAIT)
*****************************************************************
This operation will move the MCU into VLPW if you are already in VLPR.
This transition is independent of clock mode.
The entry into VLPW from VLPR will display:
--------------------------------------------
 > 9
Press any key to enter VLPW
 Press SW3 to wake up from VLPW
   in VLPR Mode moving to VLPW!
--------------------------------------------
Exit from VLPW back to VLPR is with an interrupt. After wakeup the MCU enters VLPR mode
and the Select Operation Banner will display.
--------------------------------------------

[porta_isr] porta4 ISF cleared
  in VLPR Mode !
   in VLPR Mode !  in BLPI mode now at 4000000 Hz

Select the desired operation
0 for CASE 0: ........
--------------------------------------------

*****************************************************************
A for CASE 10: Enter WAIT from RUN or VLPW from VLPR
*****************************************************************
This operation will transition the MCU into WAIT or VLPW mode depending on the RUN state
the MCU was in.  If in RUN mode the MCU enters WAIT.  If in VLPR the MCU enters VLPW.
The entry into WAIT or VLPW from RUN will display:
--------------------------------------------
 > a
Press any key to enter Wait
 Press SW3 to wake up from Wait

--------------------------------------------
Exit from WAIT back to RUN or VLPW to VLPR is with an interrupt. After wakeup the MCU re-
enters RUN or VLPR mode and the Select Operation Banner will display.
--------------------------------------------
[porta_isr] porta4 ISF cleared
  in Run Mode  !
   in Run Mode  !   in PEE mode now at 48000000 Hz

Select the desired operation
0 for CASE 0: ........
```

```
----------------------OR ----------------------
[porta_isr] porta4 ISF cleared
  in VLPR Mode !
   in VLPR Mode !   in BLPE mode now at 4000000 Hz

Select the desired operation
0 for CASE 0: ........
*****************************************************************
B for CASE 11: Enter Normal STOP from RUN or VLPS from VLPR
*****************************************************************
This operation will transition the MCU into STOP or VLPS mode depending on the RUN status
the MCU was in.  If transition from RUN the MCU enters Normal STOP.  If transitioning
from VLPR the MCU enter VLPS.
The entry into STOP from RUN will display:
-----------------------------------------------
> 6
Press any key to enter VLPS
 Press SW3 to wake up from VLPS
-----------------------------------------------
Exit from STOP back to RUN or VLPS to VLPR is with an interrupt. After wakeup the MCU re-
enters RUN or VLPR mode and the Select Operation Banner will display.
-----------------------------------------------
[porta_isr] porta4 ISF cleared
  in Run Mode  !
   in Run Mode  !   in PEE mode now at 48000000 Hz

Select the desired operation
0 for CASE 0: ........
------------------------OR----------------------
[porta_isr] porta4 ISF cleared
  in VLPR Mode !
   in VLPR Mode !   in BLPE mode now at 4000000 Hz

Select the desired operation
0 for CASE 0: ........
-----------------------------------------------
*****************************************************************
C for CASE 12: Enter PARTIAL STOP 1 with both system and bus clocks disabled
*****************************************************************
Partial STOP 1 is a new clock mode that stops both the system and bus clocks.
The current is lower than WAIT mode but much higher than Normal STOP mode. Exit is
accomplished with an interrupt and will return to the RUN state the MCU was in before
entering PARTIAL STOP.
For this operation the MCU enters PARTIAL STOP 1 and shows the following display:
-----------------------------------------------
 > c
Press any key to enter Stop PSTOP1
 Press SW3 to wake up from Stop PSTOP1
```

```
---------------------------------------------
Exit from PARTIAL STOP back to RUN or VLPR is with an interrupt. After wakeup the MCU re-
enters RUN or VLPR mode and the Select Operation Banner will display.
---------------------------------------------

[porta_isr] porta4 ISF cleared
  in Run Mode  !
   in Run Mode  !   in PEE mode now at 48000000 Hz

Select the desired operation
0 for CASE 0: ........
---------------------------------------------

*************************************************************
D for CASE 13: Enter PARTIAL STOP 2 with system clock disabled and bus clock enabled
*************************************************************
Partial STOP 2 is a new clock mode that stops the system but keeps the bus clock enabled.
The current is lower than WAIT mode but much higher than Normal STOP mode. Exit is
accomplished with an interrupt and will return to the RUN state the MCU was in before
entering PARTIAL STOP.
For this operation the MCU enters PARTIAL STOP 2 and shows the following display:
---------------------------------------------
 > d
Press any key to enter Stop PSTOP2
 Press SW3 to wake up from Stop PSTOP2

---------------------------------------------
Exit from PARTIAL STOP back to RUN or VLPR is with an interrupt. After wakeup the MCU re-
enters RUN or VLPR mode and the Select Operation Banner will display.
---------------------------------------------

[porta_isr] porta4 ISF cleared
  in Run Mode  !
   in Run Mode  !   in PEE mode now at 48000000 Hz

Select the desired operation
0 for CASE 0: ........
---------------------------------------------

*************************************************************
E for CASE 14: Running coremark 2 times in RUN  with CPO then without CPO
*************************************************************
In order to measure the performance and power of the MCU while performing certain tasks
these operations are included.  There is a new mode of operation in this MCU called CPO
(Computer Only Mode) where the clocks to everything except the core modules is gated off.
This places all the not needed circuitry in a static state greatly reducing the power
need of the MCU.
```

This operation runs 400 iterations of the COREMARK test 2 times in CPO mode with the peripherals clock gated off. Then the operations re-runs 400 iterations of the COREMARK test 2 times in normal RUN mode with all the enabled modules clocking.
Since the UART is one of those peripherals placed in static state.

During this operations the MCU starts from RUN mode. The following is shown and then the Select Operation Banner will display:

```
-----------------------------------------------
 > e
To exit either hit RESET button or wait for loop to complete
Transitioning from RUN mode
Start CoreMark in Compute Only (CPO) Mode -->
  Now running Coremark without CPO mode enabled.
Coremark iterations = 0x00 of 2
Start CoreMark in Compute Only (CPO) Mode -->
  Now running Coremark without CPO mode enabled.
Coremark iterations = 0x01 of 2
  in Run Mode  !   in PEE mode now at 48000000 Hz

Select the desired operation
0 for CASE 0:........

-----------------------------------------------

*****************************************************************
F for CASE 15: Running coremark 2 times in VLPR with CPO then without CPO
*****************************************************************
```

In order to measure the performance and power of the MCU while performing certain tasks these operations are included. There is a new mode of operation in this MCU called CPO (Computer Only Mode) where the clocks to everything except the core modules is gated off. This places all the not needed circuitry in a static state greatly reducing the power need of the MCU.
This operation runs 400 iterations of the COREMARK test 2 times in CPO mode with the peripherals clock gated off. Then the operations re-runs 400 iterations of the COREMARK test 2 times in normal RUN mode with all the enabled modules clocking.
Since the UART is one of those peripherals placed in static state.

During this operations the MCU starts from VLPR mode. There are three clock mode options for VLPR a) BLPE at 4 MHz b) BLPI at 4 MHz and 3) BLPI at 2 MHz. (Note: this may take longer to complete than in run mode since the core clock is only at 2 or 4 MHz instead of 48 MHz)

The following is shown and then the Select Operation Banner will display:

```
-----------------------------------------------
 > f
  in VLPR Mode !
   in VLPR Mode !  in BLPI mode now at 2000000 Hz

Transitioning from VLPR mode
```

```
Starting running Coremark in VLPR with--- CPO mode enabled.
-in VLPR mode
Starting running Coremark in VLPR without CPO mode enabled.
Coremark iterations = 0x00 of 2
Starting running Coremark in VLPR with--- CPO mode enabled.
-in VLPR mode
Starting running Coremark in VLPR without CPO mode enabled.
Coremark iterations = 0x01 of 2
  in VLPR Mode !  in BLPI mode now at 2000000 Hz

Select the desired operation
0 for CASE 0:........
---------------------------------------------

  > f
  in RUN Mode moving to VLPR
 Press any key to enter VLPR
 Configure clock frequency to 4MHz core clock and 1MHz flash clock
 In RUN Mode !

 in PEE clock mode moving to BLPE clock mode

 Now moved to BLPE clock mode
  in VLPR Mode !
   in VLPR Mode !   in BLPE mode now at 4000000 Hz

Transitioning from VLPR mode
Starting running Coremark in VLPR with--- CPO mode enabled.
     Back in VLPR mode
Starting running Coremark in VLPR without CPO mode enabled.
Coremark iterations = 0x00 of 2
Starting running Coremark in VLPR with--- CPO mode enabled.
     Back in VLPR mode
Starting running Coremark in VLPR without CPO mode enabled.
Coremark iterations = 0x01 of 2
  in VLPR Mode !   in BLPE mode now at 4000000 Hz

Select the desired operation
0 for CASE 0:........
---------------------------------------------


*****************************************************************
G for CASE 16: Enable LPTMR to wake up every 5 seconds from any mode except VLLS0
*****************************************************************
This operation allows you to use the LPTMR to cause and interrupt and an LLWU event about
every 5 seconds.  This will wake the MCU from any of the low power modes that the LPTMR
can work in.  This excludes VLLS0 mode since the LPTMR is clocked by the LPO (Low power
oscillator) which is off in VLLS0.
```

If you select g then the following is shown and then the Select Operation Banner will display:

```
-------------------------------------------

 > g

 LLWU configured modules as LLWU wakeup sources = 0x01,
 LPTMR Clock source is the LPOCLK
  in ........
-------------------------------------------
```

```
*****************************************************************
H for CASE 17: Disable LPTMR wakeup
*****************************************************************
```

This operations turns off the LPTMR thus disabling the interrupt and wake up event possibilities using the LPTMR.

If you select h then the following is shown and then the Select Operation Banner will display:

```
-------------------------------------------

 > h

  Disabled LPTMR
  in ........
-------------------------------------------
```

```
*****************************************************************
I for CASE 18: Enter VLPR in BLPI at Core Frequency of 4 MHz
*****************************************************************
```

This operation enters VLPR in the clock mode BLPI (Bypass Low Power Internal). The BLPI mode uses the 4 MHz fast internal reference to clock the MCU. The flash clock is set to the maximum 1 MHz clock.

If you select i then press any key the following is shown and then the Select Operation Banner will display:

```
-------------------------------------------

 > i
Press any key to enter VLPR in BLPI mode
 Configure clock frequency to 4MHz core clock and 1MHz flash clock
 In RUN Mode !

 Now moved to BLPI clock mode
  in VLPR Mode !
   in VLPR Mode !  in BLPI mode now at 4000000 Hz

Select the desired operation
```

```
0 for CASE 0:........
-------------------------------------------

*****************************************************************
J for CASE 19: Enter VLPR in BLPI at Core Frequency of 2 MHz
*****************************************************************
This operation enters VLPR in the clock mode BLPI (Bypass Low Power Internal). The BLPI
mode uses the 4 MHz fast internal reference divide by 2 to clock the MCU. The flash clock
is set to the maximum 1 MHz clock.

If you select j then press any key the following is shown and then the Select Operation
Banner will display:
-------------------------------------------

 > j
Press any key to enter VLPR
 Configure clock frequency to 2MHz core clock and 1MHz flash clock
 In RUN Mode !

 in BLPI mode with fast IRC
  in VLPR Mode !
   in VLPR Mode !  in BLPI mode now at 2000000 Hz

Select the desired operation
0 for CASE 0:........
-------------------------------------------
*****************************************************************
K for CASE 20: Enter Compute Mode run for(i=0;i<wait_count;i++)
*****************************************************************
This operation enters CPO (Compute Only Mode) and stays in a for loop for the loop count.
The loop count depends on whether the MCU is in RUN or VLPR mode.

If you enter this operation from VLPR mode the following is shown and then the Select
Operation Banner will display:
-------------------------------------------
 > k
Press any key to enter VLPR
 Configure clock frequency to 2MHz core clock and 1MHz flash clock
 In RUN Mode !

 in BLPI mode with fast IRC
  in VLPR Mode !
   in VLPR Mode !  in BLPI mode now at 2000000 Hz

Select the desired operation
0 for CASE 0:........-
-------------------------------------------
If you enter this operation from RUN mode the following is shown and then the Select
Operation Banner will display:
```

```
-----------------------------------------------
 > k
  in Run Mode  !   in FEI mode now at 48000000 Hz
Start Compute Mode --> waiting for 200000000 counts
Waiting is Over - Now OUT of Compute Mode
   in Run Mode  !   in FEI mode now at 48000000 Hz

Select the desired operation
0 for CASE 0:.......-
-----------------------------------------------
*************************************************************
L for CASE 21: To enable DEBUG
*************************************************************
This operation writes the pin mux controls to enable an External debugger to access the
SWD functions of the MCU. The code turns off the debug interface during initialization.
This re-enables debug to be possible.

Note: Enabling debug may have an effect on your power measurements in some low power
modes.

If you enter this operation the following is shown and then the Select Operation Banner
will display:
-----------------------------------------------
 > l

*-------------D E B U G    E N A B L E D--------------------*
   in Run Mode  !   in PEE mode now at 48000000 Hz

Select the desired operation
0 for CASE 0:.......-
-----------------------------------------------
```