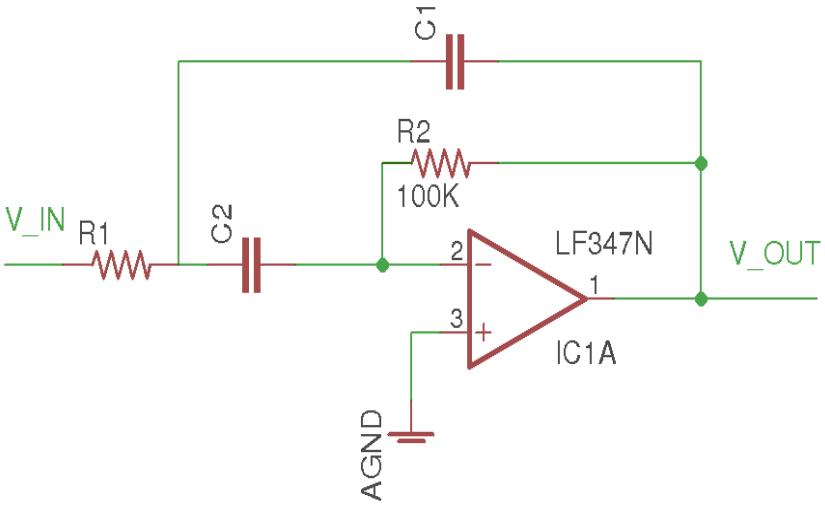
EECS192 Lecture 2
Jan. 28, 2020

- Checkoff 2/1: Hello World/LED Blink/Switch
- Checkoff 2/8: Benchtop motor and steering (using provided PCB)
- Project proposal (due 2/11 before class)
  - Documentation
  - Block Diagram/Software Model
- Cloud 9 quick demo
- LED/Port Information
- PWM Intro
- Motor Model

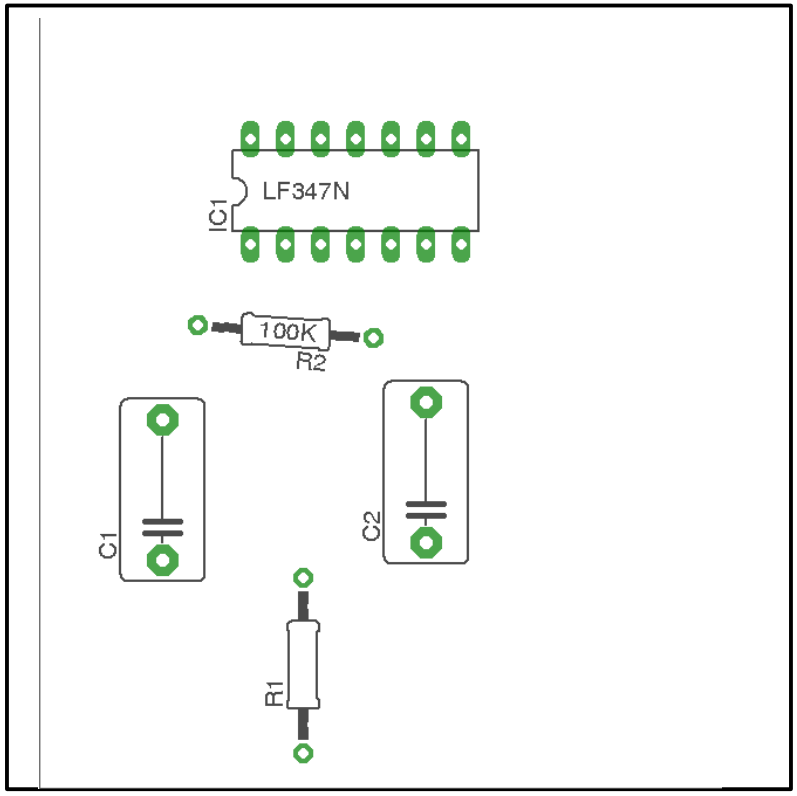
Notes:
Check off- Hello World+LED blink+switch
``look don't touch''
Github repo

Project Proposal: Documentation



Eagle: File → export → image (300 dpi png)

Eagle parts layout- no copper



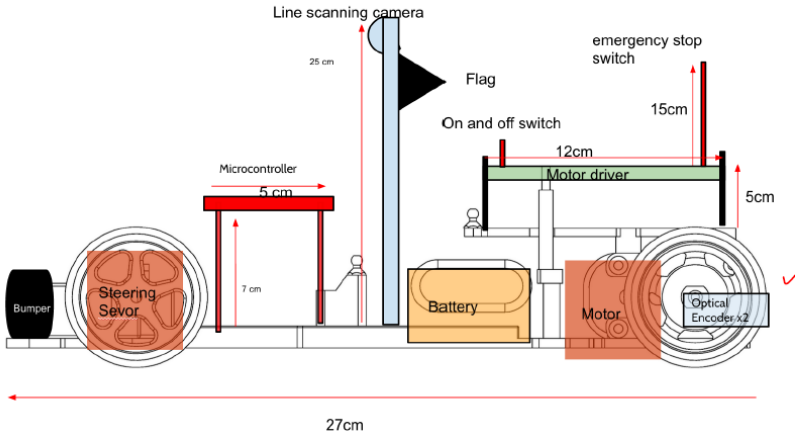
Black: tNames, tValues, tPlace
White or off: tOrigins, Unrouted

KiCad EDA
https://kicad-pcb.org/

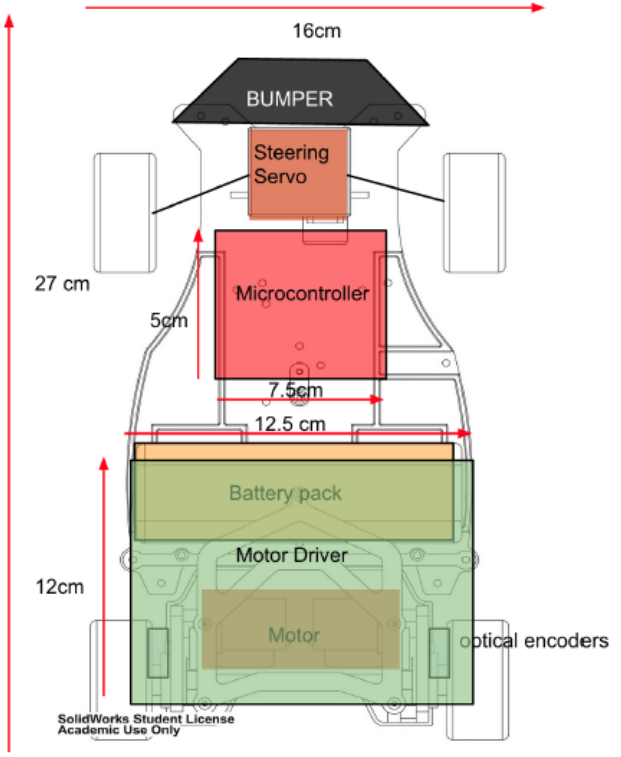
Project Proposal: Documentation

2. Detailed Mechanical Drawing of Vehicle

a. Side view of vehicle

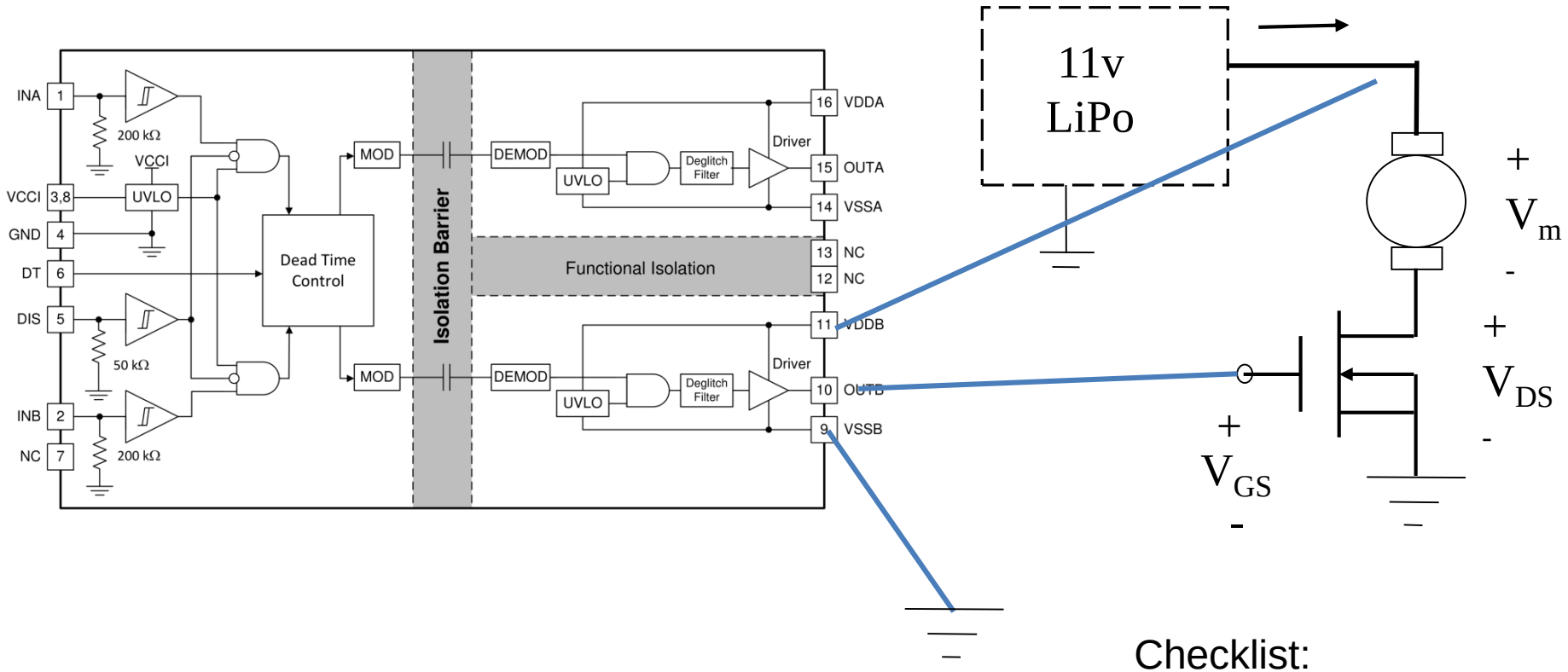


b. Top view of vechicle



c. Include a labelled photo which indicates good lo

Project Proposal:
Motor Drive with UCC21222 gate driver



Details On board….

Checklist:

1) Emergency stop
2) Reset Protection
3) Snubbing

UCC21222 pin functions- E-stop

PIN		I/O (1)	Description
NAME	NO.		
DIS	5	I	Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈ 1-nF low ESR/ESL capacitor close to DIS pin when connecting to a µC with distance.
DT	6	I	Programmable dead time function. Tying DT to VCCI or leaving DT open allows the outputs to overlap. Placing a resistor (R_{DT}) between DT and GND adjusts dead time according to the equation: DT (in ns) = 10 × R_{DT} (in kΩ). TI recommends bypassing this pin with a ceramic capacitor, 2.2 nF or greater, to achieve better noise immunity. Place this capacitor and R_{DT} close to the DT pin.
GND	4	P	Primary-side ground reference. All signals in the primary side are referenced to this ground.
INA	1	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
INB	2	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
NC	7	-	No internal connection.
	12		
	13		
OUTA	15	O	Output of driver A. Connect to the gate of the A channel FET or IGBT.
OUTB	10	O	Output of driver B. Connect to the gate of the B channel FET or IGBT.
VCCI	3	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
VCCI	8	P	This pin is internally shorted to pin 3.
VDDA	16	P	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.
VDDB	11	P	Secondary-side power for driver B. Locally decoupled to VSSB using a low ESR/ESL capacitor located as close to the device as possible.
VSSA	14	P	Ground for secondary-side driver A. Ground reference for secondary side A channel.
VSSB	9	P	Ground for secondary-side driver B. Ground reference for secondary side B channel.

(1) P = power, I = input, O = output

Project Proposal: Input/Output

Line camera: 128 pixels, 200 Hz

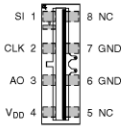
TAOS TEXAS ADVANCED OPTOELECTRONIC SOLUTIONS®

TSL1401CL
128 × 1 LINEAR SENSOR ARRAY WITH HOLD

TAOS136 – JULY 2011

- 128 × 1 Sensor-Element Organization
- 400 Dots-Per-Inch (DPI) Sensor Pitch
- High Linearity and Uniformity
- Wide Dynamic Range . . . 4000:1 (72 dB)
- Output Referenced to Ground
- Low Image Lag . . . 0.5% Typ
- Operation to 8 MHz
- Single 3-V to 5-V Supply
- Rail-to-Rail Output Swing (AO)
- No External Load Resistor Required
- Replacement for TSL1401R–LF
- RoHS Compliant

CL PACKAGE
(TOP VIEW)



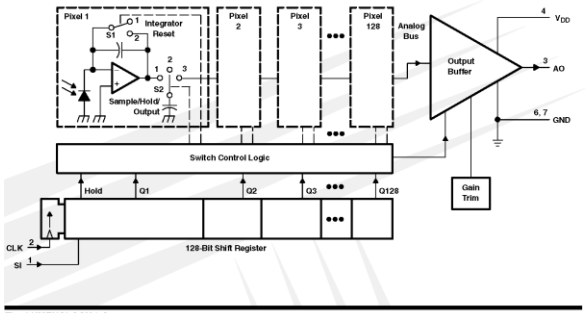
NC – No internal connection

Package Drawing is Not to Scale

Description

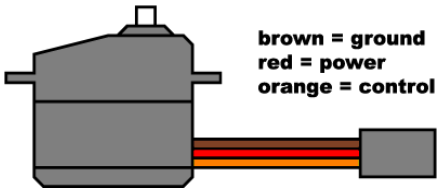
The TSL1401CL linear sensor array consists of a 128 × 1 array of photodiodes, associated charge amplifier circuitry, and an internal pixel data-hold function that provides simultaneous-integration start and stop times for all pixels. The array is made up of 128 pixels, each of which has a photo-sensitive area of 3,524.3 square micrometers. There is 8-µm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

Functional Block Diagram



The *LUMENOLOGY* ® Company

Texas Advanced Optoelectronic Solutions Inc.
1001 Klein Road • Suite 300 • Plano, TX 75074 • (972) 673-0759
www.taosinc.com



USB Camera: 320x240 (30 Hz?)

TEXAS INSTRUMENTS

UCC21222

SLUSCX6A – FEBRUARY 2018 – REVISED APRIL 2018

UCC21222 4-A, 6-A, 3.0-kV$_{RMS}$ Isolated Dual-Channel Gate Driver with Dead Time

1 Features

- Resistor-Programmable Dead Time
- Universal: Dual Low-Side, Dual High-Side or Half-Bridge Driver
- 4-A Peak Source, 6-A Peak Sink Output
- 3-V to 5.5-V Input VCCI Range
- Up to 18-V VDD Output Drive Supply
  - 8-V VDD UVLO
- Switching Parameters:
  - 28-ns Typical Propagation Delay
  - 10-ns Minimum Pulse Width
  - 5-ns Maximum Delay Matching
  - 5.5-ns Maximum Pulse-Width Distortion
- TTL and CMOS Compatible Inputs
- Integrated Deglitch Filter
- I/Os withstand –2-V for 200 ns
- Common-Mode Transient Immunity (CMTI) Greater than 100-V/ns
- Isolation Barrier Life >40 Years
- Surge Immunity up to 7800-V$_{PK}$
- Narrow Body SOIC-16 (D) Package
- Safety-Related Certifications (Planned):
  - 4242-V$_{PK}$ Isolation per DIN V VDE V 0884-11:2017-01 and DIN EN 61010-1
  - 3000-V$_{RMS}$ Isolation for 1 Minute per UL 1577
  - CSA Certification per IEC 60950-1, IEC 62368-1 and IEC 61010-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011
- Create a Custom Design Using the UCC21222 With the WEBENCH® Power Designer

2 Applications

- Isolated converters in AC-to-DC and DC-to-DC Power Supplies
- Server, Telecom, IT and Industrial Infrastructures
- Motor Drives and Solar Inverters
- HEV and EV Battery Chargers
- Industrial Transportation
- Uninterruptible Power Supply (UPS)

3 Description

The UCC21222 device is an isolated dual channel gate driver with programmable dead time. It is designed with 4-A peak-source and 6-A peak-sink current to drive power MOSFET, IGBT, and GaN transistors.

The UCC21222 device can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. 5ns delay matching performance allows two outputs to be paralleled, doubling the drive strength for heavy load conditions without risk of internal shoot-through.

The input side is isolated from the two output drivers by a 3.0-kV$_{RMS}$ isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI).

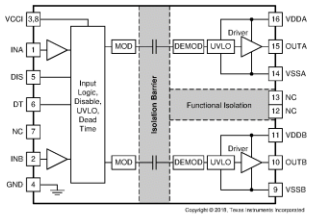
Resistor programmable dead time gives the capability to adjust dead time for system constraints to improve efficiency and prevent output overlap. Other protection features include: Disable feature to shut down both outputs simultaneously when DIS is set high, integrated deglitch filter that rejects input transients shorter than 5-ns, and negative voltage handling for up to -2-V spikes for 200-ns on input and output pins. All supplies have UVLO protection.

Device Information(1)

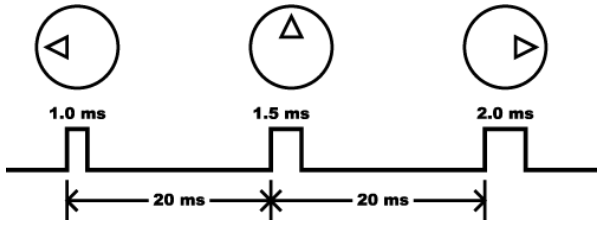
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC21222	SOIC (16)	9.9 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram

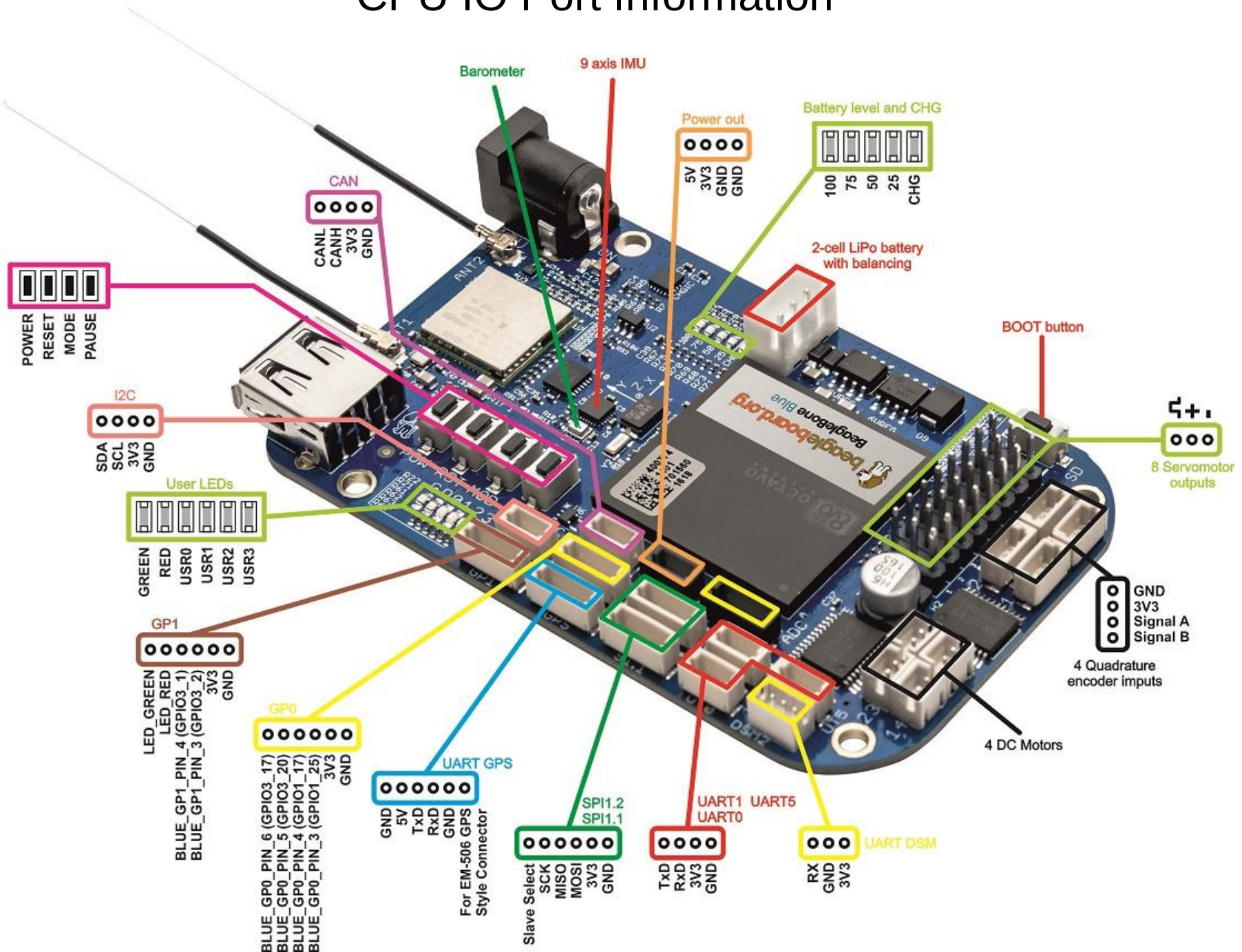


An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.



https://www.sparkfun.com/tutorials/283

CPU IO Port Information



Beagle Bone Blue Pins

http://inst.eecs.berkeley.edu/~ee192/sp20/files/BeagleBone_Blue_Pin_Table.xlsx

AutoSave Off — BeagleBone_Blue_Pin_Table.xlsx - Excel — Ronald FEARING

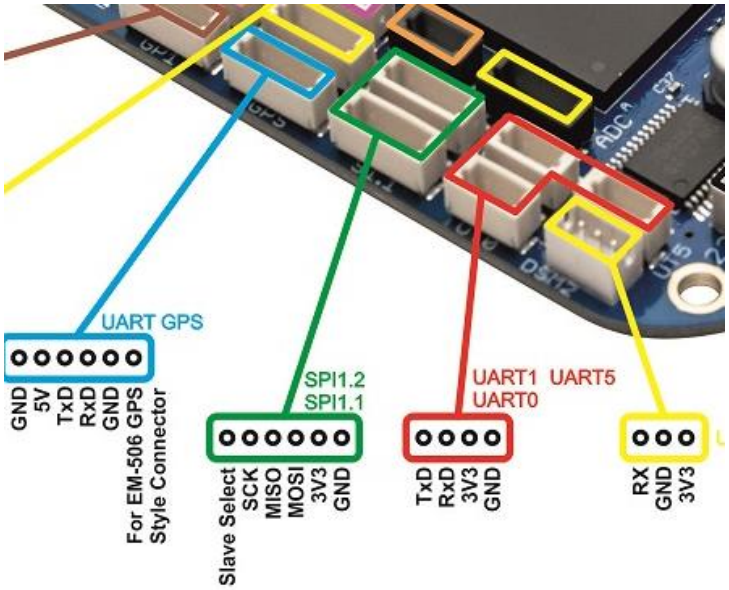
File Home Insert Page Layout Formulas Data Review View Help Search Share

E46 | UART2_RXD

	A	B	C	D	E	G	H	I	J	K	L	M	N
1	Use on Blue	Use on RC	config-pin name	Ball	Blue Name	MODE0	MODE1	MODE2	MODE3	MODE4	MODE5	MODE6	MODE7
70													
71	SPI: SS1, SS2												
72	SPI1_SCK	SPI1_SCK	P9.31	A13	SPI1_SCLK	mcasp0_aclkx	ehrpwm0A		spi1_sclk	mmc0_sdcd_mux1	pr1_pru0_pru_r30_0	pr1_pru0_pru_r31_0	gpio3[14]
73	SPI1_MISO	SPI1_MISO	P9.29	B13	SPI1_D0	mcasp0_fsx	ehrpwm0B		spi1_d0	mmc1_sdcd_mux1	pr1_pru0_pru_r30_1	pr1_pru0_pru_r31_1	gpio3[15]
74	SPI1_MOSI	SPI1_MOSI	P9.30	D12	SPI1_D1	mcasp0_axr0	ehrpwm0_tripzone		spi1_d1	mmc2_sdcd_mux1	pr1_pru0_pru_r30_2	pr1_pru0_pru_r31_2	gpio3[16]
75	SPI1_SS2 (BBBlue)			C18	spi1_cs1	eCAP0_in_PWM0_out	uart3_txd	spi1_cs1	pr1_ecap0_ecap_cap	spi1_sclk	mmc0_sdwp	xdma_event_intr2	gpio0_7
76	SPI1_SS1 (BBBlue)			H18	spi1_cs0	rmii1_refclk	xdma_event_i	spi1_cs0	uart5_txd	mcasp1_axr3	mmc0_pow	mcasp1_ahclkx	gpio0_29
77													

BeagleBone_Blue_Pin_Table | BBB-By connector | BBBlackEquiv

Display Settings



Robot Control Library

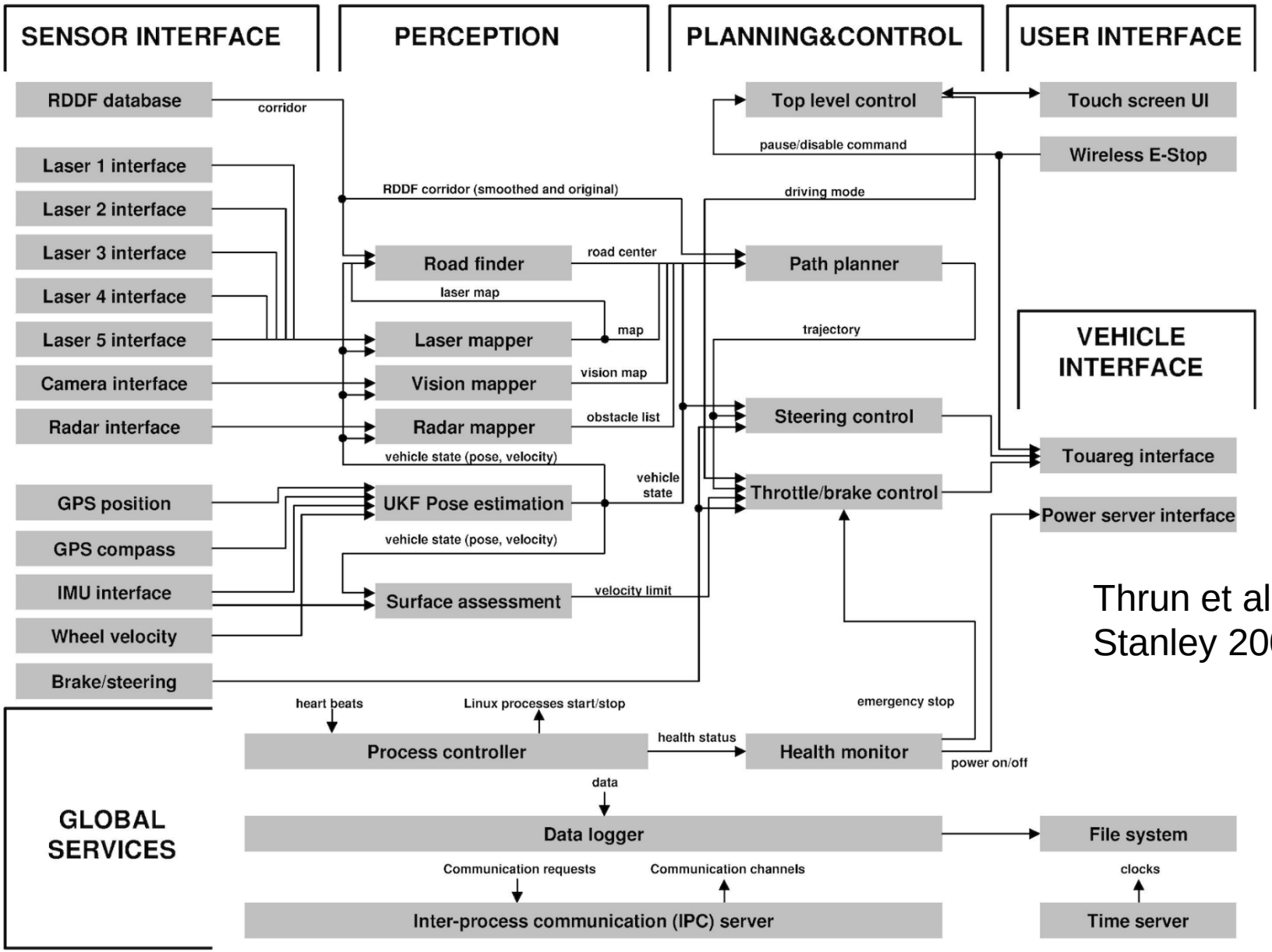
C interface for the Sitara PWM driver.

<rc/pwm.h>

These functions provide a general interface to all 3 PWM subsystems, each of which have two available channels A and B. PWM subsystems 1 and 2 are used for controlling the 4 motor drivers on the Robotics Cape, however they may be controlled by the user directly instead of using the motor API.

PWM subsystem 0 channels A and B can be accessed on the GPS or SPI header if set up with the Pinmux API to do so. The user may have exclusive use of that subsystem.

Project Proposal: Block Diagram/Software Model



Thrun et al
Stanley 2005

Project Proposal: Timing and priority of processes

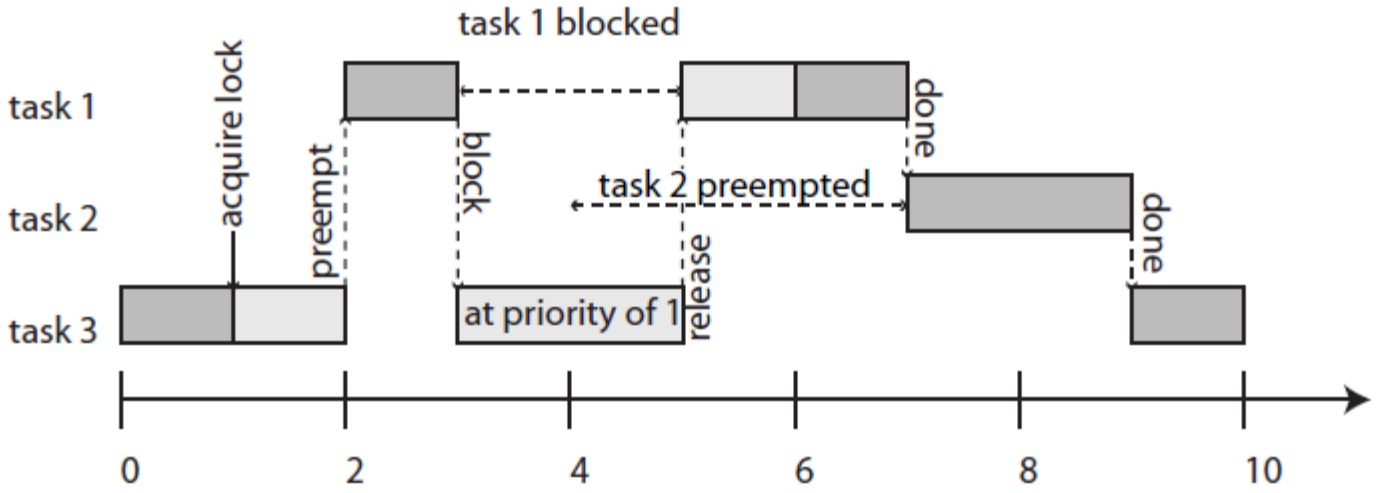


Figure 12.10: Illustration of the priority inheritance protocol. Task 1 has highest priority, task 3 lowest. Task 3 acquires a lock on a shared object, entering a critical section. It gets preempted by task 1, which then tries to acquire the lock and blocks. Task 3 inherits the priority of task 1, preventing preemption by task 2.

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Notes:
Check off- Hello World+LED blink+switch
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LED & CPU Port Information

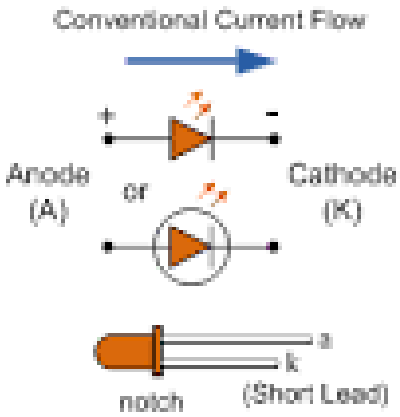
1.3 ESD handling ratings

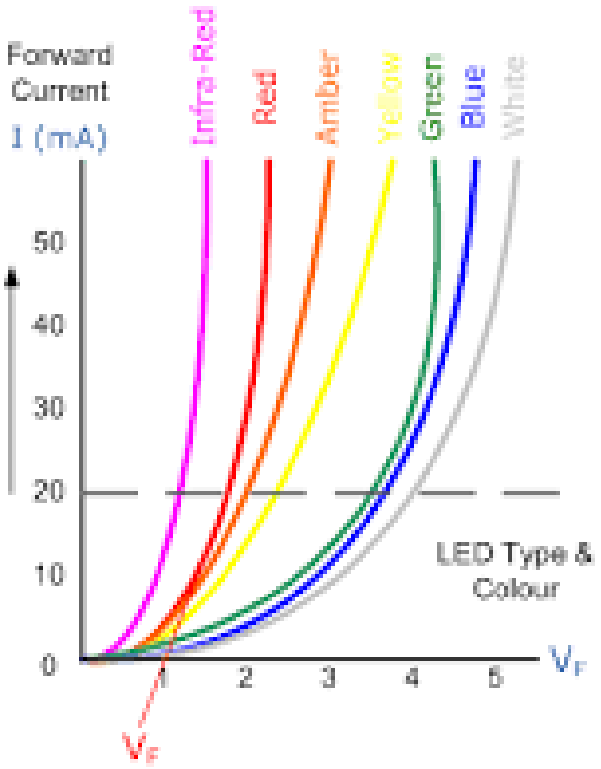
Table 3. ESD handling ratings

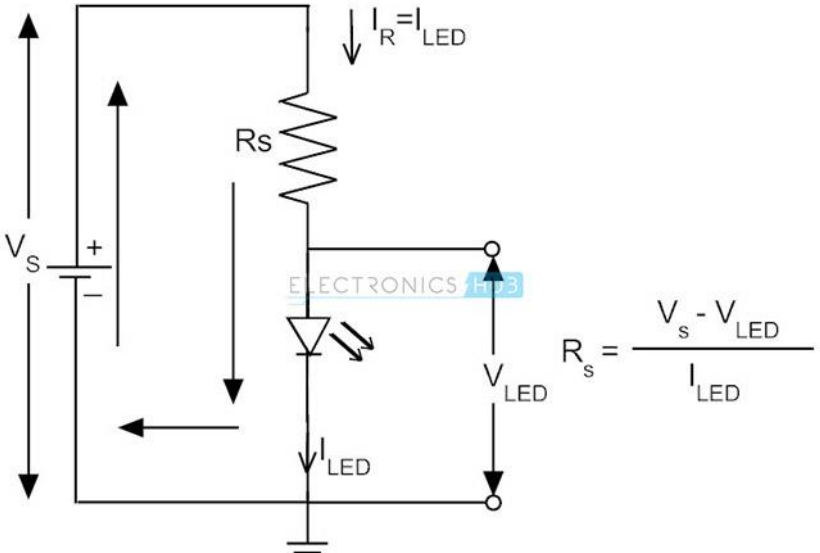
Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

Connecting LED & CPU Port Information







https://www.electronicshub.org/light-emitting-diode-basics/

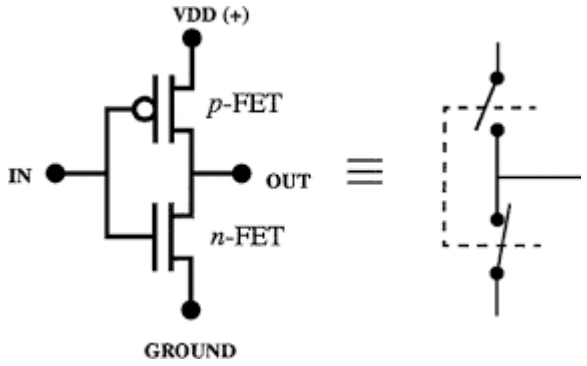
LED & CPU Port Information- typical

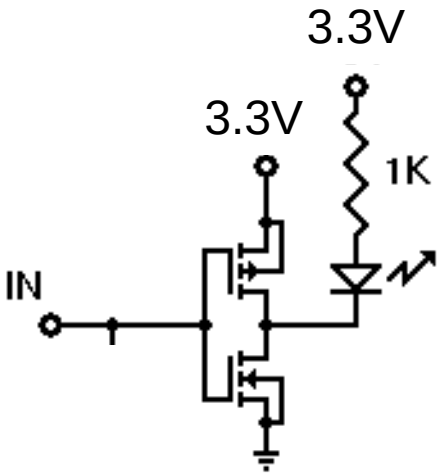
1.4 Voltage and current operating ratings

LATCHUP!

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	1[illegible]	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V
V_{REGIN}	USB regulator input	–0.3	6.0	V





LED & CPU Port Information- Am3359

5.7 DC Electrical Characteristics

over recommended ranges of supply voltage and operating temperature (unless otherwise noted)[(1)]

PARAMETER			MIN	NOM	MAX	UNIT
DDR_RESETn,DDR_CSn0,DDR_CKE,DDR_CK,DDR_CKn,DDR_CASn,DDR_RASn,DDR_WEn,DDR_BA0,DDR_BA1,DDR_BA2,DDR_A0,DDR_A1,DDR_A2,DDR_A3,DDR_A4,DDR_A5,DDR_A6,DDR_A7,DDR_A8,DDR_A9,DDR_A10,DDR_A11,DDR_A12,DDR_A13,DDR_A14,DDR_A15,DDR_ODT,DDR_D0,DDR_D1,DDR_D2,DDR_D3,DDR_D4,DDR_D5,DDR_D6,DDR_D7,DDR_D8,DDR_D9,DDR_D10,DDR_D11,DDR_D12,DDR_D13,DDR_D14,DDR_D15,DDR_DQM0,DDR_DQM1,DDR_DQS0,DDR_DQSn0,DDR_DQS1,DDR_DQSn1 Pins (mDDR - LVCMOS Mode)						
V_{IH}	High-level input voltage		0.65 × VDDS_DDR			V
V_{IL}	Low-level input voltage				0.35 × VDDS_DDR	V
V_{HYS}	Hysteresis voltage at an input		0.07		0.25	V
V_{OH}	High level output voltage, driver enabled, pullup or pulldown disabled	I_{OH} = 8 mA	VDDS_DDR – 0.4			V
V_{OL}	Low level output voltage, driver enabled, pullup or pulldown disabled	I_{OL} = 8 mA			0.4	V
I_I	Input leakage current, Receiver disabled, pullup or pulldown inhibited				10	µA
	Input leakage current, Receiver disabled, pullup enabled		–240		–80	
	Input leakage current, Receiver disabled, pulldown enabled		80		240	
I_{OZ}	Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.				10	µA

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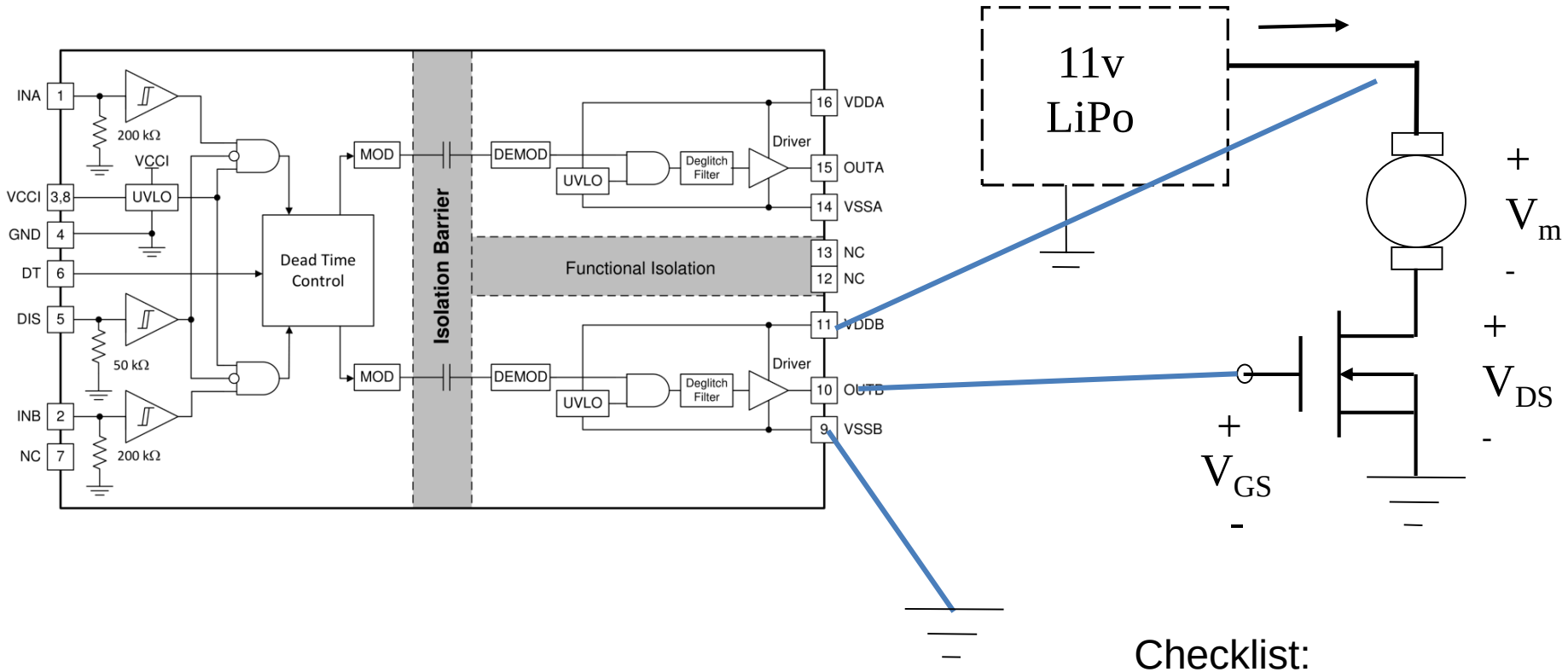

Details On board….

Checklist:

1) Emergency stop
2) Reset Protection
3) Snubbing

PWM and Timer Intro: PWM Generation

Functional description

FTM counting is up.
Channel (n) is in high-true EPWM mode.

PS[2:0] = 001
CNTIN = 0x0000
MOD = 0x0004
CnV = 0x0002

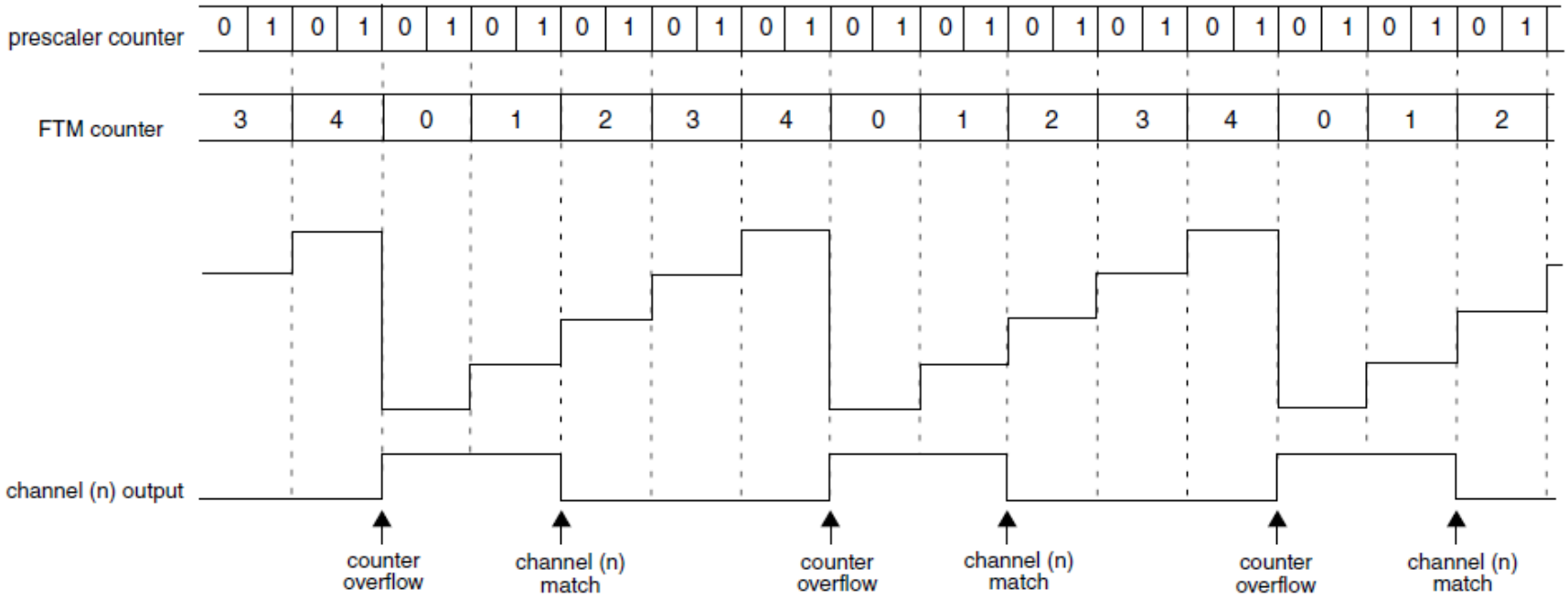

Figure 40-2. Notation used

Beagle Bone Blue Pins

http://inst.eecs.berkeley.edu/~ee192/sp20/files/BeagleBone_Blue_Pin_Table.xlsx

AutoSave Off — BeagleBone_Blue_Pin_Table.xlsx - Excel — Ronald FEARING

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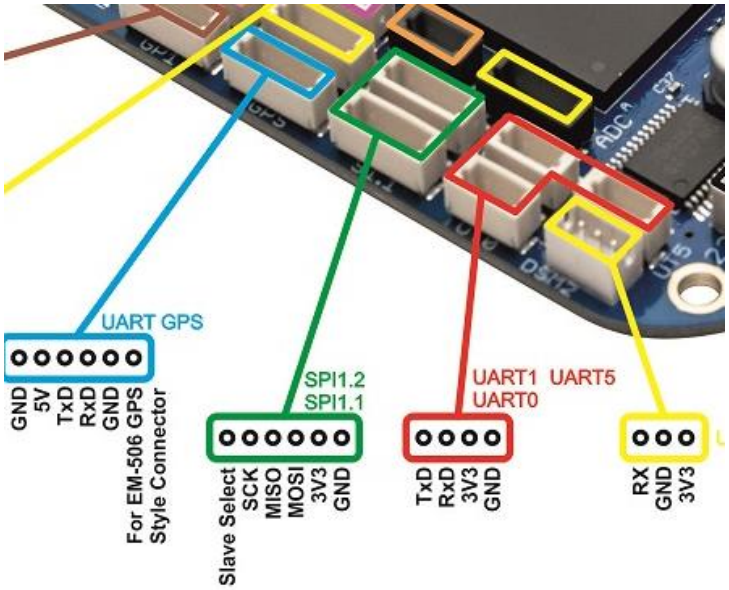
E46 | UART2_RXD

	A	B	C	D	E	G	H	I	J	K	L	M	N
1	Use on Blue	Use on RC	config-pin name	Ball	Blue Name	MODE0	MODE1	MODE2	MODE3	MODE4	MODE5	MODE6	MODE7
70													
71	SPI: SS1, SS2												
72	SPI1_SCK	SPI1_SCK	P9.31	A13	SPI1_SCLK	mcasp0_aclkx	ehrpwm0A		spi1_sclk	mmc0_sdcd_mux1	pr1_pru0_pru_r30_0	pr1_pru0_pru_r31_0	gpio3[14]
73	SPI1_MISO	SPI1_MISO	P9.29	B13	SPI1_D0	mcasp0_fsx	ehrpwm0B		spi1_d0	mmc1_sdcd_mux1	pr1_pru0_pru_r30_1	pr1_pru0_pru_r31_1	gpio3[15]
74	SPI1_MOSI	SPI1_MOSI	P9.30	D12	SPI1_D1	mcasp0_axr0	ehrpwm0_tripzone		spi1_d1	mmc2_sdcd_mux1	pr1_pru0_pru_r30_2	pr1_pru0_pru_r31_2	gpio3[16]
75	SPI1_SS2 (BBBlue)			C18	spi1_cs1	eCAP0_in_PWM0_out	uart3_txd	spi1_cs1	pr1_ecap0_ecap_cap	spi1_sclk	mmc0_sdwp	xdma_event_intr2	gpio0_7
76	SPI1_SS1 (BBBlue)			H18	spi1_cs0	rmii1_refclk	xdma_event_i	spi1_cs0	uart5_txd	mcasp1_axr3	mmc0_pow	mcasp1_ahclkx	gpio0_29
77													

BeagleBone_Blue_Pin_Table | BBB-By connector | BBBlackEquiv

Display Settings



Robot Control Library

C interface for the Sitara PWM driver.

<rc/pwm.h>

These functions provide a general interface to all 3 PWM subsystems, each of which have two available channels A and B. PWM subsystems 1 and 2 are used for controlling the 4 motor drivers on the Robotics Cape, however they may be controlled by the user directly instead of using the motor API.

PWM subsystem 0 channels A and B can be accessed on the GPS or SPI header if set up with the Pinmux API to do so. The user may have exclusive use of that subsystem.

PWM and Timer Intro: Code

http://strawsondesign.com/docs/librobotcontrol/group

```
int rc_pwm_set_duty     (       int  ss,
                                char    ch,
                                double  duty )
```

Sets the duty cycle of a specific pwm channel.

Parameters

[in]	ss	subsystem 0,1,2
[in]	ch	channel 'A' or 'B'
[in]	duty	between 0.0 (off) and 1.0(full on)

Direction???

PWM subsystem 0 channels A and B can be accessed on the GPS or SPI header if set up with the Pinmux API to do so. The user may have exclusive use of that subsystem.

```
#define RC_MOTOR_DEFAULT_PWM_FREQ   25000
```

PWM: 200 Hz for servo motor

Note only on Debian, uses PRU1.

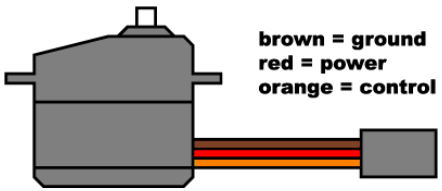
```
int rc_servo_send_pulse_normalized ( int  ch,  double input )
```

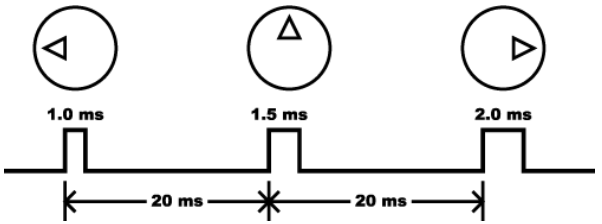
Like rc_send_pulse_us but translates a desired servo position from -1.5 to 1.5 to a corresponding pulse width from 600 to 2400us.

We cannot gurantee all servos will operate over the full range from -1.5 to 1.5 as that is normally considered the extended range. -1.0 to 1.0 is a more typical safe range but may not utilize the full range of all servos.

Example PRU code:

```
; Beginning of loop, should always take 48 instructions to complete
CH1:    QBEQ    CLR1, r0, 0     ; If timer is 0, jump to clear channel
        SET     r30, CH1BIT     ; If non-zero turn on the corresponding
channel
        SUB     r0, r0, 1               ; Subtract one from timer
        CLR     r9, r9.t1               ; waste a cycle for timing
        SBCO    &r9, CONST_PRUSHAREDRAM, 0, 4 ; write 0 to shared memory
```





rc_motor

```
int rc_motor_set   (        int       ch,
                            double    duty )
```

Sets the bidirectional duty cycle (power) to a single motor or all motors if 0 is provided as a channel.

Parameters

[in]	ch	The motor channel (1-4) or 0 for all channels.
[in]	duty	Duty cycle, -1.0 for full reverse, 1.0 for full forward

Note: this uses connectors M1…M4 which are 1 amp H Bridge output.
Not intended for car motor drive!

EECS192 Lecture 2
Jan. 28, 2020

- Checkoff 2/1: Hello World/LED Blink/Switch
- Checkoff 2/8: Benchtop motor and steering (using provided PCB)
- Project proposal (due 2/11 before class)
  - Documentation
  - Block Diagram/Software Model
- Cloud 9 quick demo
- LED/Port Information
- PWM Intro
- Motor Model

Notes:
Check off- Hello World+LED blink+switch
``look don't touch''
Github repo

Motor Model

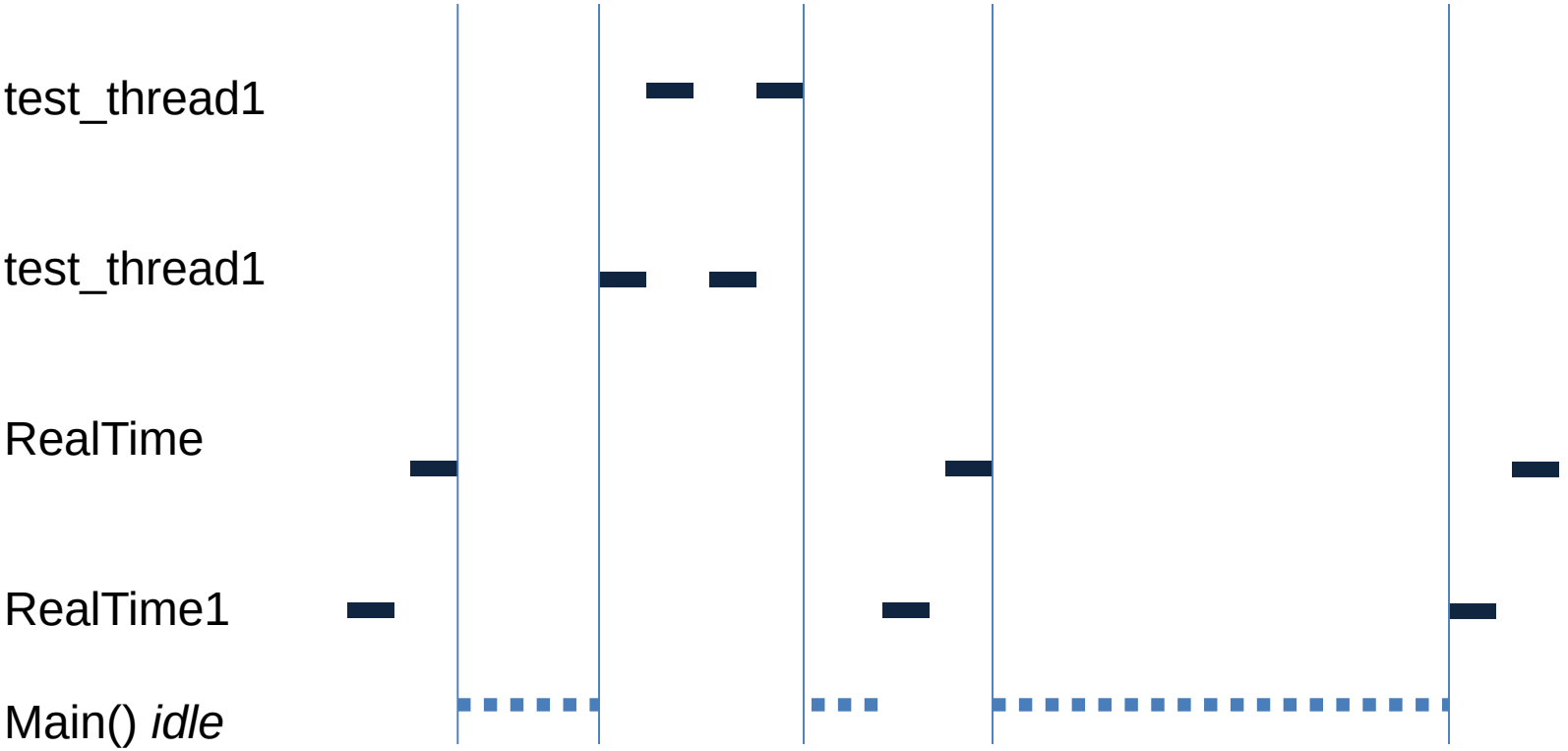
On board….

http://inst.eecs.berkeley.edu/~ee192/sp18/files/NiseAppendixI.pdf

http://inst.eecs.berkeley.edu/~ee192/sp13/pdf/motor_modeling.pdf

Extra Slides

Project Proposal: RTOS timer and threads example



PWM and Timer Intro: PWM (edge)

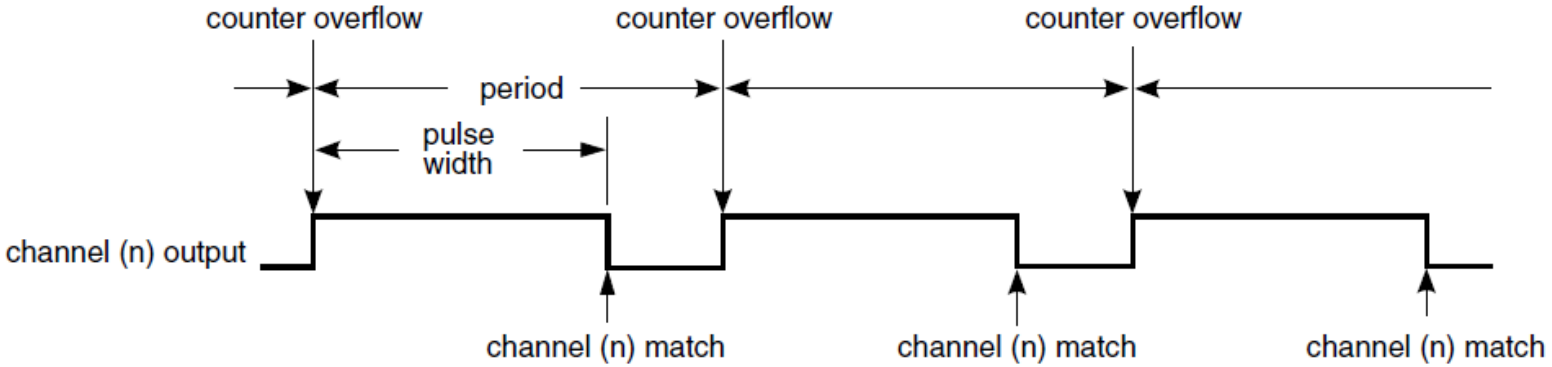


Figure 40-18. EPWM period and pulse width with ELSnB:ELSnA = 1:0

MOD = 0x0008
CnV = 0x0005

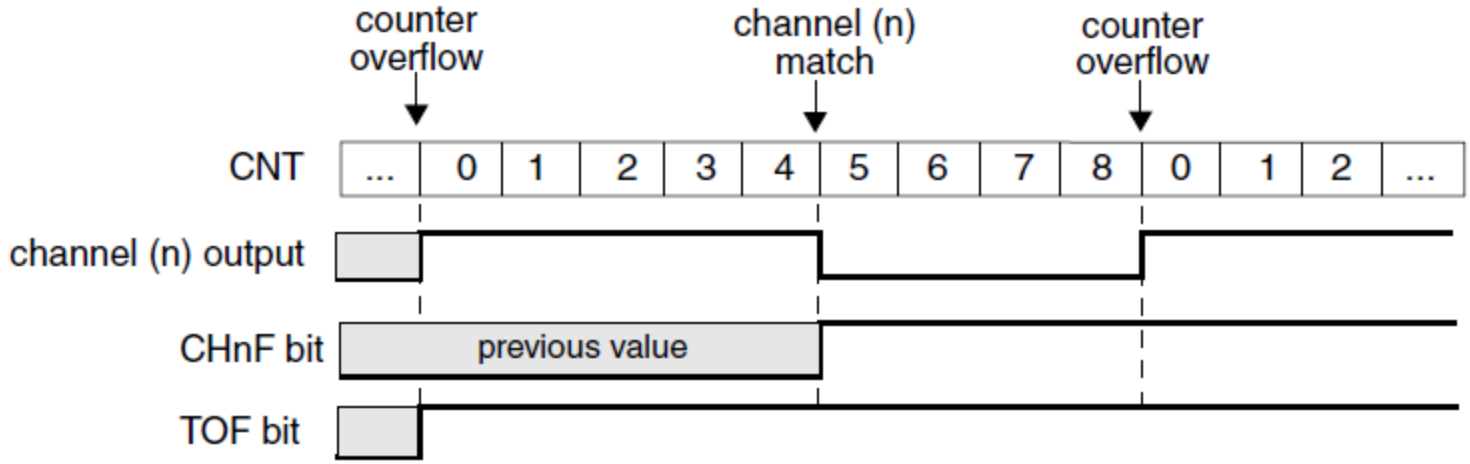


Figure 40-19. EPWM signal with ELSnB:ELSnA = 1:0

PWM and Timer Intro

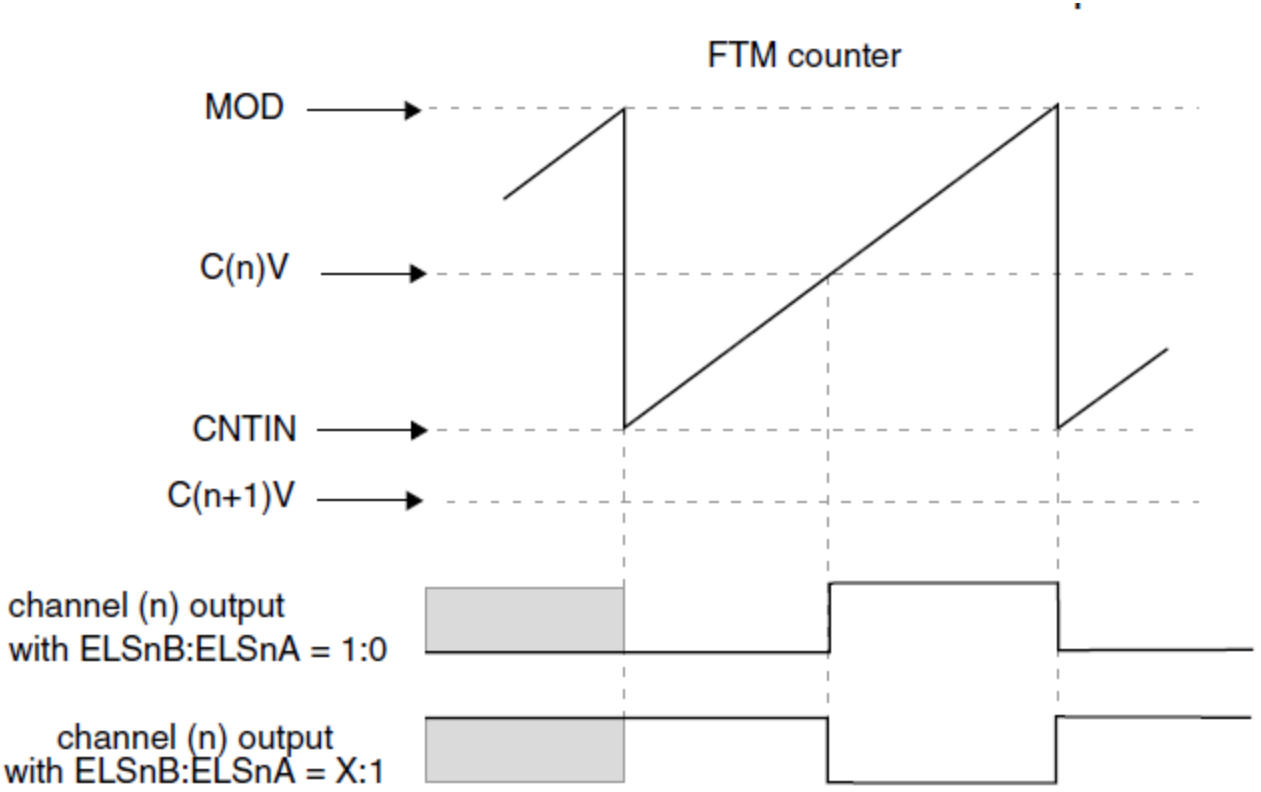


Figure 40-36. Channel (n) output if (C(n+1)V < CNTIN) and (CNTIN < C(n)V < MOD)

PWM and Timer Intro: Dead Time Insertion

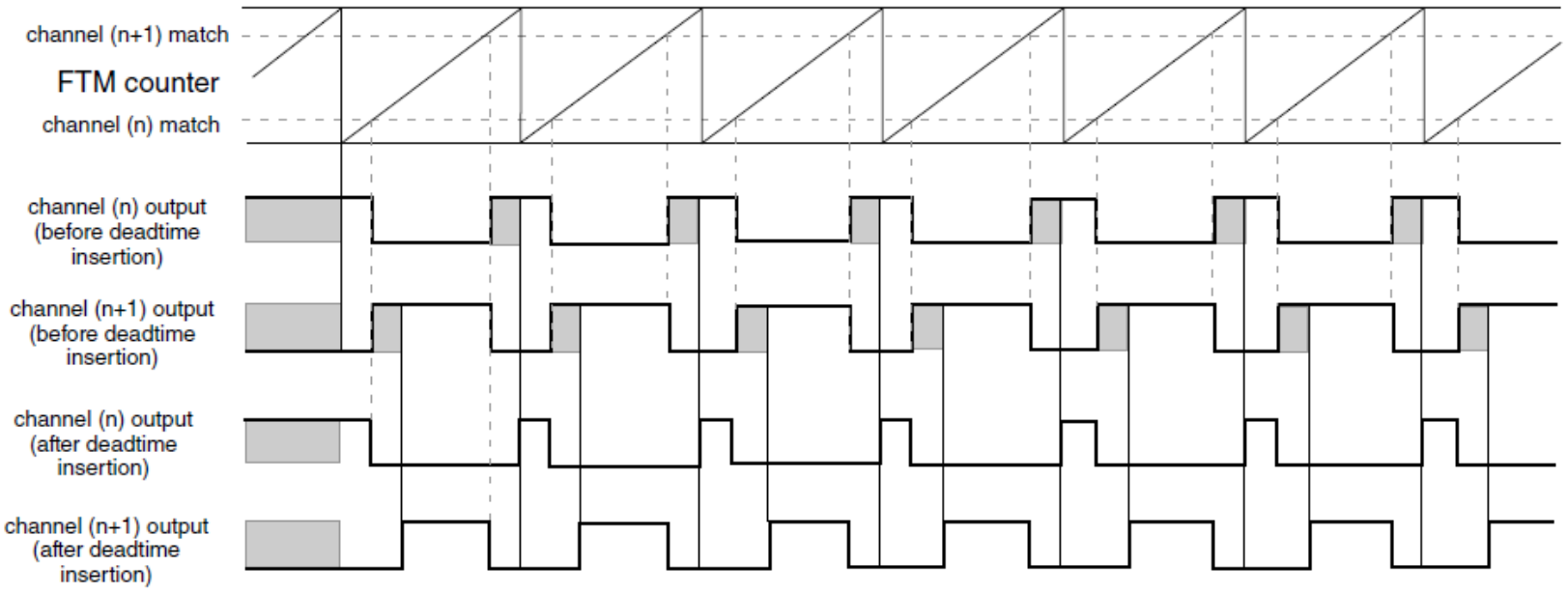


Figure 40-66. Deadtime insertion with ELSnB:ELSnA = X:1, POL(n) = 0, and POL(n+1) = 0

NOTE

- The deadtime feature must be used only in Complementary mode.
- The deadtime feature is not available in Output Compare mode.