EECS192 Lecture 3
Feb. 4, 2020

Notes:
- Handouts: lab rules
- 2/11 project proposal – upload to bcourses by Tues 330 pm
- CP 2: 2/7: bench top Motor drive/stall, steering servo
- Quiz 1: motor behavior Tues 2/11 (See Motor Worksheet week 2)
- CalDay Sat April 4/18

Topics
- Timing in Linux:
- Motor electrical model
  - Motor electromechanical behavior
- Driving MOSFETs and motor
  - UCC21222 MOSFET driver
- PWM issues for motor
- H Bridge motor drive
- (Back EMF measurement)
- Buck Converter (on Handout board)

CheckPoint 2- highlights. See Piazza for full spec

C2.1: Power from bench supply set to 12v.
C2.2: Both LEDs for both buck converters should light up
  C2.2.1: The 5v buck converter output between 4.75 and 5.25v
  C2.2.2: The 6v buck converter output 5.7 and 6.3v

C2.3: With all wheels off the ground, the motor should spin forward (from keybd command)

C2.4: With a non-super (ie, not a Savox) servo connected, demonstrate turning between left, center, and right positions (from keybd command)

C2.6: Motor stall test: 30% duty cycle for 5 seconds, with the wheels held in place.

<u>PWM Frequency > 10 kHZ (Why??)</u>

```
#define RC_MOTOR_DEFAULT_PWM_FREQ   25000
```

  C2.6.2: The current limit on the power supply must be at least 20A Use the higher current connectors on your power supplies. **Do not use test leads for motor current.**
  C2.6.5: No component should get too hot to touch

C2.9: All members must fill out the checkpoint survey before the checkoff close. Completion is individually graded.

Delay timing using rc library

```
start_time = rc_nanos_thread_time();
// routine to be timed:
   for(j = 0; j< 1000; j++)
   {shared_mem_32bit_ptr[ENCODER_MEM_OFFSET+1] = 1;
// set flag to start conversion by PRU
   while(shared_mem_32bit_ptr[ENCODER_MEM_OFFSET+1] == 1);
// wait for PRU to zero word
      for(i = 0; i< 128; i++){
linescan[i]=
    (int) shared_mem_32bit_ptr[ENCODER_MEM_OFFSET+2+i];
// copy data
            }
      }
end_time = rc_nanos_thread_time();
run_time = end_time - start_time;
```

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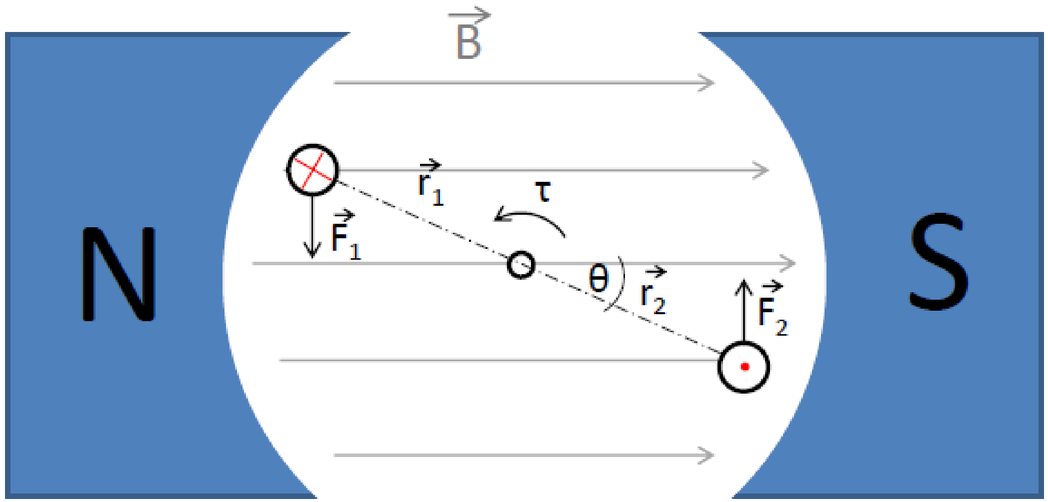
DC Motor Physical Model-review

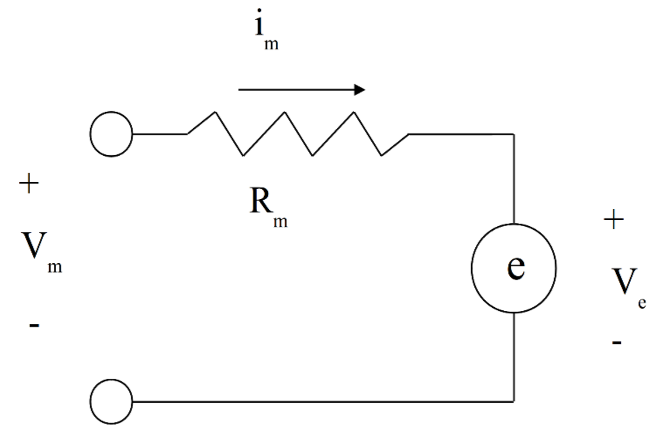


$$\vec{F} = i\vec{l} \times \vec{B}$$

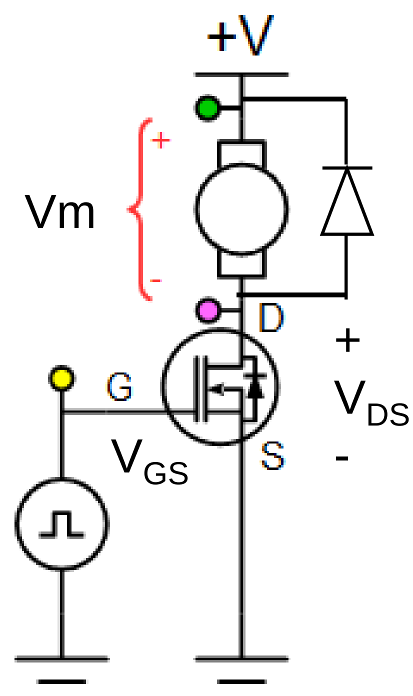
$$\tau = \vec{r}_1 \times \vec{F}_1 + \vec{r}_2 \times \vec{F}_2$$

Motor Electrical Model (neglect inductor)

Motor Electrical Model
Back EMF
Motor electromechanical behavior



Continued on board
Also- see motor worksheet……

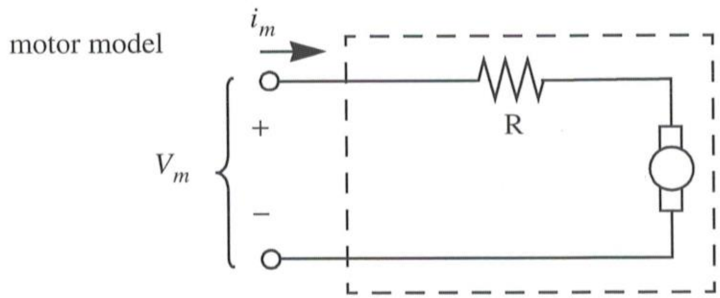


Note: missing e-stop!

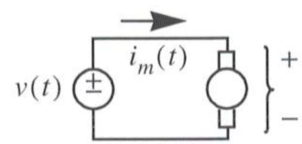
Motor model

For this problem, consider a DC permanent magnet motor (as used in your car). The car is on a carpet and moves in a straight line with no slip between the wheels and the carpet. The car is initially moving at a speed of 2 meters per second.

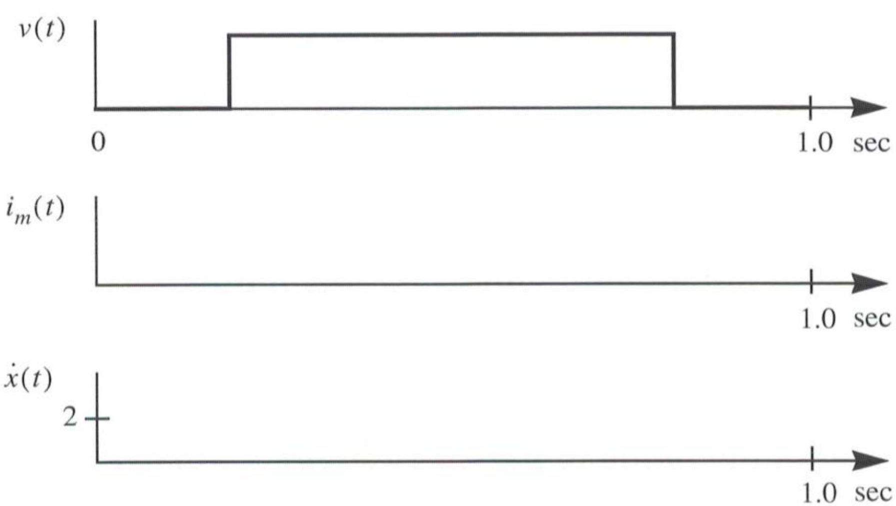
You can assume a motor model as shown below. The qualitative shape of the curves is more important than magnitudes.



[4 pts.] **a)** Consider the motor driven from a voltage source with voltage $v(t)$, as shown. Sketch car velocity $\dot{x}(t)$ and motor terminal current for the time indicated.

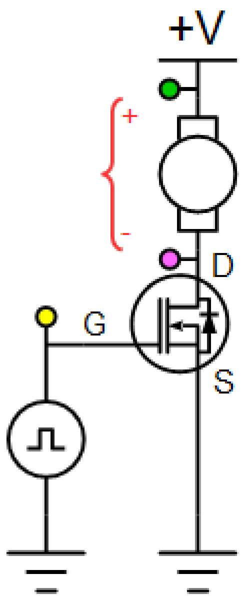


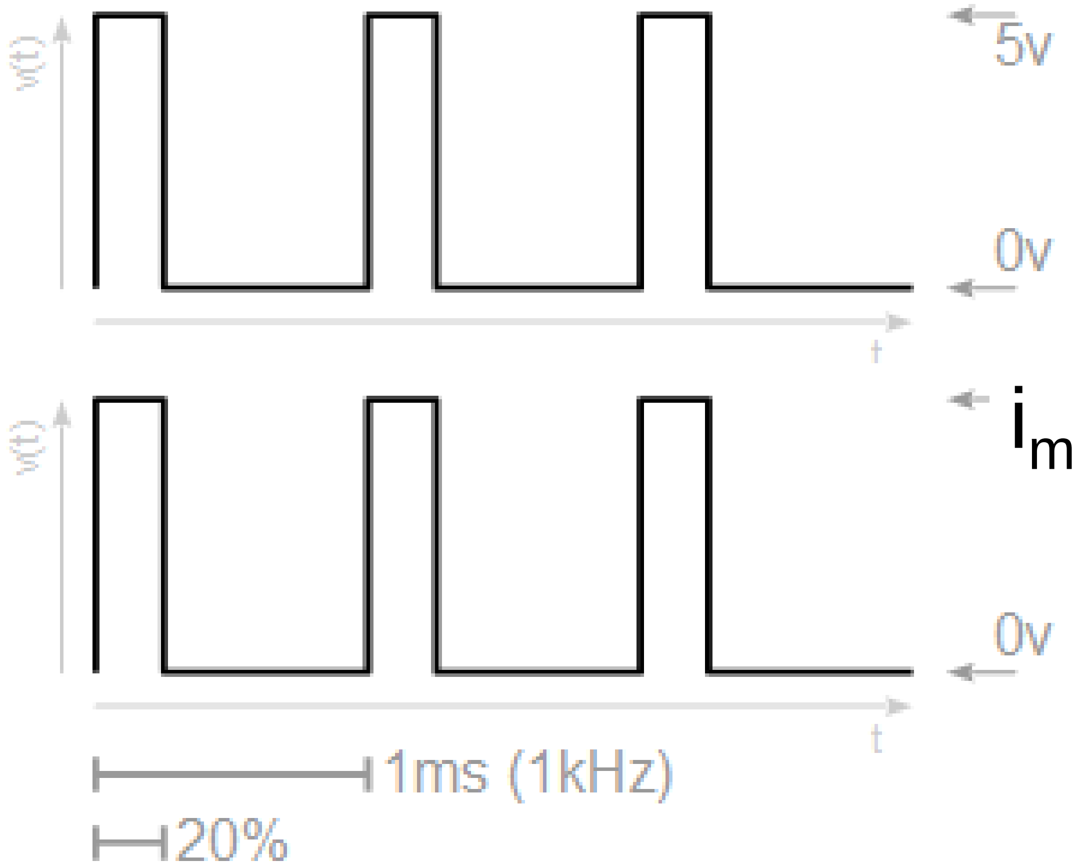
Let peak speed = 5 m/sec
Accel = 5 m/s^2
k_e = 1 v/(m/sec)
On board



(for answer
see sp99 final solution)

PWM for Main Motor control

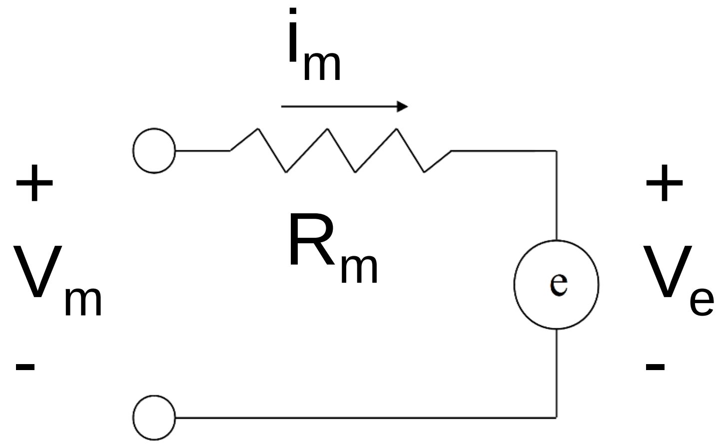




$$\langle i_m \rangle = (T/T_o)\; i_{max}$$

Is i_{max} constant?

Motor Electrical Model



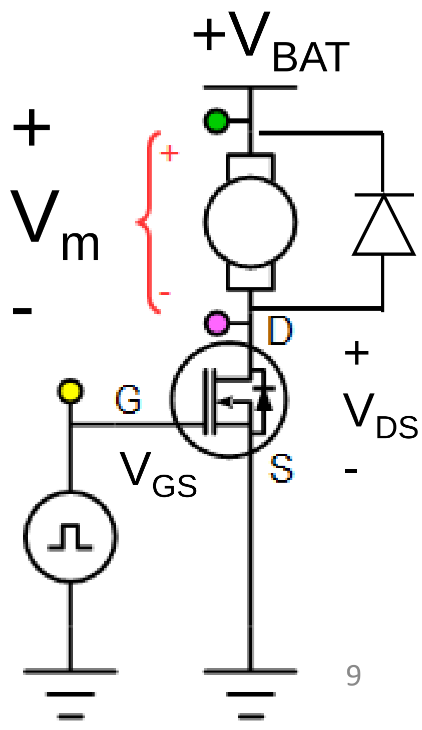
Motor Electrical Model
Back EMF
Motor electromechanical behavior

Also- see motor worksheet……

$$i_m = \frac{V_{BAT} - k_e \dot{\theta}_m}{R_m}$$

Conclusion:
$\langle i_m \rangle = ?$

Motor Resistance?
Peak current?

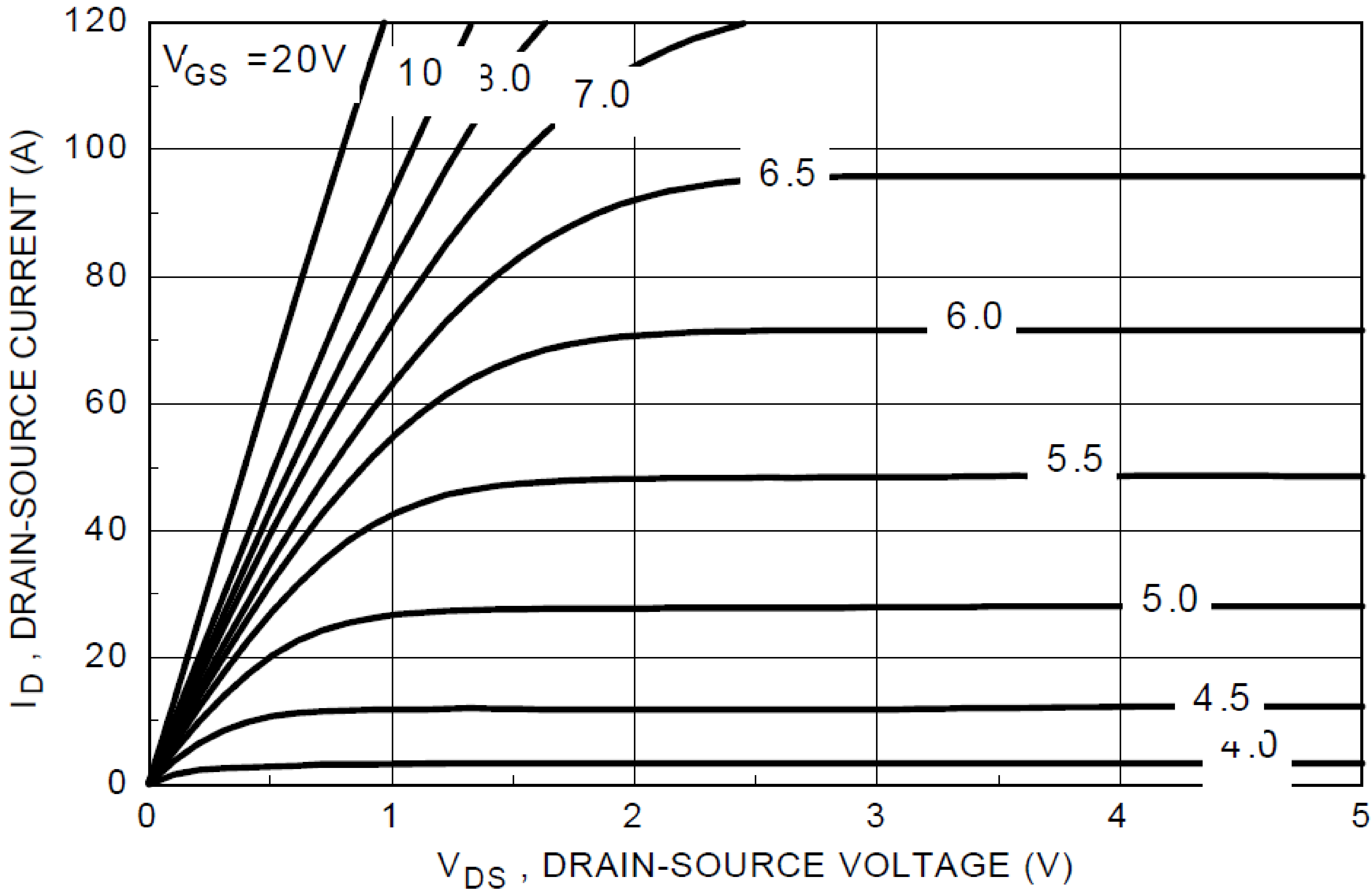


MOSFETs and motor drive

Given: Rm = 0.1 ohms, Vbatt = 7.2 V, Rbat = 0.

Vds = ? ➔ Ids = ? amps

(LiPo 11 V!)



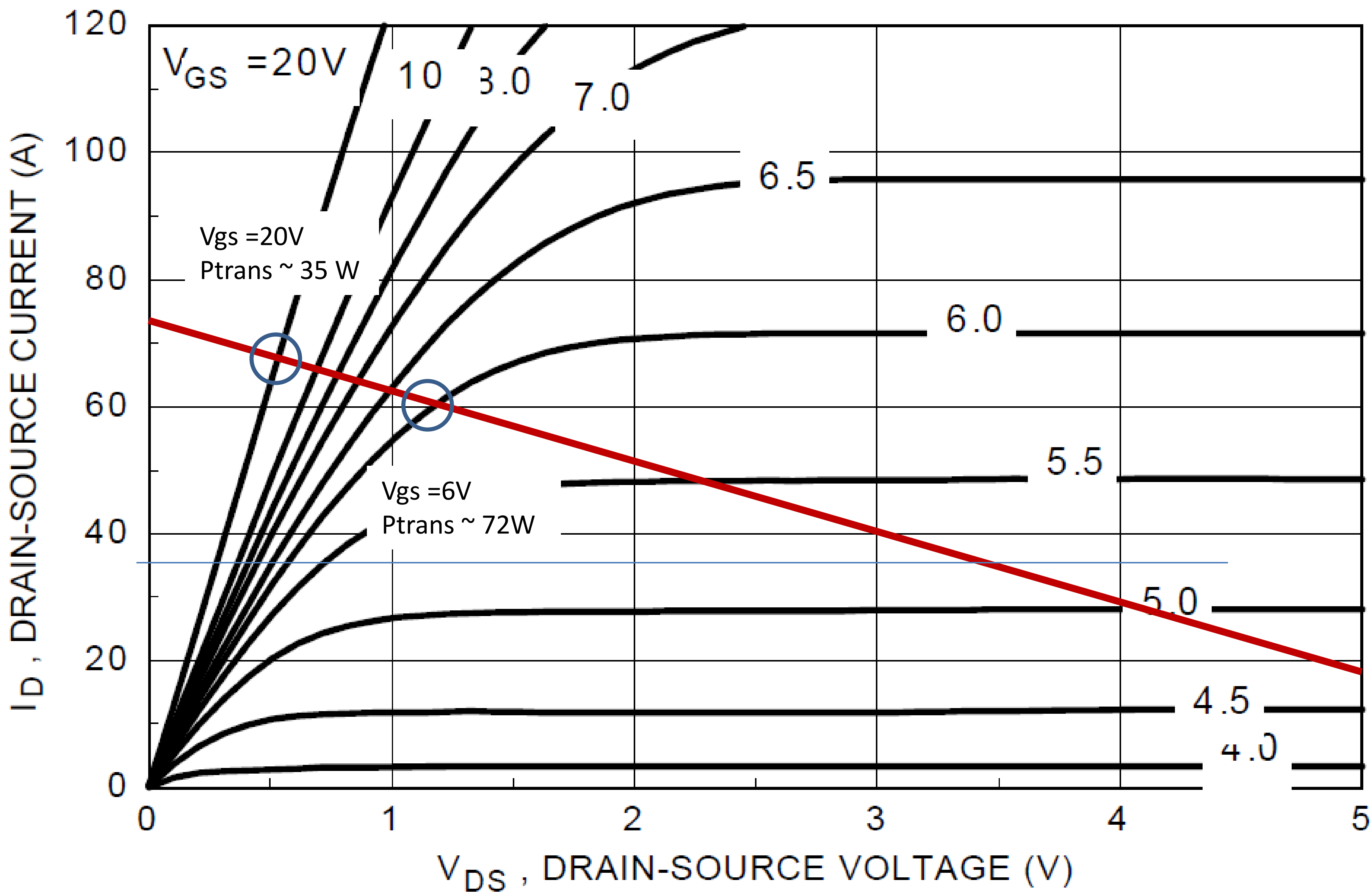
Driving MOSFETs and motor

Rm = 0.1 ohms, Vbatt = 7.2 V, Rbat = 0.

Vds = 3.6V ➔ Ids = (7.2-3.6V)/(0.1 ohm) = 36 amps

Key design points:

1) High Vgs better than low Vgs
2) Switch quickly
3) Make sure Vs=0 (big ground)



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Driving MOSFETs and motor

UCC21222 4-A, 6-A, 3.0-kV_{RMS} Isolated Dual-Channel Gate Driver with Dead Time

1 Features

- Resistor-Programmable Dead Time
- Universal: Dual Low-Side, Dual High-Side or Half-Bridge Driver
- 4-A Peak Source, 6-A Peak Sink Output
- 3-V to 5.5-V Input VCCI Range
- Up to 18-V VDD Output Drive Supply
  - 8-V VDD UVLO
- Switching Parameters:
  - 28-ns Typical Propagation Delay
  - 10-ns Minimum Pulse Width
  - 5-ns Maximum Delay Matching
  - 5.5-ns Maximum Pulse-Width Distortion
- TTL and CMOS Compatible Inputs
- Integrated Deglitch Filter
- I/Os withstand –2-V for 200 ns
- Common-Mode Transient Immunity (CMTI) Greater than 100-V/ns
- Isolation Barrier Life >40 Years
- Surge Immunity up to 7800-V_{PK}
- Narrow Body SOIC-16 (D) Package
- Safety-Related Certifications (Planned):
  - 4242-V_{PK} Isolation per DIN V VDE V 0884-11:2017-01 and DIN EN 61010-1
  - 3000-V_{RMS} Isolation for 1 Minute per UL 1577
  - CSA Certification per IEC 60950-1, IEC 62368-1 and IEC 61010-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011
- Create a Custom Design Using the UCC21222 With the WEBENCH® Power Designer

2 Applications

- Isolated converters in AC-to-DC and DC-to-DC Power Supplies
- Server, Telecom, IT and Industrial Infrastructures
- Motor Drives and Solar Inverters
- HEV and EV Battery Chargers
- Industrial Transportation
- Uninterruptible Power Supply (UPS)

3 Description

The UCC21222 device is an isolated dual channel gate driver with programmable dead time. It is designed with 4-A peak-source and 6-A peak-sink current to drive power MOSFET, IGBT, and GaN transistors.

The UCC21222 device can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. 5ns delay matching performance allows two outputs to be paralleled, doubling the drive strength for heavy load conditions without risk of internal shoot-through.

The input side is isolated from the two output drivers by a 3.0-kV_{RMS} isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI).

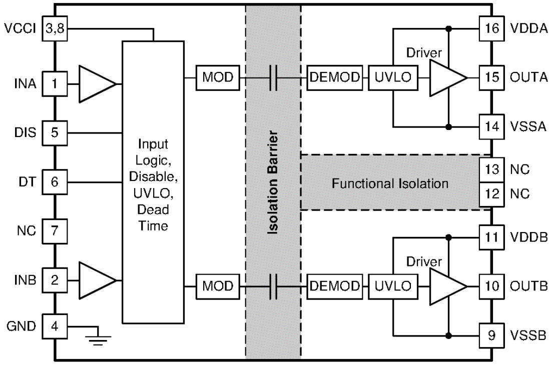
Resistor programmable dead time gives the capability to adjust dead time for system constraints to improve efficiency and prevent output overlap. Other protection features include: Disable feature to shut down both outputs simultaneously when DIS is set high, integrated deglitch filter that rejects input transients shorter than 5-ns, and negative voltage handling for up to -2-V spikes for 200-ns on input and output pins. All supplies have UVLO protection.

Device Information(1)

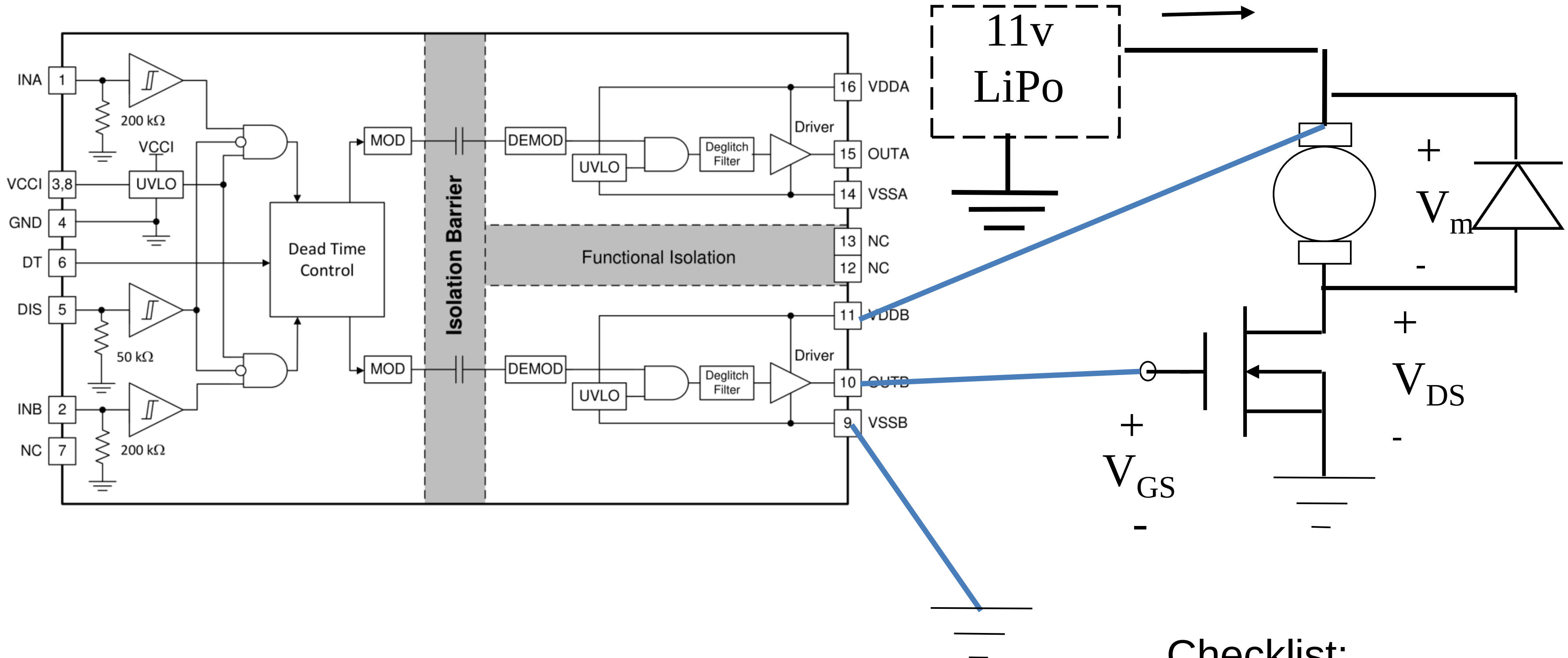
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC21222	SOIC (16)	9.9 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



Motor Drive with UCC21222 gate driver



Details On board….

Checklist:

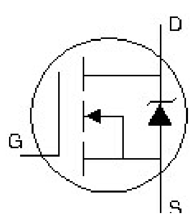
1) Emergency stop
2) Reset Protection
3) Snubbing

Driving MOSFETs and motor

How to choose PWM frequency?

CSD18542KTT Power MOSFET

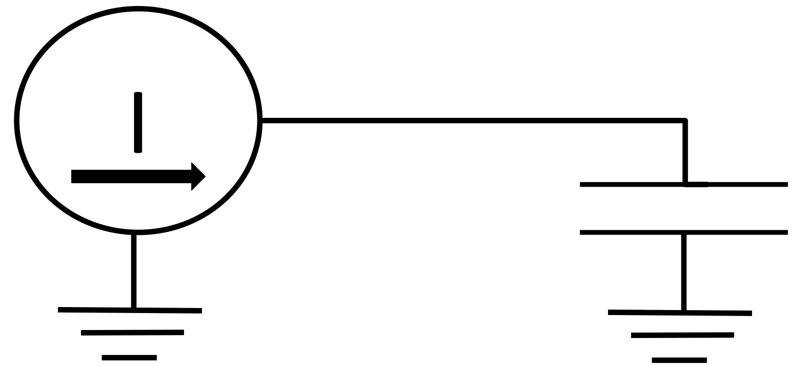
DYNAMIC CHARACTERISTICS					
C_{iss}	Input capacitance		3900	5070	pF
C_{oss}	Output capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz	570	740	pF
C_{rss}	Reverse transfer capacitance		11	14	pF
R_G	Series gate resistance		1.3	2.6	Ω
Q_g	Gate charge total (4.5 V)		21	27	nC
Q_g	Gate charge total (10 V)		44	57	nC
Q_{gd}	Gate charge gate-to-drain	V_{DS} = 30 V, I_D = 100 A	6.9		nC
Q_{gs}	Gate charge gate-to-source		10		nC
$Q_{g(th)}$	Gate charge at V_{th}		7.3		nC
Q_{oss}	Output charge	V_{DS} = 30 V, V_{GS} = 0 V	63		nC
$t_{d(on)}$	Turnon delay time		6		ns
t_r	Rise time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 100 A, R_G = 0 Ω	5		ns
$t_{d(off)}$	Turnoff delay time		18		ns
t_f	Fall time		21		ns
DIODE CHARACTERISTICS					
V_{SD}	Diode forward voltage	I_{SD} = 100 A, V_{GS} = 0 V	0.9	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= 30 V, I_F = 100 A, di/dt = 300 A/μs	148		nC
t_{rr}	Reverse recovery time		53		ns



How to choose PWM frequency: UCC21222 driver constraint

I = C dv/dt

(on board)



Gate capacitance
5000 pF

6.10 Switching Characteristics

V_{VCCI} = 3.3 V or 5.5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, load capacitance C_{OUT} = 0 pF, T_A = –40°C to +125°C unless otherwise noted[(1)].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output rise time, see Figure 28	C_{VDD} = 10 µF, C_{OUT} = 1.8 nF, V_{VDDA}, V_{VDDB} = 12 V, f = 1 kHz		5	16	ns
t_{FALL}	Output fall time, see Figure 28	C_{VDD} = 10 µF, C_{OUT} = 1.8 nF , V_{VDDA}, V_{VDDB} = 12 V, f = 1 kHz		6	12	ns

OUTPUT				
I_{OA+}, I_{OB+}	Peak output source current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement	4	A
I_{OA-}, I_{OB-}	Peak output sink current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement	6	A

Low Side Drive example

UVLO = under voltage lockout = 9 V

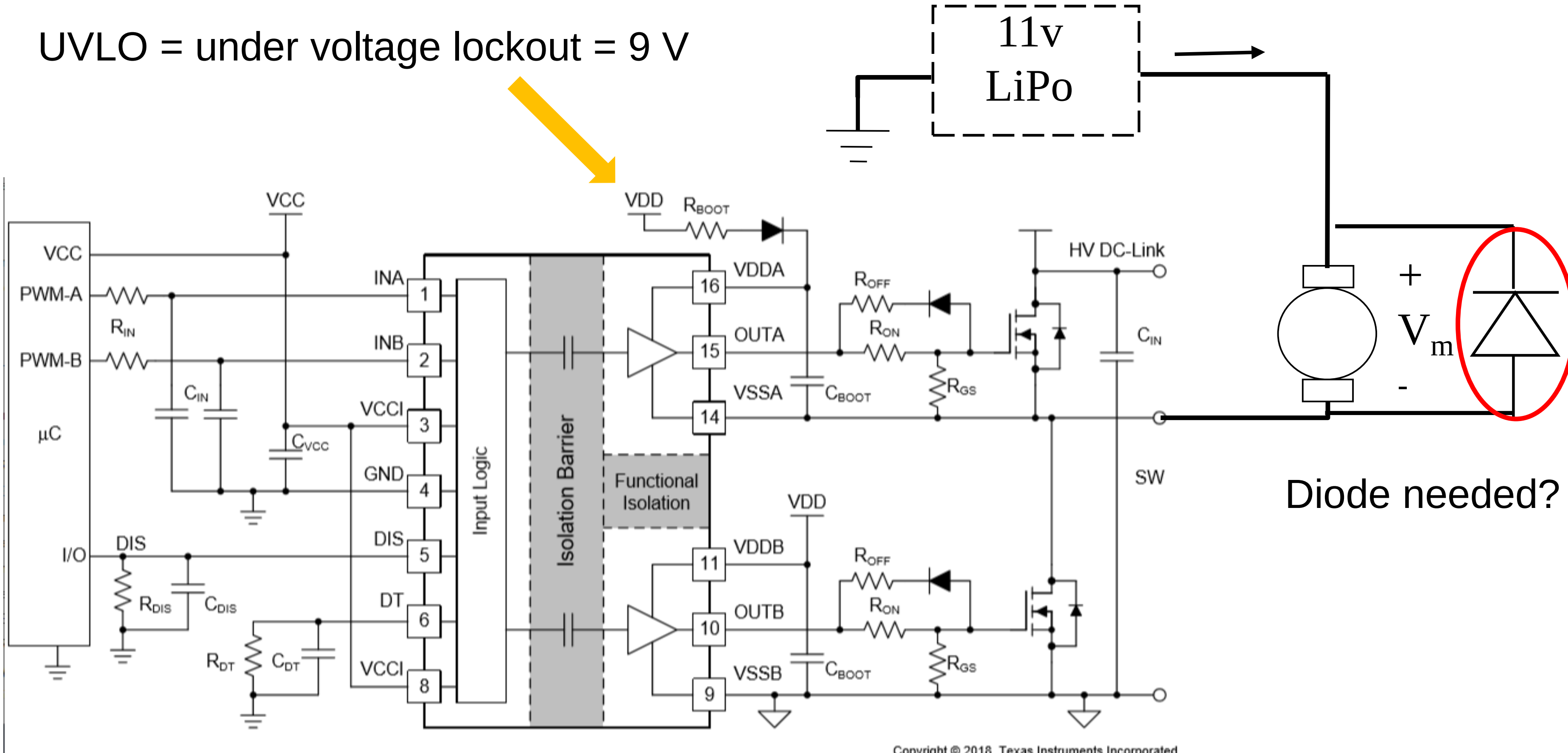
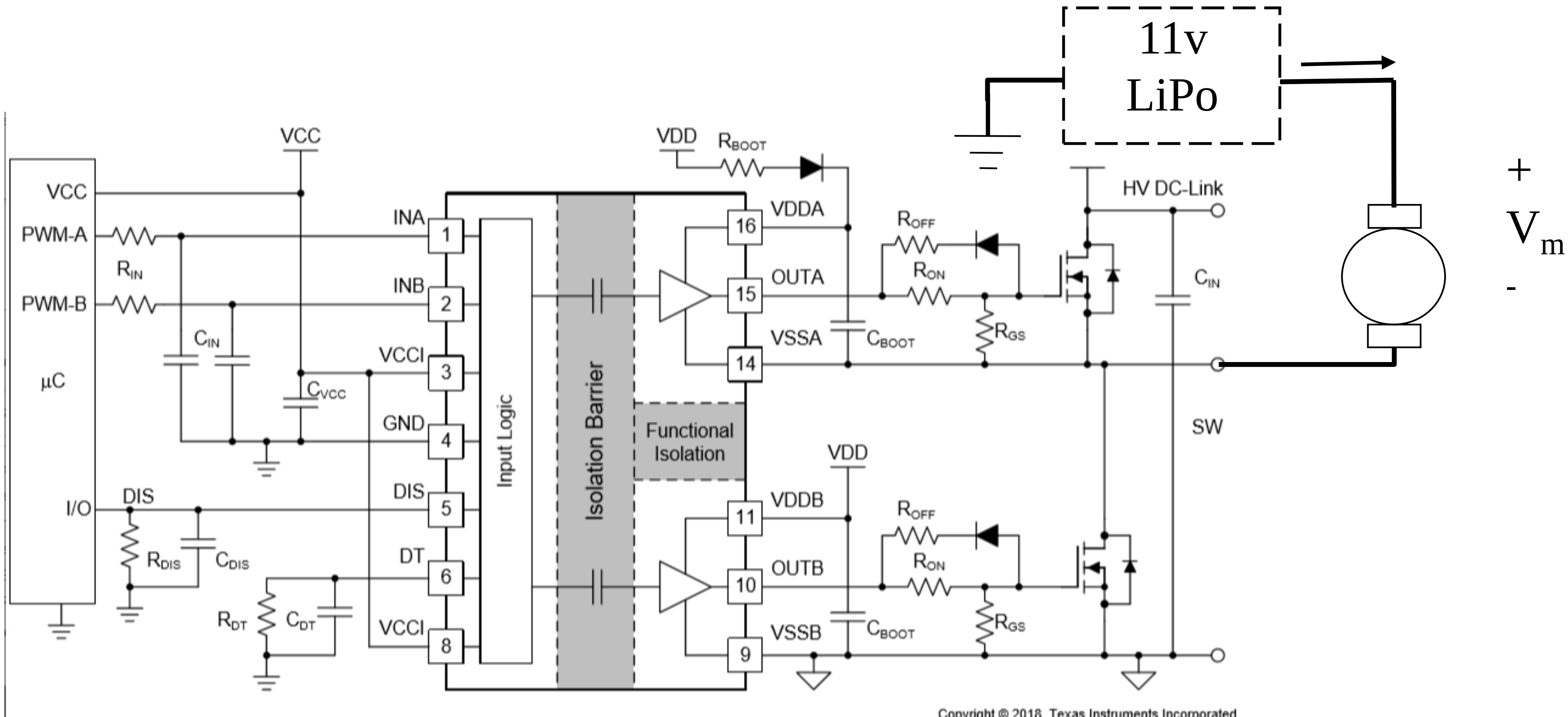


Figure 38. Typical Application Schematic

Table 3. INPUT/OUTPUT Logic Table[1]

INPUTS		DIS	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	L or Left Open	L	L	If the dead time function is used, output transitions occur after the dead time expires. See Programmable Dead Time (DT) Pin.
L	H	L or Left Open	L	H	
H	L	L or Left Open	H	L	
H	H	L or Left Open	L	L	DT is programmed with R_{DT}.
H	H	L or Left Open	H	H	DT pin is left open or pulled to VCCI.
Left Open	Left Open	L or Left Open	L	L	
X	X	H	L	L	

(1) "X" means L, H or left open. For improved noise immunity, TI recommends connecting INA, INB, and DIS to GND, and DT to VCCI, when these pins are not used.



UCC 21222 design details

9.2.2.5 Gate Driver Output Resistor

The external gate driver resistors, R_{ON}/R_{OFF}, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

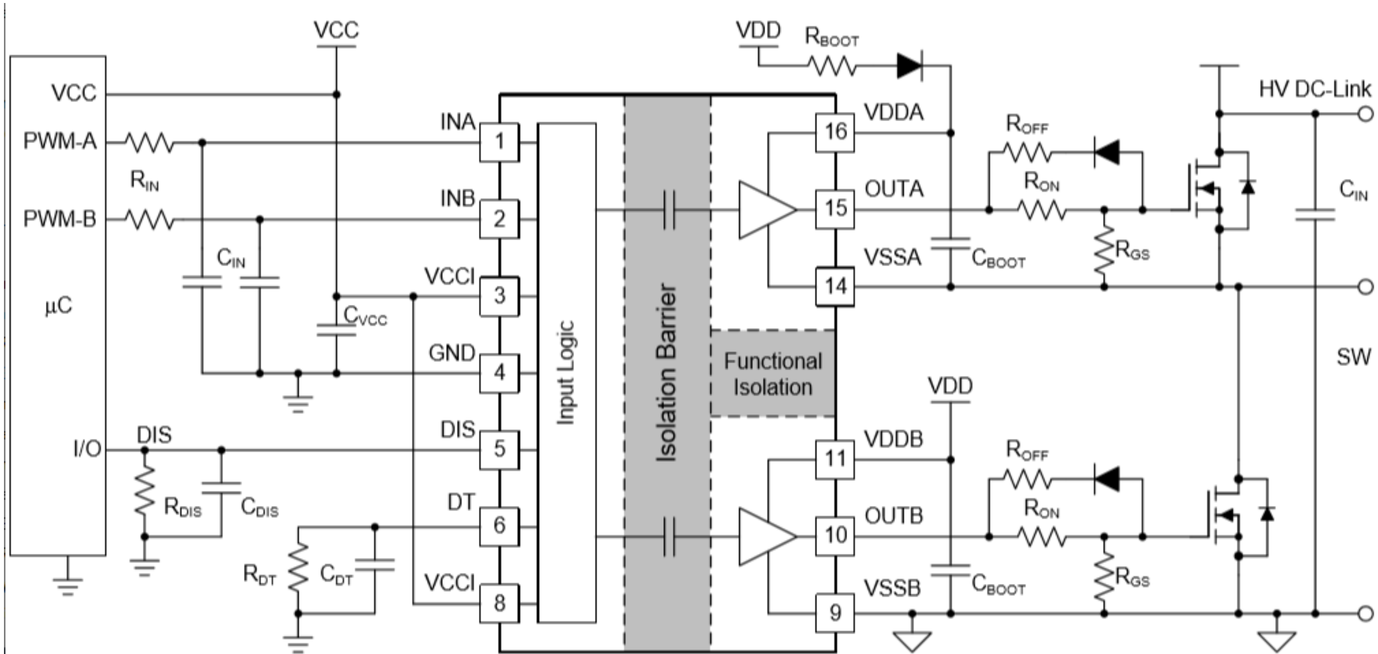
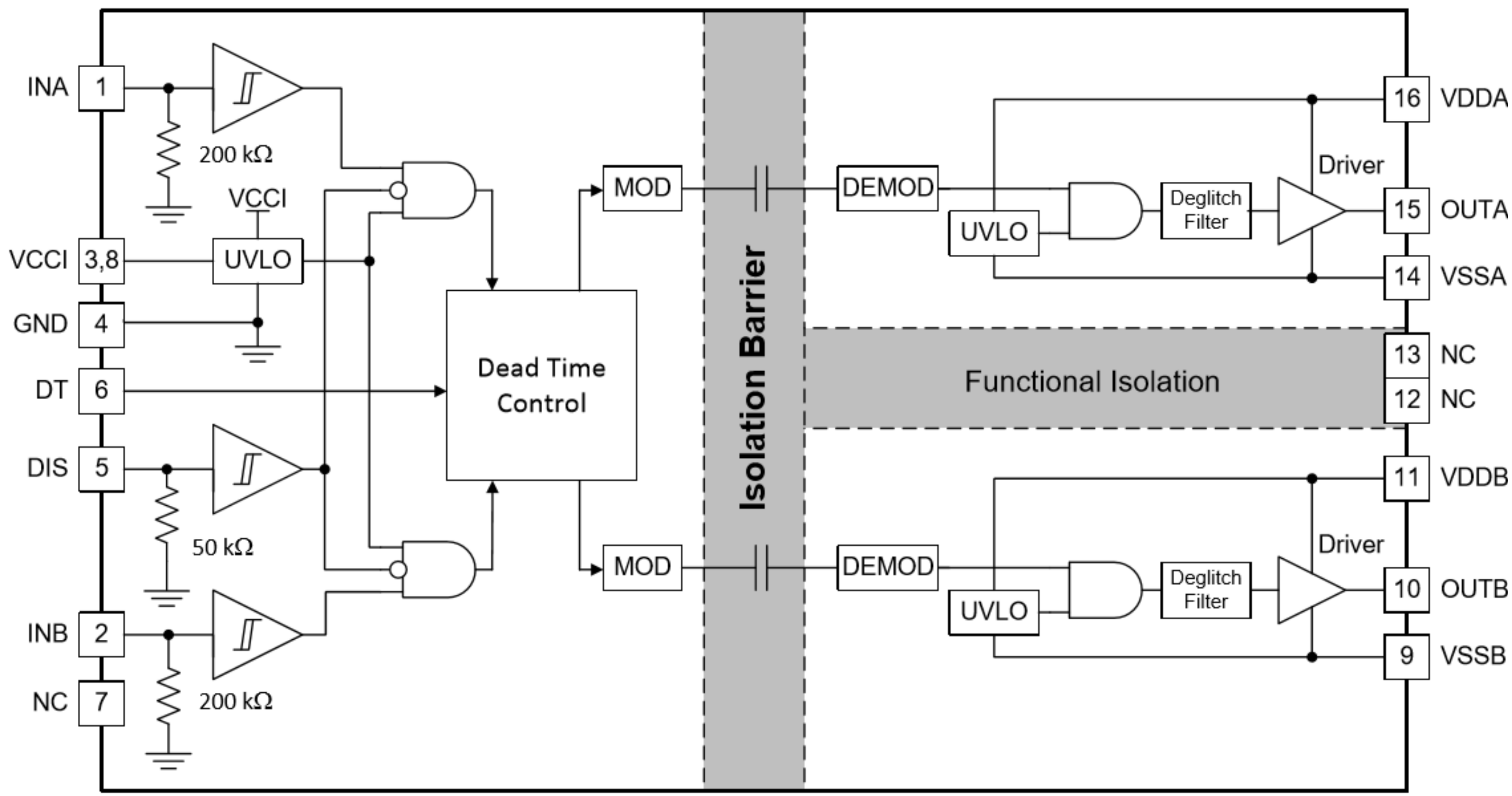


Figure 38. Typical Application Schematic

UCC 21222 internal details

UVLO: under voltage lockout (check data sheet)
DT: dead time useful for H Bridge

nctional Block Diagram



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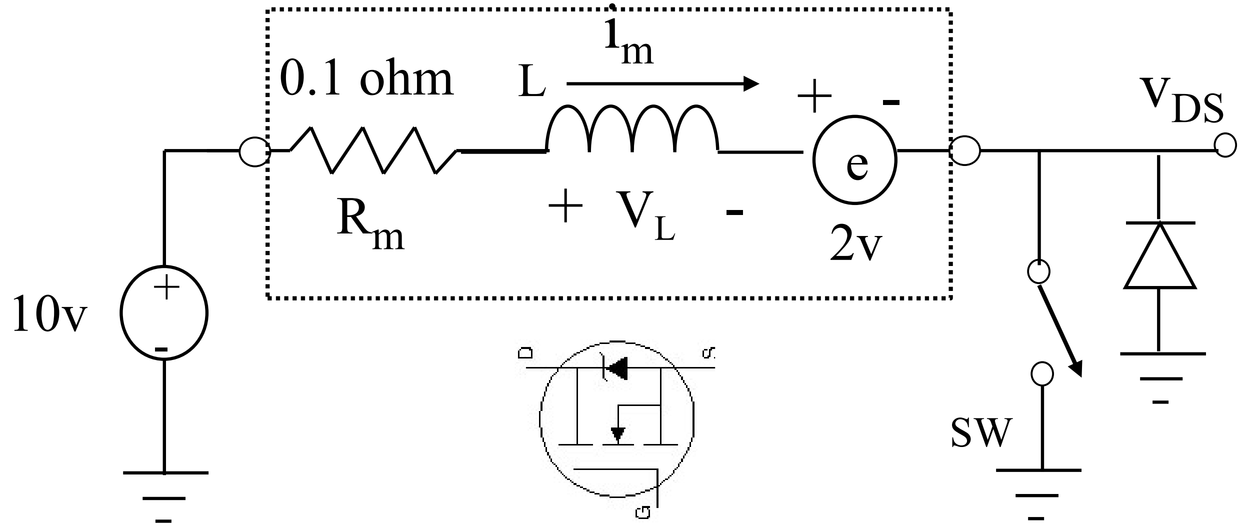
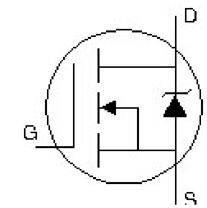
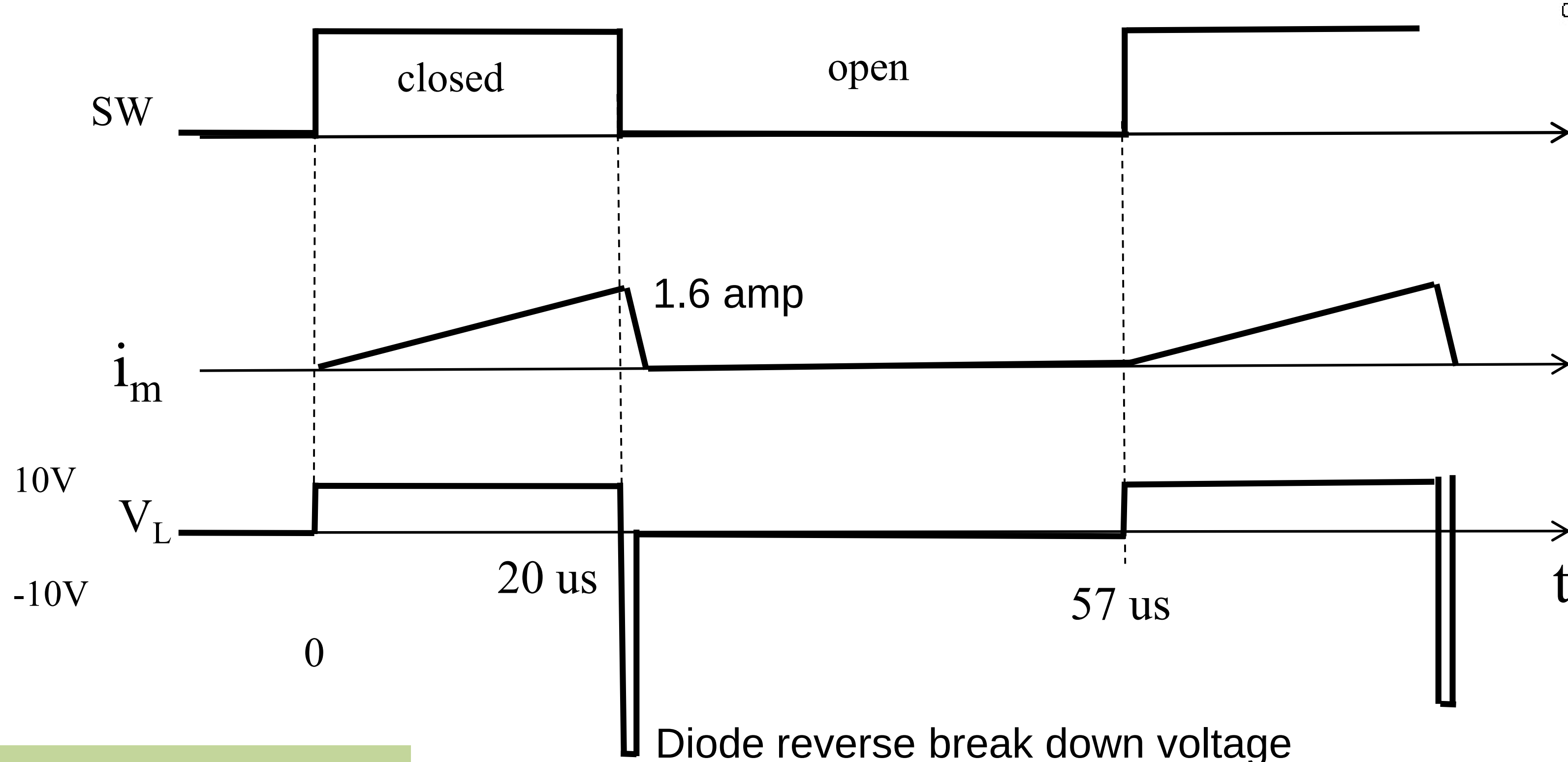
What does high side transistor do?

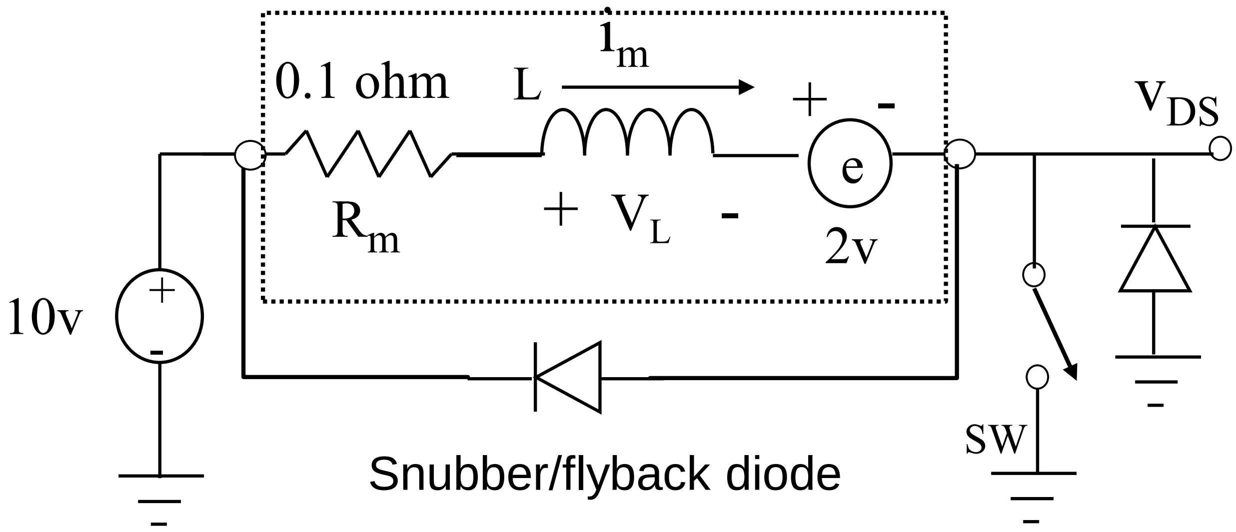
Assume ideal diode,
ideal switch, L= 100 μH.
Time constant τ = 1 ms.
Steady state,
constant velocity.
Initial rate:
V/L= +8x10^4 amp/sec



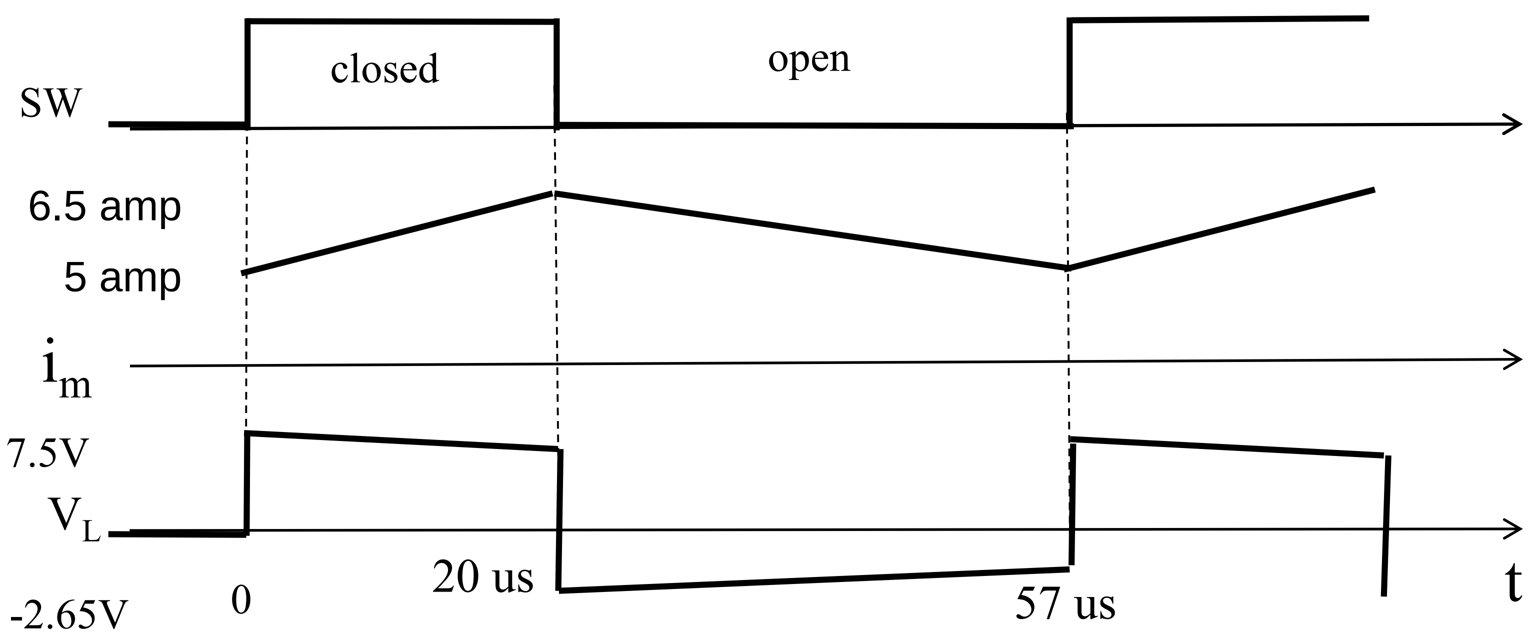




Motor+flywheel diode



Assume ideal diode, ideal switch, L= 100 μH.
Time constant τ = 1 ms.
Steady state, constant velocity.
Assume i_{min} = 5 amp



Note: 25 kHz PWM reduces peak current

Motor+flywheel diode

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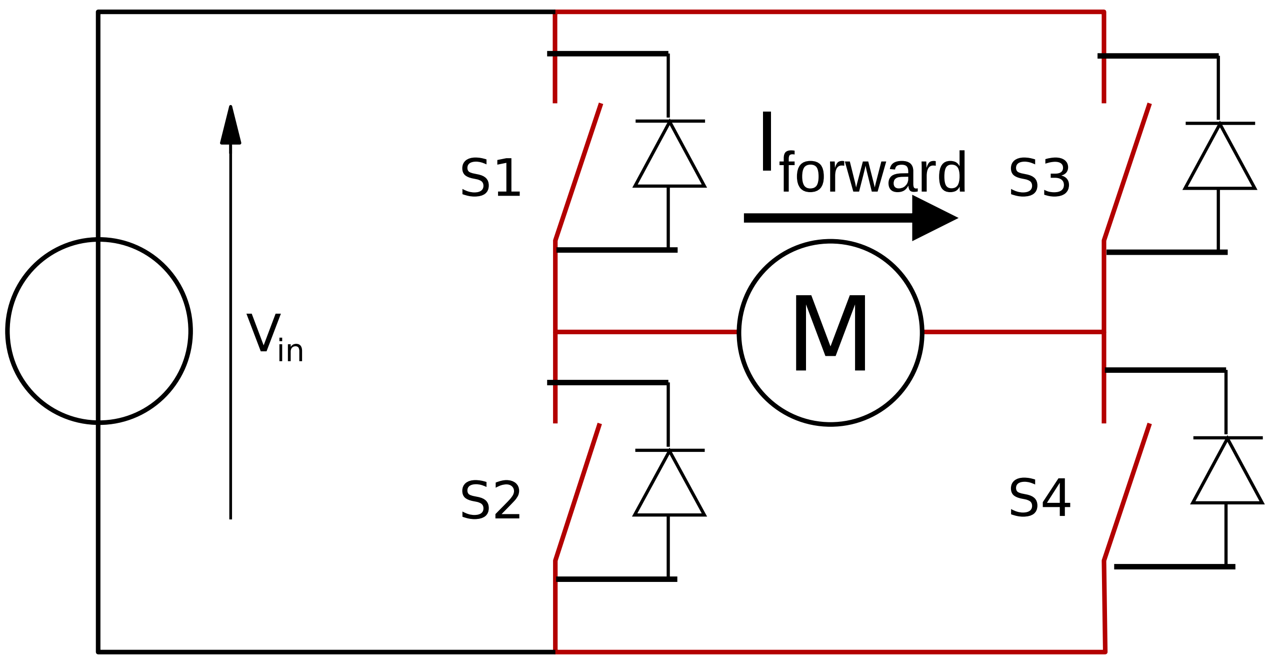
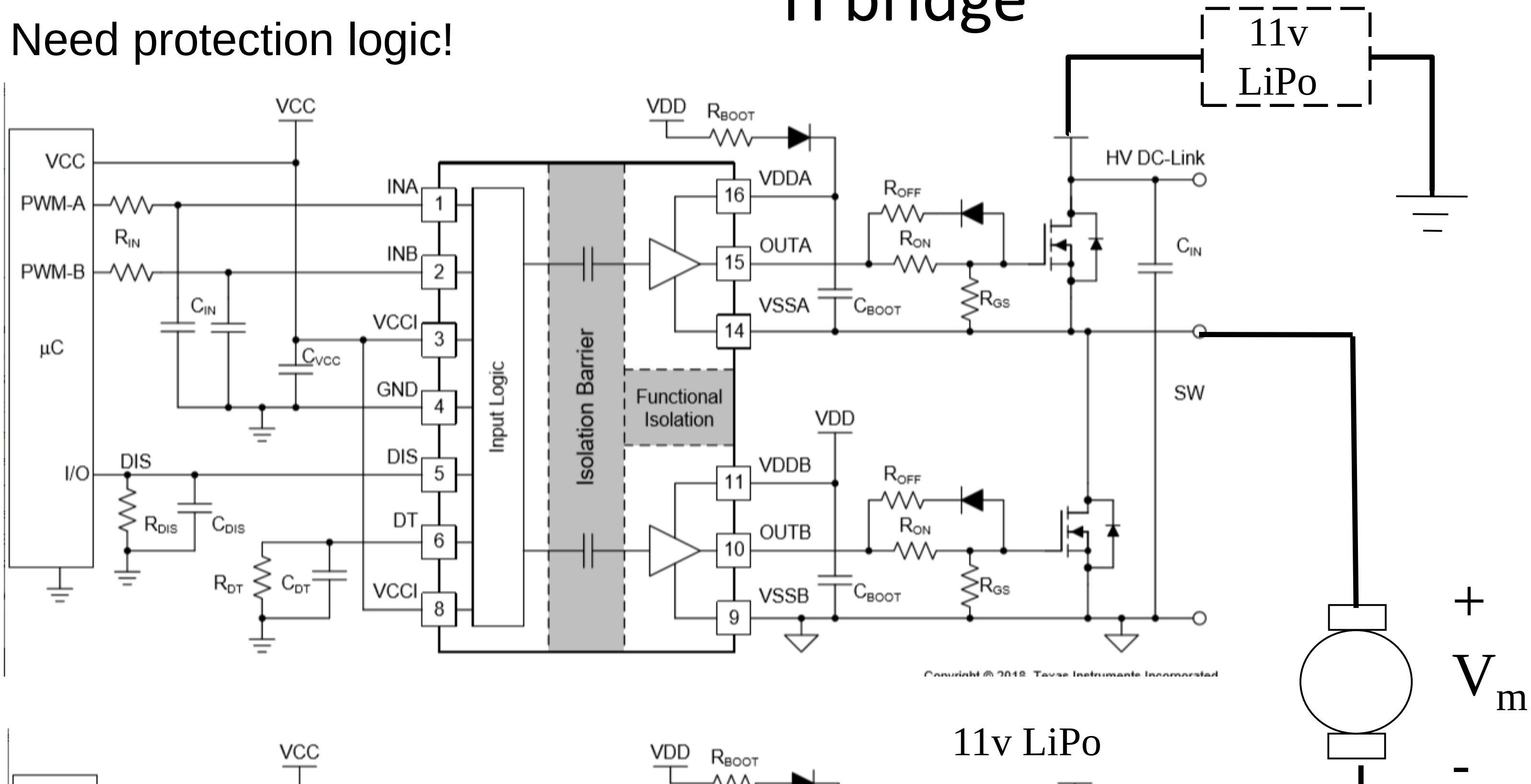
H Bridge Concept

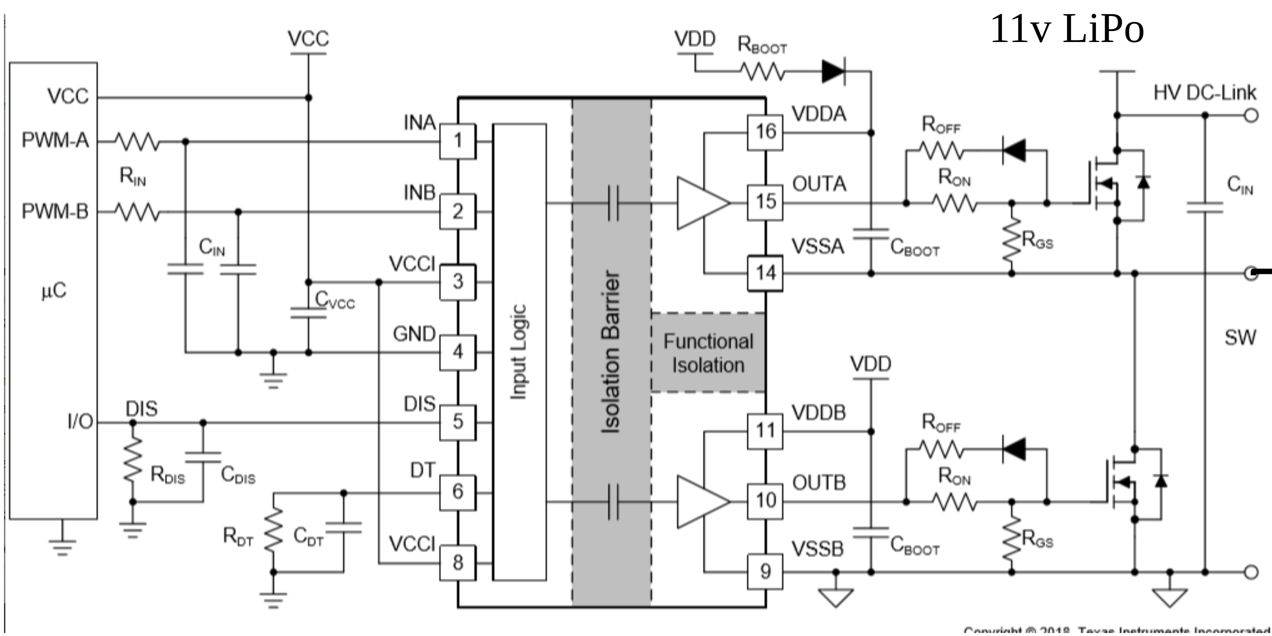


S1	S2	S3	S3	Function?
Off	Off	Off	Off	
On	Off	Off	On	
Off	On	On	Off	
On	On	Off	Off	
On	Off	On	off	
Off	On	Off	on	

H bridge

Need protection logic!





!!!!CAUTION!!!!
Software fries hardware….
Need protection logic- 74HCxxx
Estop?

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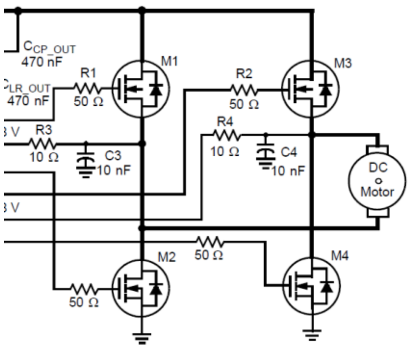
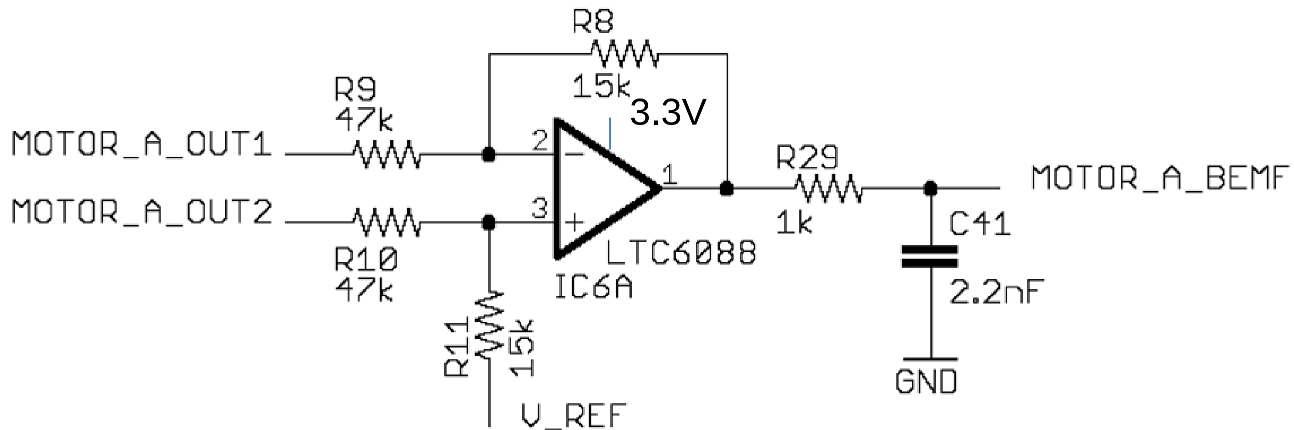
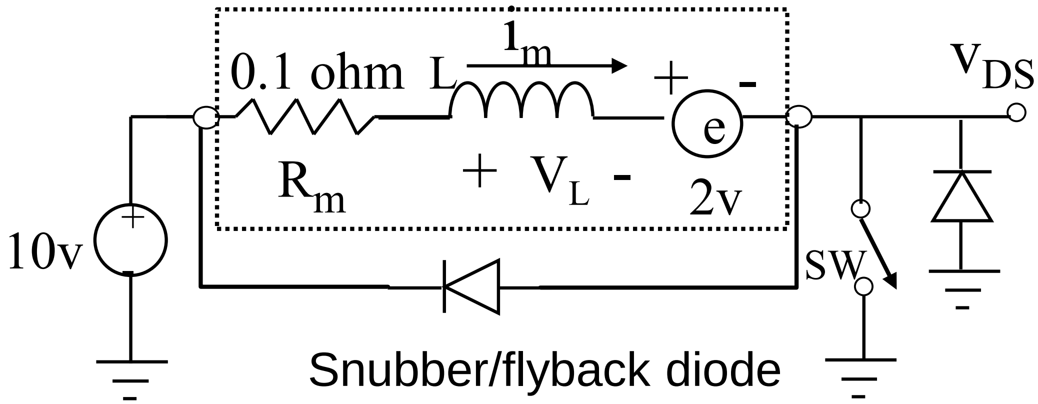


atic with External Protection Circuit



Differential amp to read back EMF for
H Bridge driving motor. Change values for
12V Back EMF…

Back EMF velocity sensing



$$V_{DS} = 10V - V_{DIODE}$$

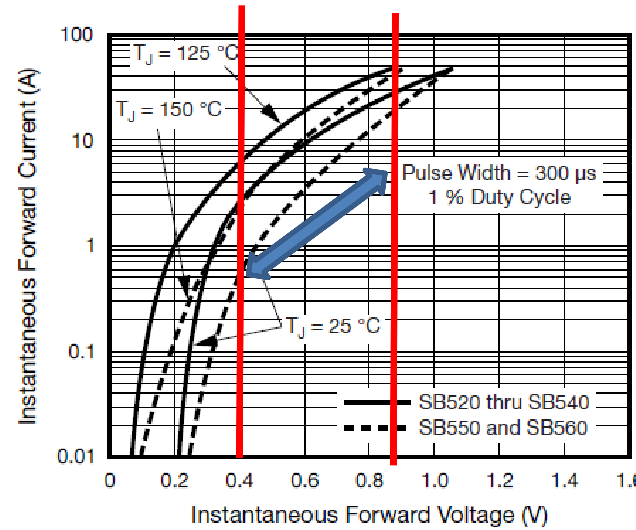
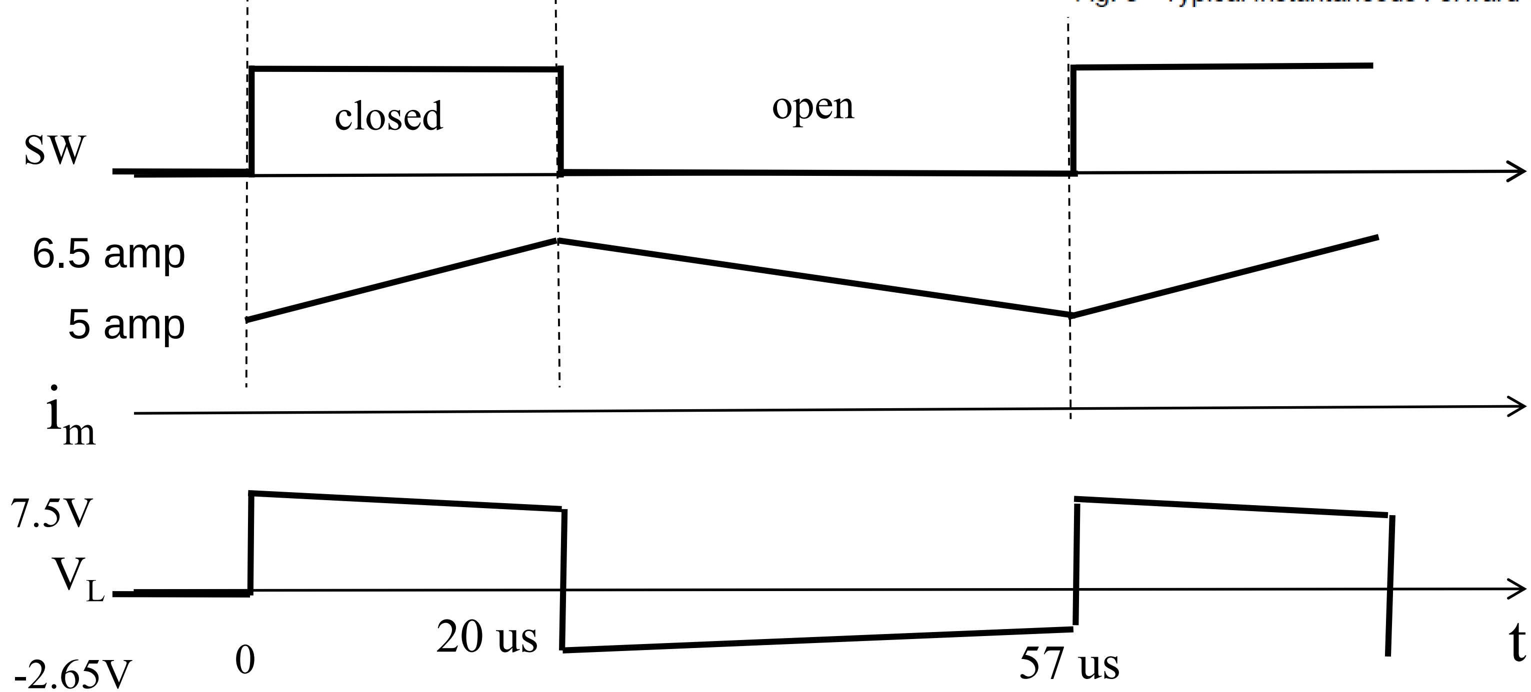


Fig. 3 - Typical Instantaneous Forward Characteristics



Back EMF velocity sensing

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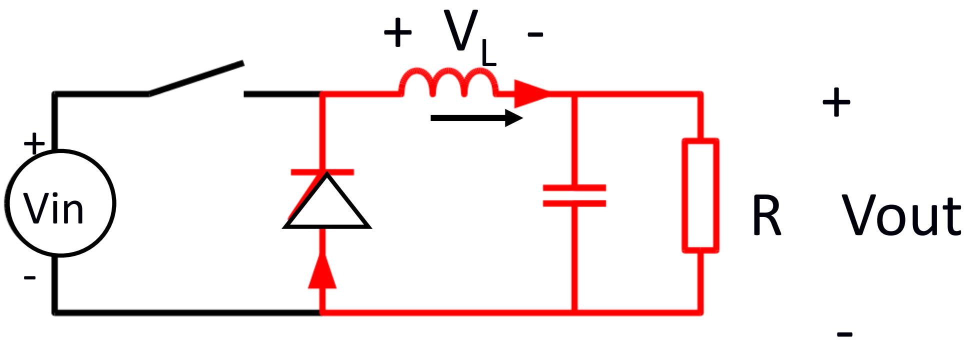
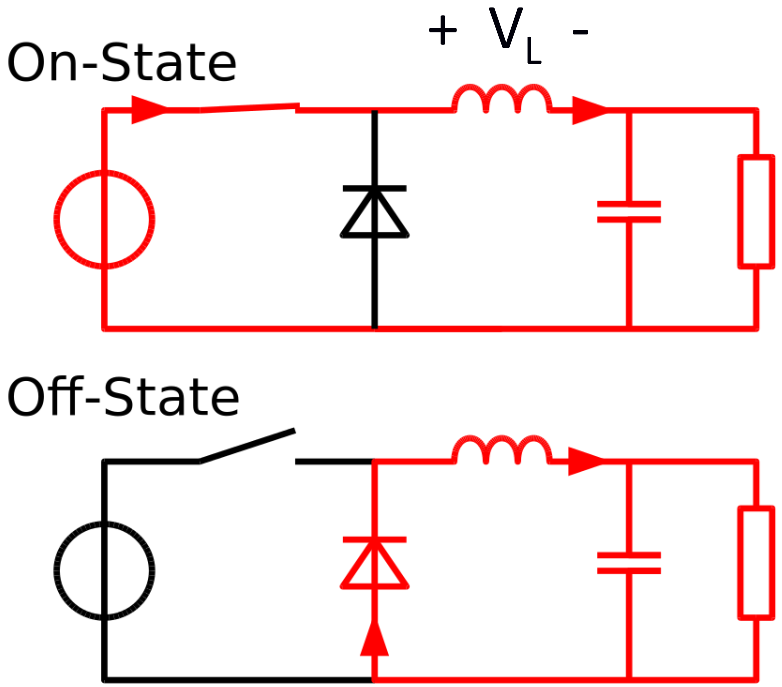
Buck Converter- DC-DC

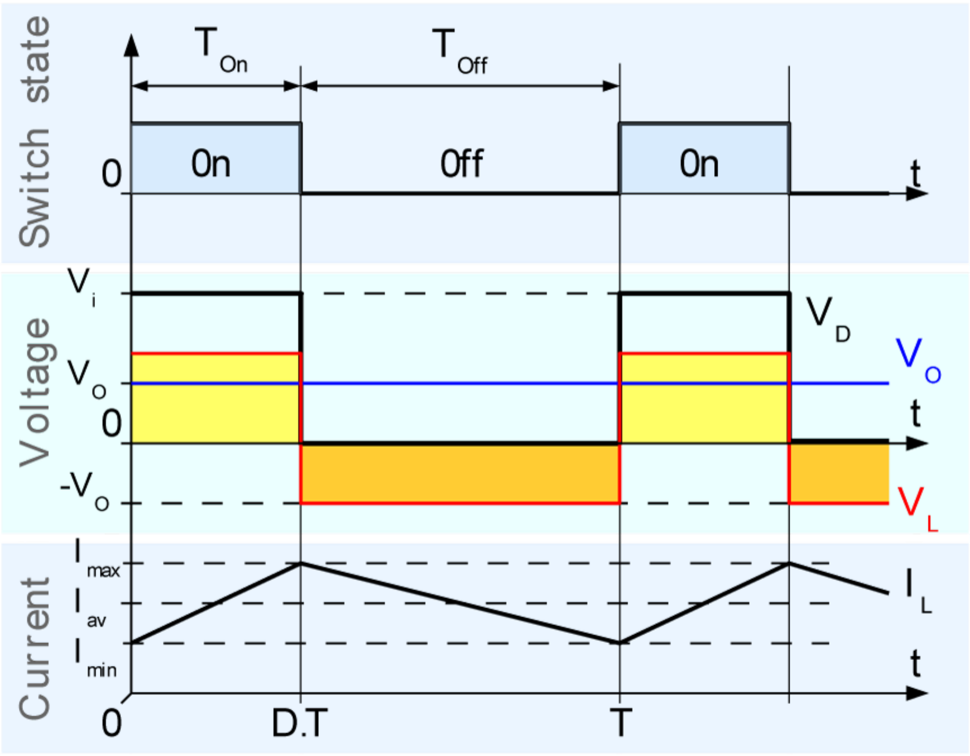


Why? Efficiency ~90%

Waveforms on board (also see buck converter notes.)
Buck: high to low. Boost: low-to-high)

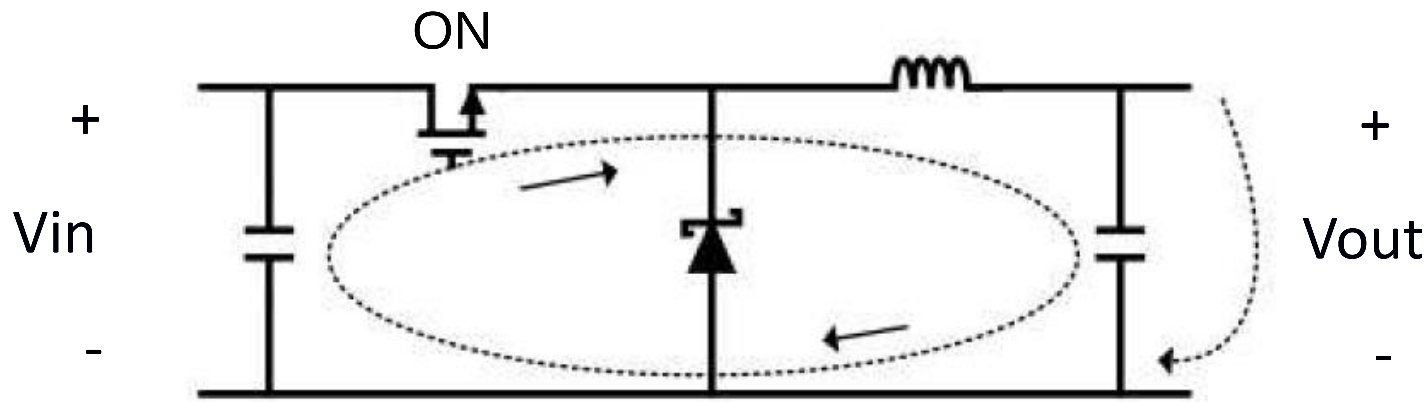
Buck Converter

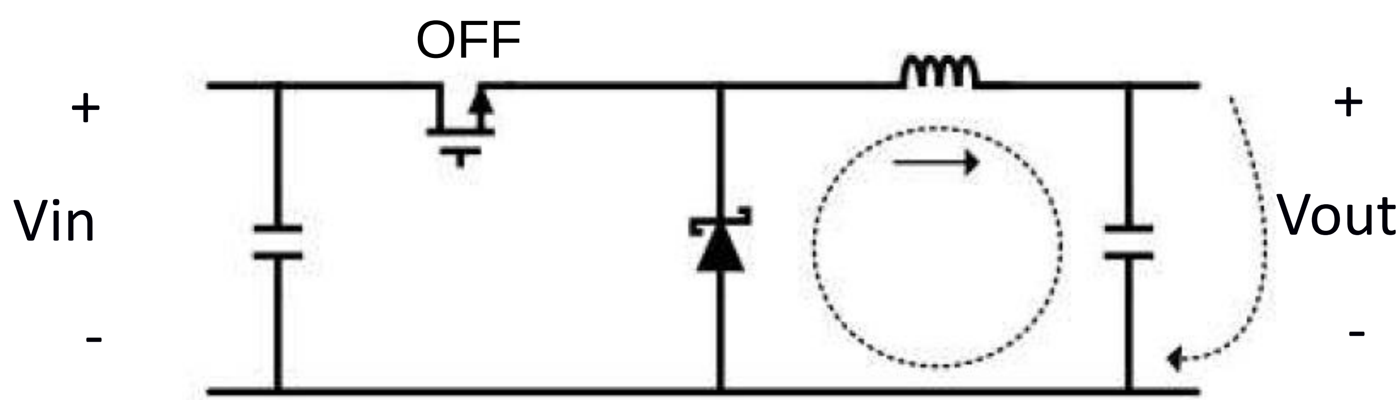




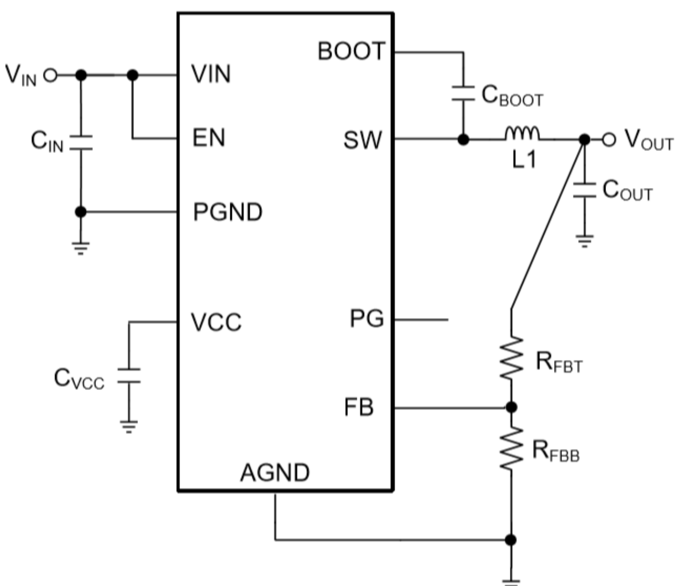
https://en.wikipedia.org/wiki/Buck_converter

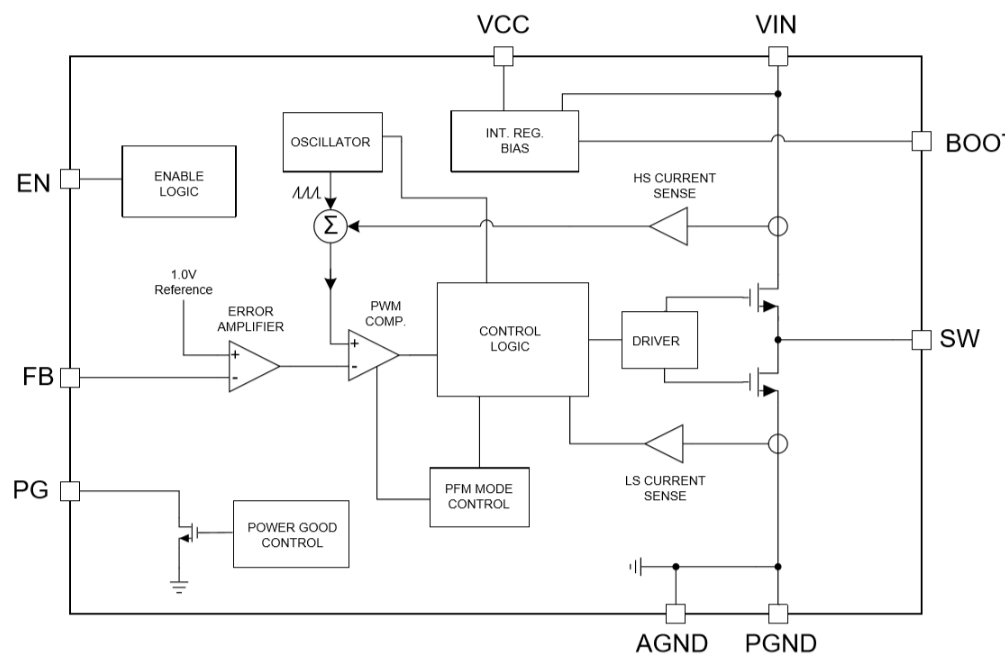
Buck Voltage Convertor





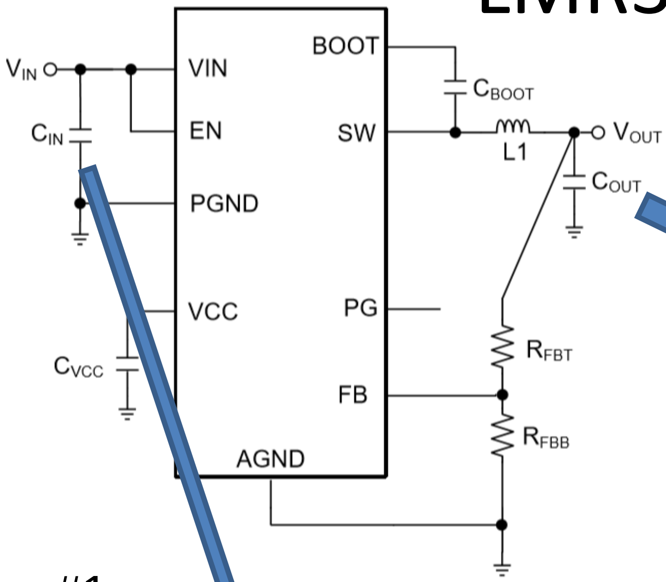
LMR33630 Buck Converter

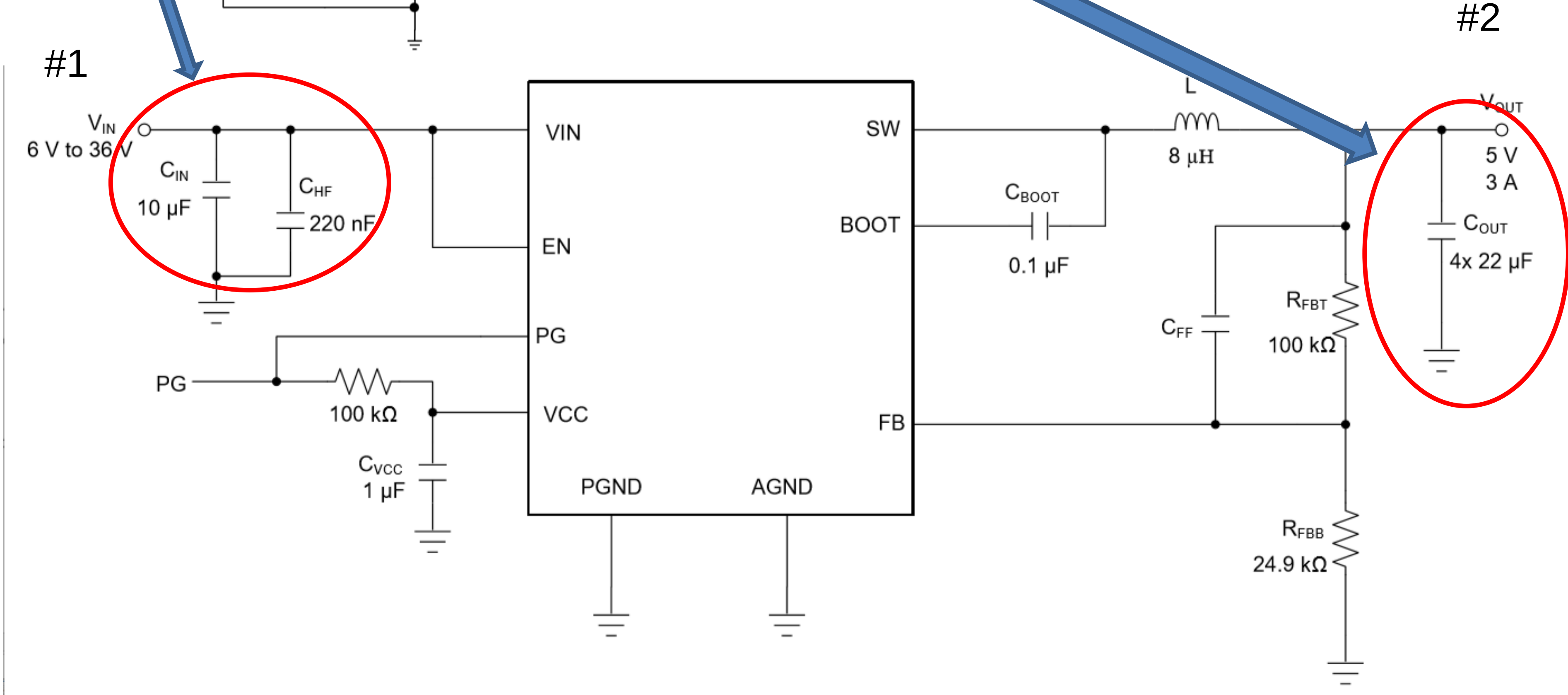




LMR33630 Buck Converter

… multiple capacitors can be used in parallel to bring the minimum effective capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor.





Buck Converter Waveforms

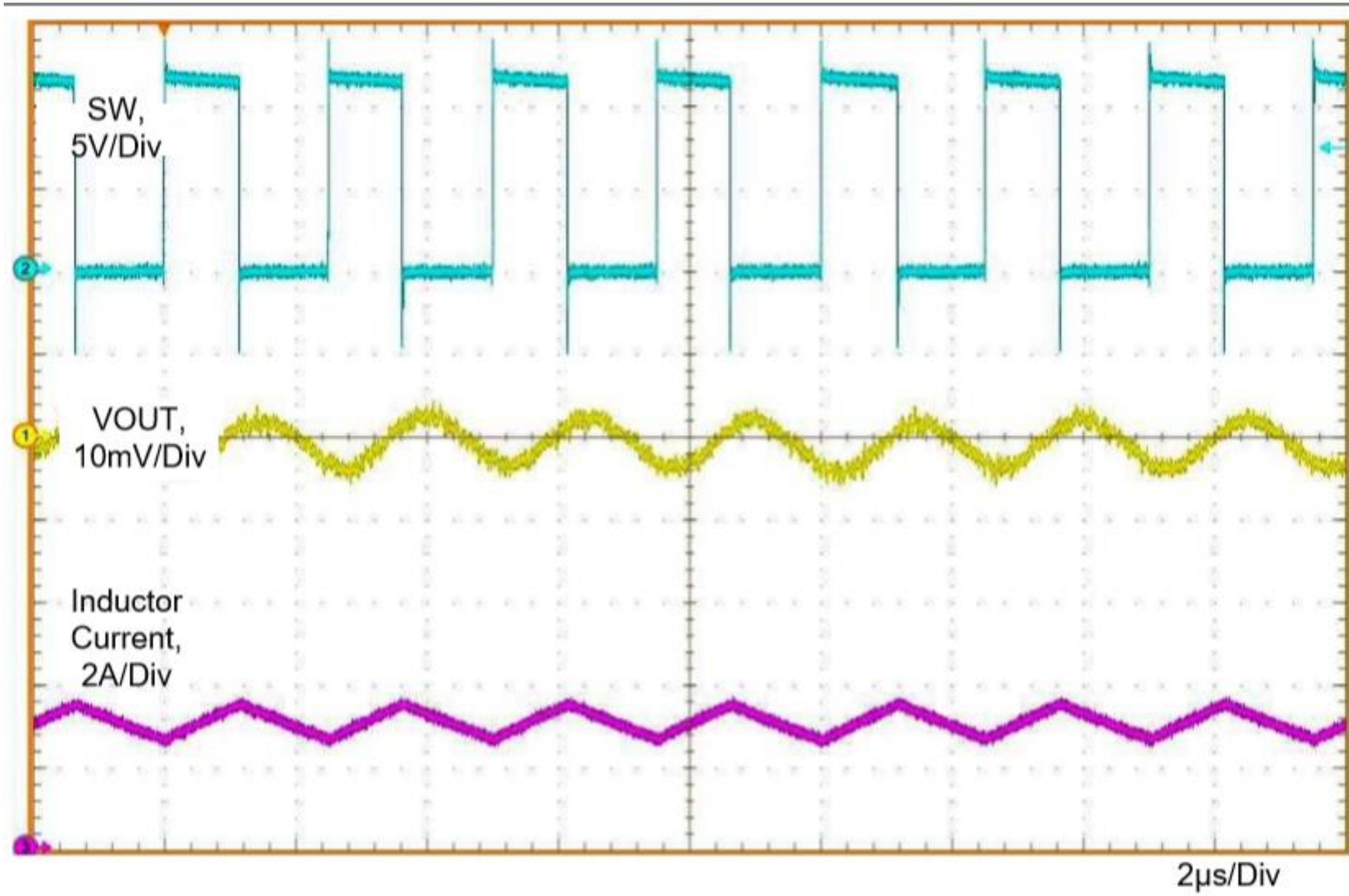
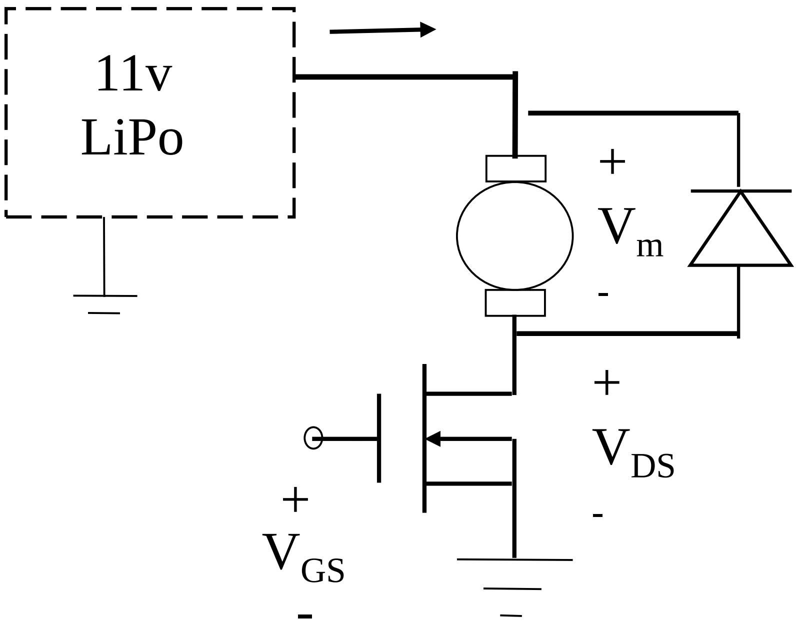


Figure 14. Typical PWM Switching Waveforms
V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3 A, f_S = 400 kHz

Extra Slides

Wiring Notes: caution on Vgs



On board

Watch out for voltage drop in wires/PCB traces.
#22 wire: 50 mOhm/m
#12 wire: 5 mOhm/m

Summary

- Wiring to prevent high Vgs
- Wiring to prevent high current through low power devices
- Linear regulator
- Buck converter