Time-Resolved Optical Characterization of Electrical Activity in Integrated Circuits

JAMES C. TSANG, SENIOR MEMBER, IEEE, JEFFREY ALAN KASH, SENIOR MEMBER, IEEE, AND DAVID P. VALLETT, MEMBER, IEEE

Invited Paper

If the rate of improvement in the performance of advanced silicon integrated circuits is to be sustained, new techniques for the measurement of electrical waveforms in operating circuits are needed. Critical factors dictating this requirement include the increased speed and complexity of circuits, the growing importance of faults that appear only during high-speed operation, and the use of flip-chip packaging technologies. Two recently developed all-optical methods for measuring the switching activity from the backside of a chip are described and compared. One is a passive approach based on the measurement of hot carrier luminescence emitted from the channel of a CMOS field-effect transistor (FET) during switching. The second uses a laser probe to sense the switching induced modulation of the silicon optical constants near an FET's source and drain.

Keywords*—*Failure analysis, integrated circuits, optical characterization.

I. INTRODUCTION

It is becoming more and more difficult to locate and diagnose faults and failures in state-of-the-art integrated circuits (ICs). Many of the advances in chip technology [1] needed to allow ICs to keep up with Moore's law [2] today and in the near future pose major problems for measurements of chip operation at the level of the individual field-effect transistors (FETs). This has been an important part of the rapid debug of aggressive new designs and process technologies and the fast analysis of field returns, which are both required for success in today's highly competitive marketplace.

Failure to develop physical analysis tools matched to the new aspects of advanced chips can threaten the successful introduction of these ICs [3]. New features include the increasing number of wiring layers, growing importance of interconnects and timing failures in limiting high-speed performance, use of flip-chip packaging, ever smaller device sizes, and use of internal clock speeds exceeding the input–output (I/O) bandwidths. The lack of direct physical access to the electrically active parts of a chip due to the wiring on top of it and the use of flip-chip packaging severely limits the effectiveness of failure analysis tools, which require direct physical access to signal lines. At the same time, the advent of gigahertz clock speeds increases the likelihood of "at speed" failures, which can only be diagnosed during high-speed operation. Finding such failures places severe demands on the loading a probe system can impose on a node, or the bandwidths of the I/Os of a chip.

These challenges have led to research to develop noninvasive high-frequency methods for the measurement of switching in the individual devices of modern digital ICs. In this paper, we describe a major thread of this effort: the development of optical tools that can measure switching in a circuit from the backside of the die on which it was fabricated. Optical tools fulfill the requirements of submicrometer spatial resolution, time resolution of signals at the picosecond level, and imaging through silicon substrates, which are transparent at infrared wavelengths. Such techniques make use of the large intellectual and technical infrastructure that has been assembled over the past two decades for picosecond optical measurements. We show that the critical technologies are all commercially available so that the construction of these tools does not require the creation of new technologies.

In this paper, we concentrate on two different techniques for use in diagnostic and test laboratories. The first is a passive approach based on the measurement of the weak luminescence generated by hot carriers in CMOS FETs [4], [5]. The second is an active approach based on the modulation of the reflection of a probe laser beam by changes in the voltages at interfaces in Si [6]–[8]. We do not discuss test and debug techniques, which involve the implementation of

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J. C. Tsang and J. A. Kash are with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: jtsang@us.ibm.com; jeffkash@us.ibm.com).

D. P. Vallett is with the IBM Microelectronics Division, Essex Junction, VT 05452 USA (e-mail: dvallett@us.ibm.com).

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test methodologies on a chip through self-test modules [9], software or tester-based approaches to fault localization, or deliberately invasive optical techniques, which use light to perturb a circuit and observe the light-induced changes in its electrical behavior. The last has been reviewed recently by Barton *et al.* [10].

We begin with a summary of anticipated changes in integrated circuit technology and how traditional methods of detecting faults and failures in ICs will become ineffective as these new solutions are widely adopted. The advantages of optical approaches in solving this problem are explained. A review of how light interacts with carriers in Si ICs provides a set of common terms for the description of the physical processes that underlie our two approaches. We describe both the passive hot carrier luminescence technique (called picosecond imaging circuit analysis, or PICA) and the active laser probe technique (called laser voltage probe, or LVP), including their physical origins and the measurement technologies required for their implementation. We present experimental results on working ICs obtained by both techniques and consider the existing limitations of both, the possibilities of future improvements and applications, and how they can be integrated with other hardware- and software-based approaches.

II. Transistor-Level Diagnostics and Test in Twenty-First Century ICs

The SIA "International Technology Roadmap for Semiconductors: 1999 Edition" [1] provides an informed view of coming changes in IC technology: Table 1, extracted from the 1999 Roadmap, shows some predictions. From Table 1, we infer that by 2005, a laboratory tool measuring switching transients from digital ICs will need to be able to resolve devices spaced by less than 0.5 μm, place switching edges with an accuracy of 10 ps, do so in devices with an area of about 0.1 μm^2 operating at voltages between 0.9 and 1.2 V, and efficiently obtain data over millions of devices.

Implied in Table 1 is the importance of "at-speed" testing. The high speeds of modern ICs necessitate picosecond-level accuracy in the timing of signals. Both the optimization of performance and the detection of faults in future ICs will require the measurement of switching events with a time resolution of 5–10 ps. At-speed testing on this time scale poses formidable challenges to electrically based diagnosis techniques, which work through the chip I/O pads. It will be difficult to obtain enough information from the few thousand chip I/Os, whose bandwidths are on the order of 100 MHz, to find timing failures due to a few gates in a gigahertz frequency chip with tens of millions of gates.

Table 1 predicts that microprocessors will have eight to nine layers of wiring and that the number of I/Os will exceed 3000. Unmentioned in Table 1 but critical here is the increasing presence of dense metal fill patterns, in areas of the chip not used by signal or power leads, to optimize the chemical-mechanical polishing processes needed to planarize the multilayer wiring structures. The "front" side of the chip,

Table 1
Projected, Selected Characteristics of CMOS Technology over the Next 11 Years as Presented in the "International Technology Roadmap for Semiconductors: 1999 Edition." All Characteristics Are for High-Performance Microprocessors Except for the Clock Jitter, Which Is a Requirement for High-Performance ASICs [1]

Year	1999	2001	2005	2011
MPU Gate Length	140 nm	100 nm	65 nm	30-32 nm
On-chip clock	1250 MHz	1767 MHz	3500 MHz	10000 MHz
RMS Clock Jitter	27 psec	16 psec	9.5 psec	3.3 psec
Number Wiring levels	6-7	7	8-9	9-10
Chip Size (mm^2)	340	340	408	536
Transistors per Chip	23.8 M	47.5M	190 M	1523 M
Logic Transistor Density per cm^2	6.6 M	13 M	44 M	269 M
Voltage Range	1.5-1.8 V	1.2-1.5 V	0.9-1.2 V	0.5-0.6 V
Number of Chip I/O's	2304	3042	3042	4224

where the FETs and the wiring that connect and power them are located, is now and will continue to be covered by metal. Direct physical access to the devices and the lower wiring layers from the front side will be impossible without physically removing part of the front surface and making the IC inoperable. The 3000 or more I/Os in Table 1 cannot be supported by contact pads lining the edge of a future chip. This, and requirements for cooling and the uniformity of power supply and ground voltages across a chip, have led to the use of flip-chip packaging, where the front surface of the chip is covered by a grid array of contacts and the chip is mounted front side down on a carrier. This geometry is shown in Fig. 1 [3]. In a "flip-chip" package, the backside of the Si substrate is "over" the front side, severely constraining physical access to the FETs and wiring.

The need for "at-speed" gate-level test and diagnostics in contemporary ICs has been surveyed in two recent *IEEE Spectrum* articles [3], [9]. Vallett and Soden [3] discuss approaches where the electrical waveforms in circuits are measured. This can be done through metallic probes, which physically contact metal lines to measure their voltages. Conventional metal probes are capable of contacting lines on the order of 0.5 μm, while smaller probes are being developed based on the scanning probe microscope. Such probes have been used at frequencies as high as 2 GHz. A focused beam of electrons can also be used as a probe of metal lines [11]. If the sample is in vacuum so that the electrons can physically interact with the metal, the electron beam excites "secondary" electrons. The excitation process is sensitive to the voltage at the metal surface. By analyzing the kinetic energy distribution of the secondary electrons, the relative voltage of the metal can be determined. If the electron beam is pulsed, analysis of the energy of the secondary electrons gives the voltage during the pulse. Measurements of time-varying signals at 50 GHz have been reported. The electron beam is derived from an electron microscope so that submicrometer dimension metal lines can be resolved.

Both multiple metallization layers and flip-chip packaging pose major challenges to the above techniques. If the metal

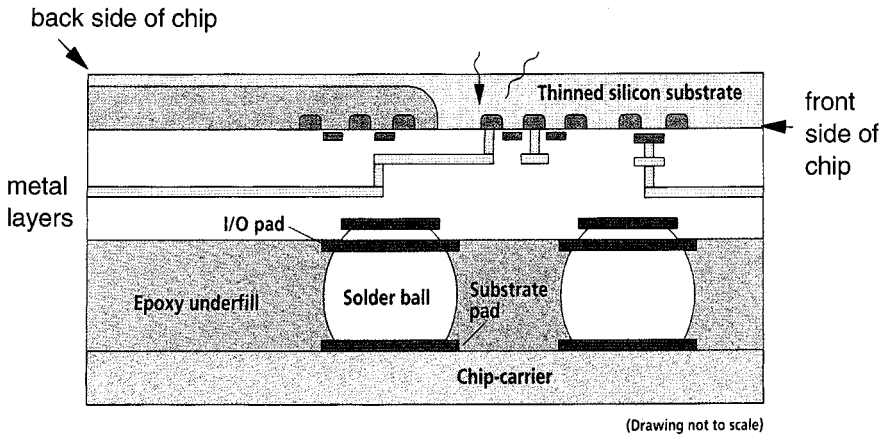

Fig. 1. Schematic of the cross section of a modern silicon integrated circuit showing multiple layers of metallization, solder balls for flip-chip packaging, and defining the front and back sides of the chip [3].

line of interest is buried under other metal lines and insulators and/or is covered by the substrate in a flip-chip package, use of probe and e-beam require "deprocessing" of the chip. A focused ion beam (FIB) tool can "drill" to a metal line of interest from the front or backside of an IC [3]. Lines so exposed can be probed directly with the electron beam or through the deposition of a test point that can be used with either probing technique. However, FIB is slow, and access is not universal, as target locations are often obscured by other lines or transistors. FIB can also alter the electrical properties of metal lines and transistors in the area of interest. Furthermore, these probing techniques require signals to be acquired in a serial fashion. For complex debugging efforts with little *a priori* understanding of the problem, serial probing can be prohibitively time-consuming.

Before we narrow our focus to two specific optical methodologies for backside testing of advanced ICs, we briefly mention several other methods of remotely sensing circuit activity to better appreciate the constraints imposed by modern IC technology on efforts to measure circuit activity. These involve 1) electromagnetic; 2) magnetic; 3) thermal; and 4) acoustic measurements [12]. We also mention the concept of built-in self-test systems [9].

High-speed ICs radiate electromagnetic waves. The spectrum of this radiation can be measured, and structure has been observed at frequencies corresponding to the I/O and gate switching times [13]. While this emission has the bandwidth to characterize operating ICs, it lacks spatial resolution. The emission wavelengths are on the order of millimeters, and it will be difficult to localize anomalies on the micrometer scale. While the diffraction limit has been exceeded at microwave wavelengths by near-field optical techniques [14], the presence of flip-chip packaging means that the source-aperture distances will be on the order of 100 μm or greater, reducing the spatial resolution of a near-field probe.

Currents in an IC generate magnetic fields. Superconducting quantum interference devices (SQUIDs) can detect very small magnetic fields. A commercial instrument [15] can detect currents on the 10 nA scale to localize a current source to a 30-μm region and has observed current faults from the front side in dc biased ICs. SQUIDs have detected time-varying radio-frequency fields at 50 MHz [16], [17]. However, in the absence of a method for imaging magnetic flux at the submicrometer level onto a SQUID, and for a flip-chip IC operating at 1 GHz, with a 100-μm-thick substrate, the spatial resolution of a SQUID detector will be unable to resolve an anomalous time-varying current from a single gate surrounded by normally switching gates.

Acoustic waves are widely used to image buried structures [18]. Any interface in a solid can scatter a sound wave, providing the basis for imaging the interface. Spatial resolution of a few micrometers, several hundred micrometers below a surface, is possible with acoustic waves. While a physical interface between two materials is a strong contrast mechanism, the switching of an FET with the introduction of a thin layer of charge under a gate layer produces little contrast. Therefore, acoustic imaging is not very sensitive to electrical activity.

Logic gates in a CMOS IC generate heat whenever they switch states. The detection of this thermal signal can show circuit activity [19]. However, in Si, the thermal wavelengths and time constants make it difficult to temporally resolve on the scale of a micrometer or less, small temperature changes at rates greater than a few hundred kilohertz [7]. For flip-chip packages, the power dissipation at the device layer occurs hundreds of micrometers below the backside, and back surface measurements of the internal temperature will be unable to resolve the source of the heat to better than a few tens of micrometers. Further, overall power dissipation of ICs will increase over time, making it more difficult to sense an individual thermal signal against the large background.

The incorporation of built-in-self-tester (BIST) circuitry in a chip was recently discussed by Zorian [9]. Such additional circuitry means that the normal I/Os of a chip need not be used to localize and characterize faults in individual transistors. However, typical BIST provides little if any information at the transistor level, certainly not analog waveforms for individual devices. Further, a critical parameter in this solution is economic since it requires additional silicon to implement the test circuitry. This reduces the number of chips that can be obtained from a wafer. Such extra structures will also affect design costs, manufacturability, and yield.

Several common themes characterize the above discussions. One is the need to image the device plane or project a probe onto the device plane. Other requirements include adequate spatial and temporal resolution. Methods that provide adequate resolution can fail if the interaction between the probe and the electrical waveform is so weak that the resulting signals cannot be readily detected. Finally, once a chip achieves production, diagnostic capability is required only on failing chips, usually a tiny fraction of all chips. As such, there is strong pressure to minimize the burden of any built-in diagnostic infrastructure.

As a result, several optical tools have been recently developed to measure circuit activity. The advantages of optical methods for the identification of gate-level problems in ICs are summarized in Table 2. Undoped Si is transparent at wavelengths longer than 1.2 μm [20], [49], [50]. Even when Si is doped n or p at 10^{18} cm^{-3}, its absorption length near 1 μm is always greater than 100 μm. It has been shown [3], [8], [10] that flip-chip substrates can be thinned and polished to between 100 and 200 μm thickness, and the chips operated normally. Therefore, backside optical measurements are practical from ICs fabricated on standard substrates. The spatial resolution of 1-μm wavelength light is about 0.7 μm. Because of the large dielectric constant of Si, resolution can be improved to $\sim$0.14 μm with solid immersion lenses [21]. There is a good understanding of the interaction of electric fields with light in Si. These include the modulation of light by applied fields and the presence of luminescence due to energetic carriers in FETs. Several common optical techniques can temporally resolve such signals on the picosecond time scale. Optical techniques do not affect the front side cooling of flip-chip parts through their contacts and allow chips to be exposed to flowing cold gases to provide backside cooling, or attached to heat-sunk infrared (IR) transparent solids, compensating for the removal of normal heat sinks for the measurements.

III. Electronic and Optical Properties of Silicon

The electronic and optical properties of silicon-based devices are explained by the electronic band structure of Si. Fig. 2 shows the band structure of Si near its fundamental energy gap. The basic feature of the band structure is its indirect energy gap (a) of about 1.12 eV at 23 °C. The indirect gap means that the absorption in Si increases slowly with increasing energy as compared to direct bandgap materials [20], [49], [50], [22]. The lines b–e represent other types of transitions that can occur in Si and will be discussed later. The penetration depth of light in Si is about 100 μm at 1.3 eV (wavelength of $\sim$950 nm). Light of this wavelength or longer can penetrate hundreds of micrometers into Si, allowing the imaging of devices through the backside at these thicknesses [20], [49], [50].

During the operation of an IC, the distributions in energy and space of carriers in the channels of the FETs change as the logic gates switch states. The electric fields defining the source and drain of an FET also perturb the electronic states near the local band edges. This paper is about how light can be used to measure these switching induced changes near the band edges of Si. In the following sections, we qualitatively describe 1) the mechanism by which light is emitted by hot carriers in FETs and 2) how the reflection of an IR laser beam from an FET can be modified by its electrical state. More detailed treatments follow in Sections IV and VII.

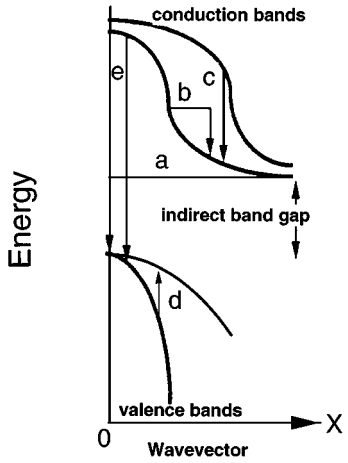

Fig. 2. Near band edge bandstructure of silicon showing the indirect band gap and several possible hot electron transitions.

A. Hot Carrier Light Emission from FETs

An applied electric field increases the energy of a carrier in Si through Joule heating. Classically, if the electric field is E, then the kinetic energy increase of a carrier in the field is just eEd, where e is the charge and d is the mean free path through which the carrier moves in the electric field between scattering events. When the mobile carrier scatters from lattice vibrations, impurities, or other carriers, it loses this extra kinetic energy and will start drifting in the field again. Mean free paths in Si are typically a few hundred angstroms. An electron in the conduction channel of a silicon nFET subject to an electric field of about 10^5 V/cm can acquire about 1 eV of kinetic energy over the distance of a mean free path [23]. One result of this heating is that states of the conduction band that are unoccupied in the absence of an applied field can become occupied. These include states above the bottom of the lowest lying conduction band in Fig. 2 as well as the higher conduction band. These new filled states introduce the possibility of light-emitting transitions to lower lying empty states of the conduction band. Similarly, holes in the conducting channel of a pFET can be heated by the electric field to a more energetic state and then emit a photon by making a transition to an unoccupied, less energetic, valence band state. In the absence of lattice vibrations and impurities, these transitions must be to states with the same wave vector. In the presence of lattice vibrations and impurities, indirect transitions involving different wave vectors are allowed. Regardless of these details, the emission of light by mobile hot carriers in saturated FETs is a well-established experimental fact [24]–[27]. The flux of visible or near-infrared emitted photons from an FET in saturation is small, though easily detectable with photon counting detectors [4], [5].

Table 2
Summary of the Advantages of Optical Probes of Electrical Activity in Current and Future Si-Integrated Circuits

Ideal Probe Properties	Optical Probe Properties
Insensitive to overlayers and substrates, and does not affect normal removal of heat from working chip	Optical Probes: a. penetrate >1mm of undoped Si at 1.3 μm, b. penetrate ~0.1mm of undoped Si at 0.9 μm, c. penetrate ~0.1mm doped Si at 1.1 μm, (a-c. are compatible with flip-chip packaging), d. require substrate polishing to optical finish for imaging, e. require removal of heat sink but contact side heat sinking remains and exposed side can be cooled by flowing gases and transparent heat sinks.
Does not perturb circuits in chip	a. PICA uses intrinsic emission and does not load devices. b. LVP uses above band gap light with weak loading, or c. sub-band gap laser probe and negligible loading.
Can spatially resolve individual gates	a. using normal optics, resolve ~0.75 μm spacings. b. using solid immersion lens, resolve~0.17 μm. c. can centroid peaks to 0.1 μm for temporally distinct peaks.
Can temporally resolve switching transitions	a. PICA capable of 100 psec instrumental FWHM and 5 psec centroid location. b. LVP capable of 35 psec time resolution.
Can measure logic states of gates	PICA and LVP can determine logic states from circuit layouts and AC waveforms.
Full chip coverage and gate level resolution	a. PICA can image full chip with reduced spatial resolution. b. Both are capable of diffraction limited spatial resolution.

B. Field and Charge Modulated Optical Responses

Light incident on Si generates a time-varying polarization of the carriers in the valence and conduction bands. The polarization field can be derived from the long wavelength dielectric response function or the complex index of refraction, which [22] can be calculated from the band structure in Fig. 2 or derived from measurements of the transmission and reflectance of Si. The behavior of the response function near 1 eV depends on the density and type of carriers in Si, since they can change the positions of the filled and empty band edge states that interact with the light. It also depends on the strength of any applied electric field near the surface. Applied voltages at a silicon interfaces modify the energies of the filled and empty states at the band edges and perturb the wave functions of the states contributing to the dielectric function. Such voltages can also change the populations of the free carriers in the bands by depleting or inverting a doped region. The dependences of the optical response of Si on doping and applied electric fields include a voltage-induced modulation of the density of free carriers at the probe beam, an electric field-induced shift in the bandgap of the semiconductor, and electric field-induced changes in the matrix elements, which connect the filled and empty states of the band structure in Fig. 2. For common modulation amplitudes, the intensity of the modulated reflectivity is usually four to six orders of magnitude weaker than the unmodulated reflectivity. There are also many second-order contributions associated with, for example, local heating by currents in devices, which can change the bandgap of the sample. There are many articles about the experimental modulation of the optical response of Si by applied voltages and currents, including the dependence on the amplitude of the applied fields, as well as the methodology for the detection of these small signals [22]. For the device structures of interest in modern ICs, several different mechanisms can contribute to the signals generated by the voltage waveforms.

C. General Experimental Considerations

The optical detection of the above phenomena present complementary experimental challenges. The hot carriers generated in a current carrying, saturated FET, appear at locations in the band structure where none had previously been. There are generally few hot carriers, and the efficiency of their coupling to light is weak. Therefore, the intensity of any optical emissions from these carriers is small. However, in most cases, the intensity of any background emission from the silicon FET is negligible, so that the experimental challenge for PICA is the detection of a small, background-free light pulse with the duration of the switching time of the FET.

For LVP, where FET activity is monitored by measuring changes in the reflection of a light beam, there is always a background signal due to the normal reflections at the interfaces of the device. Since switching-induced modulation of the reflected light is between one to ten parts-per-million, the measurement of switching in an integrated circuit by this method involves the high bandwidth detection of a small time-varying signal against a large static background.

Measurement systems capable of detecting hot carrier light emission from CMOS gates, or using a laser to observe the modulation of the local optical constants of an IC by the switching of its gates, can readily obtain images of the physical circuits. In the former case, external infrared illumination of the chip will produce an image of the layout of the chip on the detector used to image the hot carrier

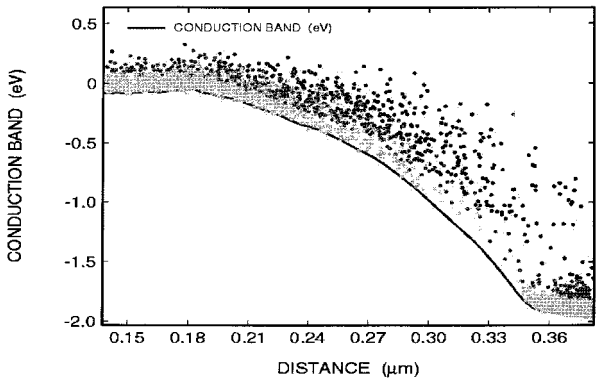

Fig. 3. Dependence on position in the channel of the conduction band energy and the kinetic energy of electrons in a 0.15-μm nFET for $V_{\rm DD} = 3.4$ V, $V_{\rm GS} = 1.0$ as derived in a Monte Carlo simulation [23].

emission. This can be directly registered to the hot carrier emission detected by the camera. In the latter case, the probe laser beam can also be used as part of a scanning laser microscope to produce an image of the circuit, which can be registered to the waveforms obtained by the laser voltage probe.

IV. Hot Carrier Emission Effects in FETs

We now quantitatively consider hot carriers in FETs and their detection.

A. Theory

When a FET is conducting, there are free electrons (or holes in a pFET) in the channel. These carriers have a distribution of energies which depend on the applied fields, sample temperature, type of device, etc. Ordinarily, this distribution is the Maxwell–Boltzmann distribution, where the probability that a carrier has kinetic energy U is proportional to $\exp(-U/kT_E)$. T_E is the effective temperature of the distribution and k is the Boltzmann constant. Typical values of T_E for electrons in the high field regions of saturated submicrometer length FETs are between 2000–3000 K, giving rise to the use of the word "hot" to describe the carriers. The host lattice of Si atoms remains near the ambient temperature. Under high field conditions, energy can be given to the free carriers by the local fields faster than it can transferred to the lattice from the carriers. Therefore, the carriers and the lattice can have different temperatures.

The energy distribution of carriers in FETs under normal operating conditions can be theoretically derived. Fischetti *et al.* [23] calculated the energy distribution of electrons in a saturated, deep submicrometer Si nFET (0.15-μm effective channel length, 0.25-μm metallurgical channel length, $V_{\rm ds} = 3.4$ V and $V_{\rm gs} = 1.0$ V). The calculated dependence of the average electron energy on the position in the channel is shown in Fig. 3. This figure was the result of a Monte Carlo calculation and shows the energy of the conduction band as a function of position between the source and the drain. The dots above the conduction band energy show the energies of test particles in the channel under the above bias conditions. The electrons in the low field part of the channel within 0.1 μm of the source ($x < 0.20\,\mu$m) have an excess energy of less than 0.2 eV and are described by $T_E < 3000$°K. The highest fields exist between the end of the pinched-off channel and the drain ($0.27 < x < 0.35\,\mu$m) when the nFET is in saturation, and there are "hot" carriers with kinetic energies over 1 eV. Significant near-infrared and visible light emission, which involve carriers with more than 1 eV of kinetic energy, is only generated in the pinch-off region of the FET in saturation. The calculations of Fischetti *et al.* [23] determine the energy distribution of carriers in the channel even if the distribution is nonthermal. For electric fields below 10^5 V/cm, electrons are generally characterized by a Maxwell–Boltzmann like distribution for higher kinetic energies. For higher fields, near 10^6 V/cm, nonthermalized distributions, with some evidence for ballistic behavior, are obtained.

Several different types of optical transitions involving thermalized or nonthermalized carriers can produce infrared and visible light emission from FETs. The quantitative theory of how hot carriers can emit light in FETs has been considered by many groups [24]–[27]. These theories require the calculation of the hot carrier distribution and the matrix elements for transitions involving the hot carriers. The calculated distributions have generally been similar. Controversy exists over the quantitative details of the optical transitions. Possible mechanisms are intraband processes where momentum conservation is satisfied by the presence of defects or the participation of phonons ("b" in Fig. 2), momentum-conserving direct transitions between the higher and lower conduction or valence bands ("c" and "d" in Fig. 2), and direct conduction to valence band transitions (e). In all cases however, the hot carrier emission is weak, the radiative events being a tiny fraction of the phonon dominated relaxation processes. Because the densities of states and matrix elements vary slowly with energy, the photon energy dependence of the hot carrier emission is the same shape as the carrier distribution. For thermalized hot carrier distributions, the spectra will be Maxwell–Boltzmann-like, characterizable by a T_E. The conduction to valence band recombination processes in Si are not detectable in FETs since the required minority carrier densities are miniscule.

Hot carrier distributions relax or "cool" by the emission of phonons. Such processes are characterized by scattering times on the 0.1 ps time scale. If the applied fields producing hot carriers suddenly vanish, hot carrier distributions relax to the lattice temperature in a few picoseconds [4]. Since the applied voltages in present day FETs change over times greater than this, the hot carrier distributions and the associated light emission respond essentially instantaneously to voltage changes in FETs. The hot carrier distributions and light emission reflect the instantaneous electrical state of an FET in a circuit on the picosecond time scale. This is different from the normal interband electron-hole recombination processes, which are much slower.

The above discussion did not make any distinction between hot electrons and hot holes. Both have the same electric charge and experience the same force under an applied

field. On the other hand, the hole mobilities in Si are half that of the electrons. As a result, for the same electric field, holes gain less energy before scattering than electrons. The temperature of a hot hole distribution in a pFET will be lower than the electron temperature in a comparable nFET. This lower temperature means that the optical emission from pFETs is typically more than an order of magnitude weaker, though still detectable, than from nFETs for similar bias voltages [27]–[29].

For a given device geometry, the intensity of the emission will increase with increasing voltages, which produce increased electric fields and currents [5]. While the operating voltages in modern ICs decrease with decreasing device sizes, the scaling used to produce new generations of chips either keeps the device electric fields constant or allow the electric fields to increase [30]. Since the density of hot carriers depends exponentially on the electric fields near the drains of FETs, the intensity of the emission per carrier in the channel should remain constant or increase with decreasing device size. Decreases in device sizes will produce decreases in the number of hot carriers due to the decrease in the channel current during normal operation. The combination of the exponential dependence of the hot carrier emission intensity on electric fields in the devices and the linear dependence on the device geometry suggests that hot carrier emission processes will not become less efficient as smaller and smaller devices come on line, as long as traditional scaling practices continue [30].

B. Static Hot Carrier Luminescence in Silicon FETs—Experimental Results

Both n- and pFETs in saturation emit detectable near infrared light due to hot carrier effects [24], [28], [29]. The intensity of the nFET emission $I_{\rm NFET}$ has been shown to be a strong function of the source to drain voltage $V_{\rm DS}$ and the gate voltage $V_{\rm GS}$, consistent with theory. For fixed $V_{\rm DS}, I_{\rm NFET}$ shows a peak near $V_{\rm GS} = V_{\rm DS}/2$ [28]. If $V_{\rm DS}$ changes while the density of the carriers in the channel is kept constant, $I_{\rm NFET}$ increases exponentially with $V_{\rm DS}$ [24], [27]. The measured spectrum of $I_{\rm NFET}$ is Maxwell–Boltzmann-like [10], [24], [27], [31]. The measured pFET emission intensity is typically only about 2% of that from a comparable nFET. These experimental results all agree with the theory of hot carrier emission in silicon FETs [24], [25], [27]. Most of the picosecond imaging circuit analysis (PICA) data to be discussed in this paper will concentrate on nFET emission because of its greater intensity.

C. Switching-Induced, Pulsed Hot Carrier Light Emission from CMOS Logic Gates

In CMOS circuits, nFETs and pFETs are combined to perform different logical operations [30]. Because of its complementary character, under static (dc) conditions when the gate voltage $V_{\rm GS}$ is either zero or $V_{\rm DD}$, only the subthreshold leakage current runs through a CMOS logic gates. The low leakage current means there is no detectable emission from well-designed, properly fabricated CMOS circuits under dc conditions since detectable amounts of light require larger currents.

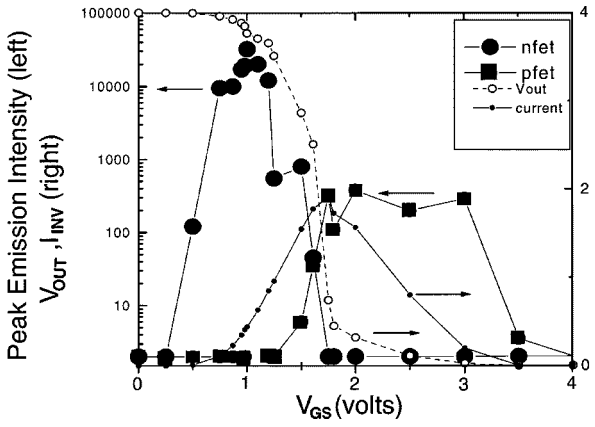

Fig. 4. Dependence of $V_{\rm OUT}, I_{\rm DD}$, nFET emission intensity, and pFET emission intensity on $V_{\rm GS}$ for a simple CMOS inverter.

In contrast, when a conventional CMOS logic gate changes state, current exists. This produces transient light emission. Tsang and Kash [4], [5] used this transient hot carrier emission to study intrinsic time-varying behavior in silicon CMOS circuits. The analysis of the current voltage characteristics of a CMOS inverter during switching can be found in any CMOS textbook [30]. When the gate or input voltage $V_{\rm GS}$ of an unloaded inverter is swept from ground to $V_{\rm DD}$, there are a range of values of $V_{\rm GS}$ when both nFET and pFET are conducting, and a "short circuit" current runs from $V_{\rm DD}$ to ground. Linear behavior of an nFET with the pFET in saturation, both n- and pFETs in saturation, and linear behavior by the pFET with the nFET in saturation are all observed as a saturating logic CMOS inverter switches. For both transistors, as $V_{\rm GS}$ switches, $V_{\rm GS} = V_{\rm DS}/2$ for a brief period. This gate voltage condition produces maximum optical emission from the FETs [28]. As a result, optical emission from hot carriers is expected from both the nFET and the pFET of an inverter. In Fig. 4, we show the $V_{\rm GS}, V_{\rm OUT}$, and $I_{\rm INV}$ characteristics of a simple inverter as $V_{\rm GS}$ is slowly varied from zero to $V_{\rm DD}$ so that $V_{\rm OUT}$ goes from $V_{\rm DD}$ to zero. We also show the measured intensity of the light emission from the nFET and the pFET during the switching. No emission is observed when either the n- or pFET are cut off. Light emission is observed from the nFET during the first half of the transition as $V_{\rm OUT}$ begins to drop and $V_{\rm GS}$ approaches $V_{\rm DD}/2$. Light emission is observed from the pFET during the second half of the transition as $V_{\rm OUT}$ goes from $V_{\rm DD}/2$ to zero, and the pFET is in saturation. Thus, observation of the emissions from the pFET and nFET can be combined to trace out both the start and the end of the switching transition. Current and planned CMOS circuits are characterized by gate to gate delays between about 10 and 50 ps. The rise and fall times of these gates track the gate to gate delays [30]. The nFET emission from a simple inverter for a $V_{\rm OUT} = V_{\rm DD}$ to zero transition occurs during the initial rise of the input waveform so that the switching-induced light pulse will have a width of less than half the rise time of the gate.

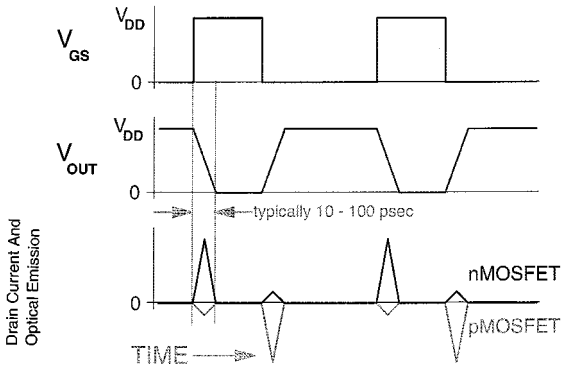

Fig. 5. Schematic of the relationship between electrical and hot carrier induced optical emission waveforms for a CMOS inverter.

The above discussion was for an unloaded gate. In a functional chip, a logic gate drives downstream circuits. The load generated by these circuits, due to the metal lines and gates of the downstream logic, is largely capacitive. For an inverter driving a capacitive load, the output voltage cannot instantaneously follow changes in the input voltage. Then, for example, $V_{\rm GS}$ can reach $V_{\rm DD}/2$ while $V_{\rm OUT}$ is still at $V_{\rm DD}$. For a transition where $V_{\rm OUT}$ goes from $V_{\rm DD}$ to zero, pFET emission will be weaker than for the unloaded inverter (or may not occur at all) if a voltage drop is developed across the pFET only after the pFET is turned off. Also under this situation, the nFET emission can be significantly stronger than for the unloaded inverter. In contrast to the unloaded inverter, current will pass through the nFET even after the pFET is turned off, supplied by the charge stored on the load. The presence of the load increases the amount of emission from the nFET during a $V_{\rm OUT} = V_{\rm DD}$ to zero transition. The pFET emission remains solely due to the short circuit current. For a $V_{\rm OUT} =$ zero to $V_{\rm DD}$ transition, however, the opposite situation occurs, and there can be strong, load-driven pFET emission [4], [5].

In summary, for either loaded or unloaded CMOS logic gates, switching transitions generate optical emission from hot carriers. The timing and relative strength of the emission is shown schematically for a simple inverter in Fig. 5. The dominant emission will be associated with nFETs undergoing $V_{\rm OUT} = V_{\rm DD}$ to zero transitions. The presence of current in the n- and pFETs is necessary for observable light emission but does not guarantee it since the presence of hot carriers in an FET depends on both the source-to-drain voltage and the gate voltage.

Fig. 6 shows an example of optical emission from an operating CMOS ring oscillator over a 200 $\times$ 400 μm field of view. The oscillator consists of an odd number of inverters (47 gates where one of the 47 is a NAND gate with one dc input at "1"), laid out in four connected rows. The effective channel length of the FETs is 0.6 μm. The normal operating voltage is 3.5 V and the gate-to-gate delay is $\sim$100 ps. The normal operation of the ring oscillator consists of the continuous sequential switching of the inverters around the ring. The ring oscillator drives a divider circuit, which produces an electrical output once every 32 cycles of the ring oscillator.

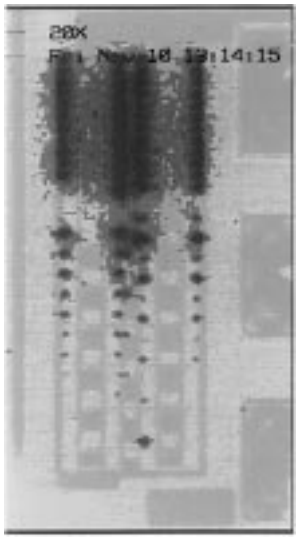

Fig. 6. Time-integrated commercial emission microscope image of switching induced light emission from a CMOS ring oscillator. This ring oscillator consists of 46 inverters and a NAND gate configured as an inverter, was built from 0.6 μm technology, and was biased at 5 V for the measurement. The emission is superimposed on an illuminated image of the circuit. Darker spots correspond to more intense hot carrier emission.

The image was obtained with an intensified charge-coupled device (CCD) camera on a commercial emission microscope and shows light emission from each of the 47 gates of the ring oscillator. The light emission appears in Fig. 6 as bands of dark spots and is superimposed on an image of the ring oscillator and its divider circuit. The divider circuit occupies the bottom two-thirds of the figure. The ring oscillator itself is completely obscured by the emission from the gates at the top of Fig. 6. Some emission spots also occur over gates in the divider circuit. If the dc input to the NAND gate is zero, the ring oscillator cannot operate, no electrical pulse circulates, and no light emission is observed from the ring oscillator or the divider circuit. For this image, we observe emission only from the nFET electrons because of their higher mobility, which produced hotter carriers than the pFETs. (In addition, for this particular circuit, part of the pFETs are buried under metal wiring, which is opaque to any hot carrier emission.) With a more sensitive light detector, emission was observed from the pFETs.

V. The Temporal Resolution of Weak Light Emission

The image in Fig. 6 was obtained by collecting the emission for several minutes with a CCD camera. The image shows that light was emitted but provides no information about the temporal characteristics of the light. Our models of light emission in CMOS circuits predict this light is emitted as short pulses. The pulses should only occur during switching of the gates of the ring oscillator circuit. The measured intensity of the emission in Fig. 6 means that each gate emits only a few detected photons every second or less than one photon per hundred thousand switching events. This emission rate is consistent with theory. In this section, a technique for measurement of the picosecond

time dependence of the intensity of such weak signals is described.

A. Single Photon Detectors

The most sensitive commercial detectors of light work on the principle of single photon counting [32]. The photomultiplier is such a detector. In a photomultiplier, a photon incident on a photocathode has a finite probability, the quantum efficiency, of emitting a photoelectron. The quantum efficiency depends on the wavelength of the light and the composition of the photocathode. The emitted photoelectron is then multiplied within the photomultiplier to create a pulse of about 10^6 electrons, with a duration of typically 1 ns. This amplified electron pulse can be detected and analyzed. Noise pulses are also generated in a photomultiplier. The thermal generation of electrons by a photocathode produces "dark" counts at rates of 10–1000 counts per second for a conventional 1-in-diameter photocathode cooled to $-25\,^{\circ}\mathrm{C}$, a standard operating temperature. Other sources of false counts include electron pulses generated by cosmic rays or by thermal generation of electrons within the multiplying section of the photomultiplier. These can be electronically distinguished from real photons and dark count by pulse height discrimination.

B. Time Correlated Photon Counting

The temporal properties of light detected by photon counting can be analyzed with picosecond accuracy using the technique of photon timing or time correlated photon counting (TCPC). TCPC has been described in many reviews [32]. It uses the fact that in a photon-counting photomultiplier, each photon-generated electron packet proceeds through the gain stages as a short nanosecond-length pulse. The time of arrival of a pulse in a given part of the multiplier is a fixed delay relative to when the photon arrived at the photocathode. This delay has a jitter of 50–100 ps in a well-designed photomultiplier. This determines the ultimate time resolution of TCPC. Therefore, measuring the time a pulse goes past a chosen point in the detector can be used to determine when the photon excited the photocathode.

Since typically 10^6 switching events are required to produce one detected photon from an nFET, the time dependence of the optical emission cannot be determined during one execution of a set of switching events by the chip under test. Multiple passes must be summed to recreate the time dependence of a single set of events. This recreated time dependence of the light from a single FET is called the "optical waveform" of the FET. Since far fewer than one photon is detected on average from each repetition of the instruction set, this optical waveform is not the actual intensity of emission versus time from a single pass, but rather measures the relative probability of detecting a photon at any given time within the pass. For each detected photon we determine the delay between the start of the electrical test pattern and the emission of the photon. An electrical trigger pulse synchronous with the start of each pass is used to initialize an electronic stopwatch. This start pulse can either be generated by the chip or by the tester driving the chip. If a photon is detected by the photomultiplier, the stopwatch is stopped. (If no photon is detected, the stopwatch is simply reset at the end of the set of instructions.) Typically, a time-to-amplitude converter followed by an analog-to-digital converter is used as the digital stopwatch for the time delay. This delay is the time from the start of the circuit to the emission of the photon, plus a constant offset fixed by the optical and electronic delays of the apparatus. The delay is passed to a computer, which stores it and updates a histogram of the number of detected photons for each time interval. As the histogram is built up, it ultimately (after 10^9 or 10^{10} passes) provides a good representation of the optical waveform. The signal-to-noise of the waveform improves as the number of passes is increased. For most cases when photon counting is used, the noise is due the combination of the dark count of the detector and the statistics for the detection of single photons. This technique does not "gate" or "strobe" the detector. Every photon that is emitted by the sample can be detected, except for a small "deadtime" correction, which will be discussed later.

Detectors consistent with TCPC include conventional single-channel photomultipliers, silicon avalanche photodiodes, and microchannel plate imaging photomultipliers. The properties of the last detector have been described in the context of time integrated imaging by Lampton and Carlson [33] and, in the context of TCPC, by McMullan *et al.* [34] and Charbonneau *et al.* [35]. All of the time-resolved hot emission results to be presented below were obtained using a microchannel plate imaging photomultiplier. The imaging of the chip on the photocathode of this detector allows the identification of individual devices and modules in space as well as time. Therefore, a single measurement of light emission from a working IC using a microchannel plate imaging photomultiplier provides temporal and spatial information about the behavior of many different devices. With such a parallel measurement of time-dependent optical emission from multiple devices, it is possible to make a detailed characterization of an entire circuit with a single measurement; hence the name "picosecond imaging circuit analysis,"or PICA, for the technique.

C. Imaging Detectors for PICA

A cross section of the detector used for PICA, a Mepsicron, is shown in Fig. 7 [33], [36]. This detector has been widely used in atomic and condensed matter physics and chemistry [36]. The light from the sample is imaged onto the photocathode at the top of the figure. The quantum efficiency of the photocathode is uniform over its area. Therefore, the time-integrated two-dimensional spatial dependence of the local density of photoelectrons emitted from the photocathode is the intensity of the optical image on the photocathode. An electric field is applied to the gap between the photocathode and the first microchannel plate. This accelerates the photoelectrons emitted from the photocathode into the first microchannel plate and prevents the electrons from drifting laterally in the gap. When an electron enters a channel of the microchannel plate, it is subjected to an accelerating voltage. Within the channel,

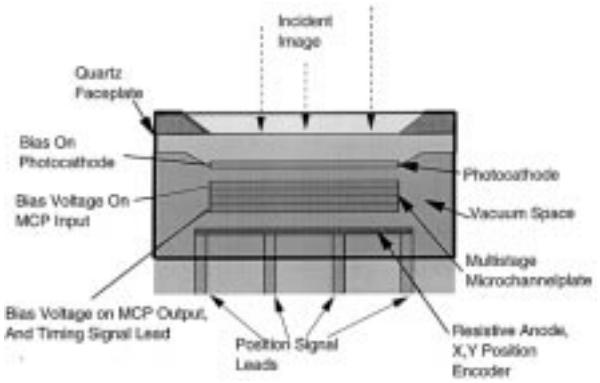

Fig. 7. Cross-sectional view of an imaging microchannel plate photomultiplier [36].

it undergoes multiple collisions with the walls, generating more free electrons, and ultimately producing a pulse of 10^5–10^6 electrons. These additional electrons come from the high voltage supply biasing the photomultiplier. The power supply provides a transient current pulse with the passage of each amplified electron pulse through the microchannel plate. This current pulse is used as the timing pulse for TCPC. While the electron pulse is within the microchannel plates, it is confined to a few neighboring channels so that when the pulse emerges from the bottom of the microchannel plate and strikes the resistive anode/encoder in Fig. 7, it is still spatially localized to the same x, y location as the photon that originally struck the photocathode.

To determine this x, y location, a special resistive anode is used, which captures the electrons coming from the microchannel plates. The electron packet spreads to the edges of the resistive anode, and the electrons are collected by charge sensitive amplifiers at the four corners. The location of where the packet was incident on the resistive anode can be calculated from the ratios of the charges collected at each amplifier [33].

The microchannel plate imaging photomultiplier therefore responds to each detected photon with three outputs [34]. One is due to the current pulse from the high-voltage power supply, which signals the passage of an electron pulse through the microchannel plates and provides temporal information with an instrumental response time of ∼90 ps, the full-width at half-maximum (FWHM). The other pair of outputs (x, y) are used to derive the spatial position of the photon. Typical spatial resolution at the face of the photocathode is about 60 μm with a 25-mm diameter photocathode. Because of the RC time constant of the resistive anode and charge amplifiers, the detector has a "dead" time of several microseconds between detected photons. The deadtime correction to the efficiency of the detection system is negligible for data rates below 10 KHz, which has always been the case in PICA up to now.

D. The PICA System

Fig. 8 shows a block diagram of a PICA system. The chip under test is at the lower left. It is observed by a collection lens which images the light emission onto the photocathode of the detector. The sample is excited by the circuit tester at the lower right, and either the sample or the tester generates a pulse at a fixed time in each electrical cycle of the chip. In the description of TCPC above, this trigger pulse was used to start the timer and the photon timing pulse was used to stop the timer. In actual practice, the roles of these pulses are interchanged because there are many more trigger pulses than photon timing pulses. Outputs from the four charge amplifiers at the anode corners go to a position analyzer, which generates voltage signals proportional to the x, y location of the detected photon on the photocathode. Digital signals representing the output of the time-to-amplitude converter and the x, y positions of the detected photon are stored in a three-parameter multichannel analyzer for subsequent display and analysis of optical waveforms and time-resolved images.

To demonstrate its capabilities, this PICA system was used to image a portion of the operating ring oscillator in Fig. 6. The time-integrated image of the light emission observed by the PICA system is similar to that shown in Fig. 6. If the data describing the time of arrival of the detected photons are presented by binning the photons detected by the Mepsicron into sequential 34-ps-wide time frames, a series of images are obtained, three of which are shown in Fig. 9. The data in Fig. 9 were measured for the ring oscillator biased at its design voltage of 3.5 V. In this image, a grayscale photograph of the circuit is used as a background for the emission, which appears as dark spots. Two strong spots are seen in the bottom row of Fig. 9(a), one in the bottom row and one in the top row of Fig. 9(b), and two in one of the center rows of Fig. 9(c). In Fig. 9(c), we also see one emission spot from a gate in the divider circuit. In Fig. 9, the divider is on the right side of the figure, in contrast to Fig. 6, where it was at the bottom. In Fig. 9, we see many of the gates of the ring oscillator in the left half of the figure which were covered by the time integrated light emission in Fig. 6. The hot carrier emission is detected by the Mepsicron; the background grayscale image was taken with a conventional camera. At any instant of time, within the approximately 100-ps temporal resolution of the PICA system, only one or two gates in the ring oscillator are emitting light. Because the gate-to-gate delays are ∼100 ps and the period of the ring oscillator is ∼10 ns, the measurement in Fig. 6 taken over several minutes sums over many individual switching events. These individual events are temporally resolved by the PICA system. The different spots in Fig. 9 due to the emission from the nFETs of the ring oscillator, which are separated by about 20 μm, can be easily resolved by the PICA system. This behavior is consistent with the known behavior of the ring oscillator, and the model of light emission by hot electrons generated by switching in the ring oscillator.

The spatial resolution of the PICA system depends on the spatial resolution of the detector and the optical system used to image the sample on the detector photocathode. The 60-μm spatial resolution of the Mepsicron, a 100X NA 0.85 commercial microscope objective, and the diffraction limit with 1 μm wavelength light, mean that FETs separated by about 0.75 μm can be spatially resolved. With the 25

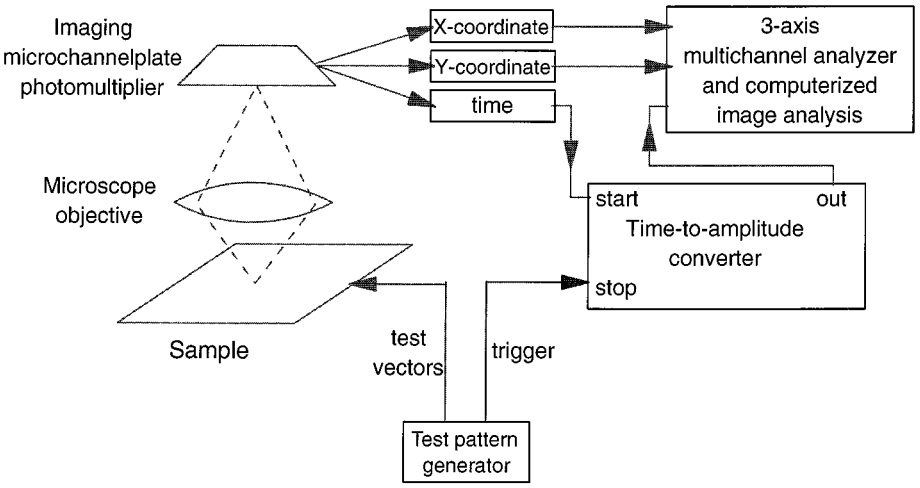

Fig. 8. Block diagram of a picosecond imaging circuit analysis system.

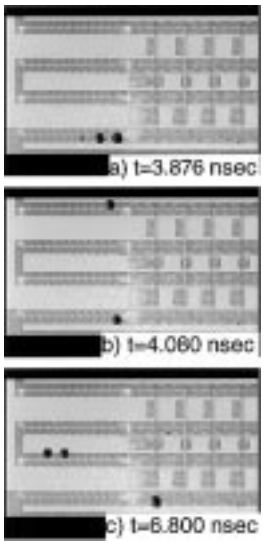

Fig. 9. Example of spatial and temporal response of an imaging microchannel plate photomultiplier using a time correlated photon counting system to look at the emission from a ring oscillator identical to the circuit used to produce Fig. 6. The pulse nature of the emission is clearly seen, as is the ability to spatially resolve light pulses from next-nearest-neighbor gates. The emission is superimposed on an image of the circuit, and appears as the dark spots.

mm detector size, a field of view of 0.25 mm is seen in the PICA image. If a lower magnification is used, a larger field of view can be obtained, at the sacrifice of spatial resolution. The temporal resolution of the PICA system for determining gate-to-gate delays is considerably better than the 90-ps FWHM instrumental resolution of the TCPC system. Gate-to-gate delays, which are determined by measurements of the time shift of the peaks of the emission pulses, can be performed with accuracies at least an order of magnitude better than the FWHM of the instrumental response function.

VI. Picosecond Imaging Circuit Analysis

The spatial and temporal resolutions of PICA allow the quantitative description of the switching activity in individual gates of a CMOS circuit. We demonstrate this in the following using the simple ring oscillator of Figs. 6 and 9, viewed from the front side. Examples of quantitative backside measurements on normally operating, flip-chip packaged microprocessors, including a state-of-the-art 600-MHz microprocessor, are then presented.

A. Front Side Characterization of Ring Oscillators with PICA

Fig. 9 showed the emission from the same ring oscillator as in Fig. 6, at three instants of time during one cycle of the ring oscillator. Summing over all the 34-ps time frames of the 10-ns period of the ring oscillator produces the 47 bright spots of Fig. 6. Curve A of Fig. 10 is the optical waveform from a single nFET in the center of one of the rows of Fig. 6. The optical waveform from each nFET of the ring oscillator is similar to curve A. Each waveform is a pulse train with a period of just under 10 ns, the electrical period of the ring oscillator. Each cycle includes a strong light pulse and a weak one. These pulses correspond to the $V_{\rm OUT} = V_{\rm DD}$ to zero and $V_{\rm OUT} = 0$ to $V_{\rm DD}$ transitions of the inverter, respectively. Two strong pulses from next-nearest-neighbor gates are shown in each frame of Fig. 9. In between each pair of strong pulses in Fig. 9 is an nFET emitting a weak pulse at about the same time. However, the false color levels chosen for Fig. 9 suppress the appearance of the weak pulse. During the period when curve A of Fig. 10 shows an inverter switching from $V_{\rm OUT} = V_{\rm DD}$ to zero (producing a strong pulse of light), the next gate, which generates curve B, switches from $V_{\rm OUT} = 0$ to $V_{\rm DD}$ (producing a weak pulse of light), and vice versa. The emission in curve B shows the same periodicity as curve A but is almost 180° out of phase. Curve C of Fig. 10 is the optical waveform from the next-nearest-neighbor inverter nFET. It is almost in phase with curve A but is delayed in time by about 190 ps. Because of the imaging nature of PICA, all of these optical waveforms were measured simultaneously. The next-nearest-neighbor light emission peaks all show gate-to-gate delays of about 190 ps except for those delays involving nFET pairs spanning adjacent rows of the ring oscillator. These delays are

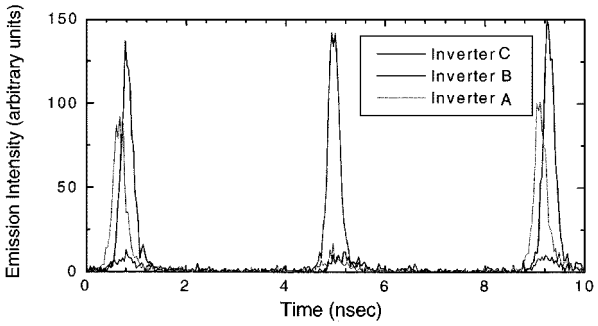

Fig. 10. Three optical waveforms of switching induced light emission from three neighboring inverters of the ring oscillator shown in Fig. 6, biased at its normal operating voltage of 3.5 V. The data was obtained using the system in Fig. 8.

longer, at about 225 ps. The sum of the gate-to-gate delays of all the inverters in the ring is the period of the oscillator.

The gate-to-gate delay in a ring oscillator is half of the value of the next nearest neighbor delay. The gate-to-gate delay for the ring oscillator imaged in Fig. 9 is about 95 ps for pairs of gates within a single row of the circuit. This is consistent with simulations of this circuit. The observation of longer delays associated with emissions from next nearest neighbor gates on different rows of the ring oscillator is due to the effects of RC loading on the speed of the inverters. The extra delay is due to the additional length of polysilicon lines connecting the inverters on different rows, which provides a larger load than the relatively short lines needed to connect inverters in the same row [37]. This additional delay has been confirmed by simulations of the circuit. The presence of alternating weak and strong emission pulses from each inverter nFET reflects the asymmetric nFET currents for the $V_{\mathrm{OUT}} = V_{\mathrm{DD}}$ to zero transition as compared to the opposite transition. The alternation of the emission intensities allows the unambiguous assignment of logic levels of gates before and after the switching event. PICA therefore provides a complete description of the operation of the entire ring oscillator at the gate level in a single acquisition.

B. Use of PICA for Backside Characterization

We have shown that PICA can measure the propagation of signals in a simple CMOS test circuit. In this section, we present results obtained using PICA on commercial, flip-chip packaged ICs to describe the time evolution of states in normally packaged, fully functional, parts. These measurements were all obtained from the backside of the chip.

Fig. 11 shows four PICA images obtained from an IBM Power3 microprocessor [38]. This microprocessor featured 0.25-μm channel length transistors, operated at 2.5 V, with an internal clock frequency of over 200 MHz. It was fabricated on a 270-mm^2 Si substrate, which was flip-chip mounted on a 1088-pin ceramic package. The sample was prepared by removing the cap of the package to expose the unpolished backside of the flip-chip IC. The mechanically rough backside of the die meant that the buried front side could not be imaged through backside. The backside was therefore thinned and polished to an optical finish. The solder

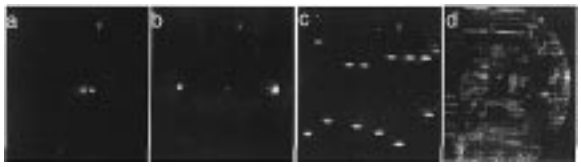

Fig. 11. Four time-resolved images of switching induced light emission from an IBM Power3 CMOS microprocessor obtained using a "macro" imager on a PICA system. Only the clock system of the chip is being operated during the measurement. Each frame corresponds to an interval of about 28.5 ps. Frame (b) is delayed by 425 ps with respect to Frame (a). Frame (c) is delayed by 540 ps with respect to Frame (b). Frame (d) was obtained 800 ps after Frame (c).

balls of the flip-chip package, and the epoxy potting the front side of the chip to the ceramic holder, provided sufficient mechanical stability for the chip to be thinned by grinding with diamond grits to 200 μm and made optically smooth by polishing. The thinning reduces the amount of emitted light that is absorbed in the die, while the polishing enables the imaging of the front side of the chip from the backside.

The thinned and polished part was placed in a socket for the ceramic package and activated using the normal I/Os of the chip. The imaging system for Fig. 11 used a macro lens, which allowed the PICA detector to observe in a single measurement an area including about 2/3 of the chip. The images in Fig. 11 [38] were obtained with a simple ac test pattern. The chip was excited by a 50-MHz clock signal, and appropriate dc input levels were applied to enable the doubling of the frequency of the external clock in the chips phase-locked loop (PLL). The main time-varying signal in the chip during PICA measurement was the 100-MHz internal clock.

The clock signal in this microprocessor is generated by a phase-locked loop. Because of the need for precise synchronization of the clock signals across chip, the output of the phase-locked loop is distributed to the chip in a multistep process. The PLL output drives a single centrally located clock buffer. Emission from this buffer during a 28.5-ps time interval is shown in Fig. 11(a). The PLL drives two repeater buffers, and switching in these buffers during a subsequent 28.5-ps time interval is shown in Fig. 11(b). These repeaters drive 16 sector buffers located throughout the chip. Emissions from 13 of these sector buffers at a later time are shown in Fig. 11(c). The remaining three are outside the figure's field of view. Finally, the sector buffers drive local clock regenerators. Switching activity in these circuits is shown in Fig. 11(d) at a still later time after the earlier stages of the clock tree have completed switching. Because of the use of a macro lens, which can view a large area of the chip, the spots of light in Fig. 11 include contributions from multiple devices. Nevertheless, the intensity of the light emission from each spot can be measured as a function of time and used to time the activity in the clock distribution system. The optical waveforms of the switching in the central clock of Fig. 11(a), two repeaters of Fig. 11(b), and a typical sector buffer in Fig. 11(c) are shown in Fig. 12 [38]. The delays associated with the propagation of the 100-MHz clock signal to the repeaters and the sector buffers can be seen in Fig. 12. Fig. 12 can be used to determine the accuracy of simulations

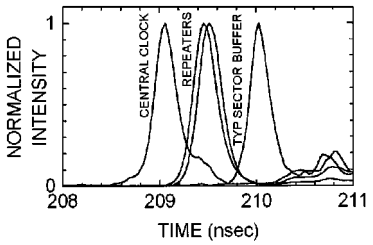

Fig. 12. PICA waveforms from the central clock buffer, two repeaters, and a typical sector buffer of the microprocessor imaged in Fig. 11 [38].

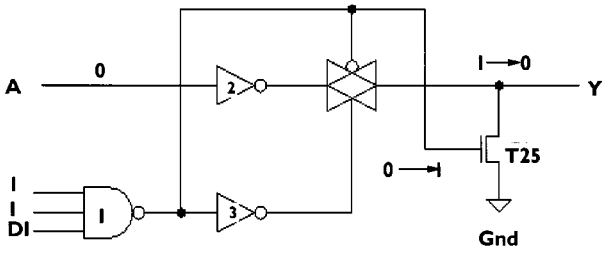

Fig. 13. Schematic diagram of an I/O circuit in a microprocessor suspected of causing timing failures on chip-to-chip paths [39], [51].

of the clock distribution system and to measure the skew in the clock distribution system across the chip.

We now discuss an example of how PICA can be used to identify failures in an IC. Fig. 13 [39], [51] is a schematic of an I/O circuit in an IBM S/390 G5 microprocessor. The microprocessor is a 600-MHz part based on a 0.25-μm process. Test versions of this chip showed timing failures on chip-to-chip paths. A common I/O circuit, shown in Fig. 13, was thought to be the problem, but normal I/O testing was unable to identify the exact cause of the defect. It could not determine if the failure was in T25, Gate 1, Gate 3, or one of the wires connecting these devices in Fig. 13. The failure was characterized electrically by a slow output at Y when D1 was switching from one to zero and A was fixed at zero. PICA measurements observed both properly functioning and defective I/Os. Fig. 14 shows the optical waveform obtained (a) from transistor T25 for a properly functioning I/O and (b) from this transistor for a faulty I/O. Comparison of Fig. 14(a) and (b), and our earlier discussions of PICA show that for the faulty I/O, T25 is conducting when it should be off since there should be just a short emission pulse during switching, as seen in the waveform for the good I/O. The optical waveforms for Gates 1 and 3 for good and bad I/Os resembled the waveform of the good T25. Fault simulations of the switching currents in this I/O showed that the observation of proper behavior by gates 1 and 3 for all I/Os and anomalous, slow switching by T25 for faulty I/Os was due to a highly resistive lead driving the gate of T25. Fig. 15 shows (a) the proposed schematic of the faulty I/O based on the PICA data and the simulations and (b) a scanning electron microscope (SEM) image of the physical, process related, defect in the lead. There was a physical void between the lead and the gate. The SEM was guided directly to the defect by the PICA data. The ability to correlate emission data with circuit timing information is a critical element that sets PICA apart from static-emission analysis [39], [51].

VII. Laser Voltage Probe Charge Sensing and Franz Keldysh Effects in Si Devices

The long-wavelength dielectric function or complex index of refraction of Si describe the velocity and amplitude of a laser beam in Si. The optical response depends on the band structure, temperature, voltage levels across the sample, concentrations of free carriers, etc. Free carriers contribute to the response through intraband, free-carrier-like transitions, and interband transitions between filled and empty states in different bands.

The intraband, free-carrier-like transitions are due to the motion of the charged carriers in the electric field of the light. The effect of free carriers introduced by doping on the optical response of Si was treated by Heinrich [7] and Koskowich and Soma [40]. Changes in the bias of a p-n junction or the base of a bipolar transistor change the local free-carrier concentration and produce small changes in the local index of refraction. The magnitude of the change of the index of refraction in a doped junction for doping levels near 10^{17} cm^{-3} can be between one part in 10 000 to 100 000 [40]. Since the depletion layer of the junction is generally a small fraction of the thickness of the sample, the actual measured change in the reflected and transmitted light is even smaller. Heinrich *et al.* [6], [7] showed that such small changes in the free-carrier concentration in the base of a bipolar transistor during switching could be detected in reflection with 1.3-μm light using a very precise, phase-sensitive optical detection technique. The electric-field-induced changes in the relative phase of the probe beam enabled him to derive the voltage being applied across the base. The wavelength of light used by Heinrich was below the bandgap of Si, producing little absorption, and did not perturb the test device. Heinrich showed that similar results could be obtained for the depletion region of a p-n junction.

The application of an electric field to Si also modifies the electronic states near the edges of the conduction and valence bands. These changes slightly shift the absorption edge [22]. This is the Franz Keldysh (FK) effect, and it depends on the strength of the electric field, and the wavelength of light. Koskowich and Soma [40] showed that when the probe beam energy is below the bandgap, the electric-field-induced free carrier and the FK contributions to the local index of refraction are small and comparable in magnitude. As demonstrated by Heinrich [7] for nonresonant excitation conditions, the optical detection of the effect of voltage changes on a p-n junction requires careful effort to attain adequate signal to noise.

The FK effect is strongly enhanced if the photon energy is resonant with the indirect bandgap of Si. At 23 °C, the electroabsorption from a p-n junction fabricated on lightly doped, 10^{14} cm^{-3} (50–100 Ω·cm) Si with a heavily doped p layer (for maximum local fields of about 10^4 V/cm), shows large peaks at energies near the band edge of Si including strong resonances at 1.05 eV and 1.17 eV [22], [41] and some

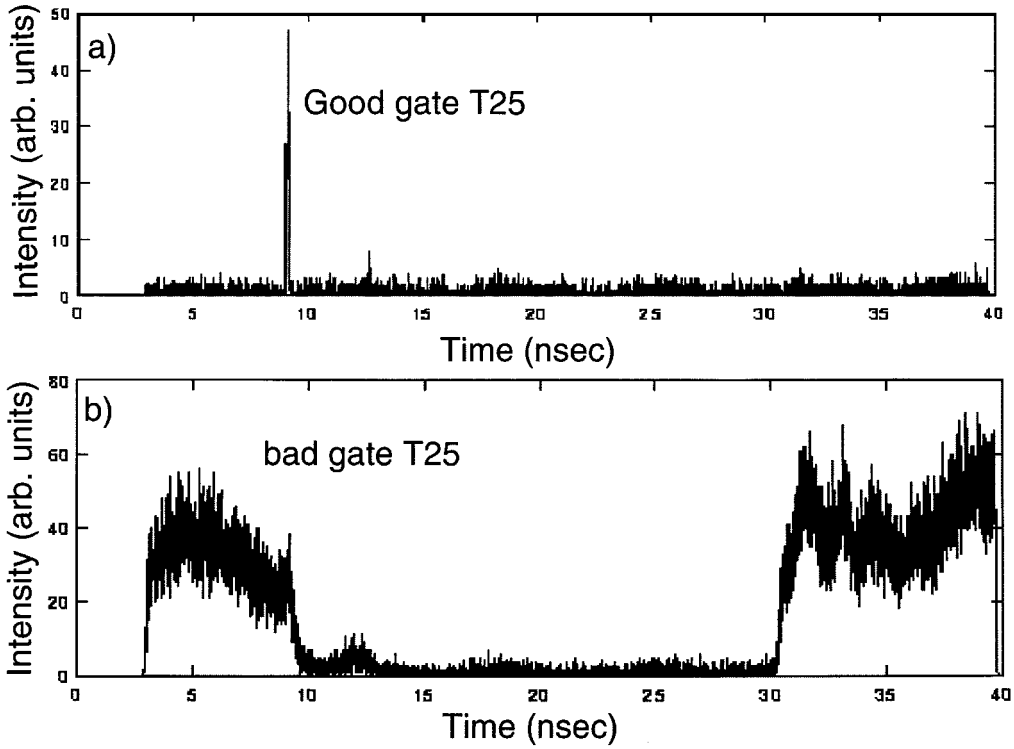

Fig. 14. PICA measurements on transistor T25 of Fig. 13 for both (a) good and (b) defective I/Os [39], [51].

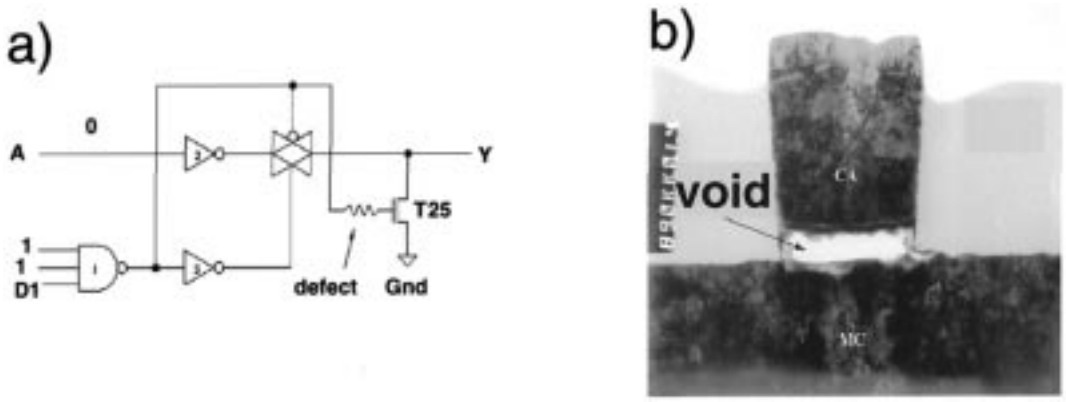

Fig. 15. (a) Schematic diagram of a faulty I/O based on Fig. 13, and PICA data, and (b) SEM image of the physical defect (a void) responsible for the failing behavior observed in electrical tests on this part [39], [51].

weaker lines. These lines reflect the emission and absorption of the various phonons required for different optical transitions by the indirect character of the energy gap of Si. The structures are about 30 meV wide.

As a result, electroreflectance measurements can be dominated by the FK effect if the wavelength of the probe is 1.06 μm (1.169 eV) and the sample is 23 °C. Experiments by Paniccia *et al.* [8] on biased Schottky barriers on heavily doped Si show that the magnitude of a transmitted beam can be modulated by 2×10^{-5} at this resonance. Changes of this magnitude can be measured using standard synchronous detection methods. Since the FK resonance is tied to the band edge of Si, it shifts with the band edge, which can move as the sample temperature changes. Frova *et al.* [41] showed that the maximum in the electroreflectance of a Si p-n junction at −181 °C occurs 1.21 eV, which is about 40 meV higher than at 23 °C. At −181 °C, the strength of the FK effect for 1.17-eV light (the 23 °C resonance energy) is an order of magnitude smaller than at 23 °C. Quantitative measurements of the electroabsorption at energies below 1 eV, or wavelengths longer than 1.23 μm, will require a phase-sensitive detection system, as found by Heinrich [7]. It should be noted that use of the resonant wavelengths for the FK effect is accompanied by photon absorption. This absorption raises the possibility of the optical injection of carriers into the junction by a measurement. These injected carriers can be a significant perturbation on the electrical performance of a small device and means that laser probing of devices at

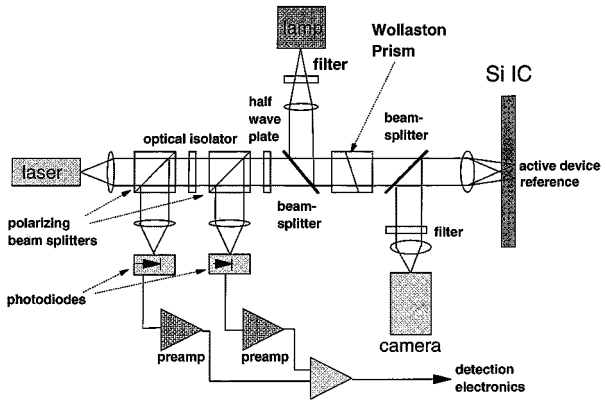

Fig. 16. Phase sensitive laser probe measurement system for the detection at a wavelength of 1.3 μm of electrical activity in a Si integrated circuit [7].

these wavelengths can be invasive if higher power levels are used.

The FETs of CMOS logic gates have reverse biased p-n junctions and large electric fields due to the diffusions defining the sources and drains. For laser probe measurements of voltage changes in these gates, the preferred probe point is the output node where the nFET and pFET are connected [8]. For a p-type substrate, the n-well pFET drain provides a reverse biased p-n junction when the gate output is at $V_{\rm dd}$, and an unbiased p-n junction when the output is at ground. The intensity and/or phase of a reflected beam generated by a probe coming through the substrate and reflecting from the contact to this drain will change with the logic state of the gate. Because a sub-1-μm wavelength laser beam can pass through several hundred micrometers of Si, the technique is suitable for use with a flip-chip mounted IC.

VIII. Laser Probes of Electrical Activity in Si Devices

A laser probe of a flip-chip mounted IC measures the light reflected from the IC because the far side of the sample where the transmitted beam would emerge is covered by opaque metal wiring layers and a grid of electrical contacts. A probe beam incident on the backside of an IC can undergo reflection at the air-to-substrate interface, the drain n-well diffusion, the n-well metal contact interface, and various dielectric-wiring interfaces. Gradations in the substrate doping can also produce reflections. Backside laser probes of electrical activity in silicon ICs will always find a strong reflected beam. The changes in the reflectivity induced by the time-varying electric fields at the sources and drains of the FETs will be much smaller.

Using subband gap light to minimize the generation of electron-hole pairs by the probe beam, Heinrich demonstrated that the two-beam phase-sensitive technique shown in Fig. 16 can detect the small changes introduced into a beam of light by voltages biasing a p-n junction. Heinrich did not use any resonant enhancements of the electroreflectance, so that the voltage-induced changes in amplitude were too small to detect practically. However, the field-induced changes in the index of refraction also produce changes in the transit time of the beam through the Si, which is measurable as a shift in the phase of the probe beam. In Heinrich's system, a 1.3-μm wavelength laser was used as the source. An optical isolator attenuates reflected beams so that they do not perturb the laser. The linearly polarized probe beam is split by a Wollaston prism into two orthogonally polarized, spatially displaced beams. The two optical beams, a probe and a reference, travel through neighboring regions of the device under test. A single objective is used to focus the probe on the active junction while the reference is focused on a region without an active device. The reflected light from the two beams are recollimated by the focusing objective and recombined as they pass back through the Wollaston prism. If the relative phase of the probe and reference is unchanged by the device, the reflected beam is linearly polarized. Any change in the relative phase of the reflected beams, even if there are negligible changes in their intensities will produce a partial circular polarization of the recombined reflected beam. The polarizing beam splitters and photodiodes are used to convert the change in polarization of the reflected beam into an electrical signal to determine the phase shift between the probe and reference beams. Heinrich showed that the system in Fig. 16 could detect voltage changes in p-n junctions of less than 0.1 V at 5 GHz [7]. The two-beam system provides a powerful method to normalize the contributions to the reflected probe beam from common inhomogeneities in both beams and isolate the effect on the probe beam of the applied field in the reverse biased p-n junction of the device under test.

The use of a two-beam approach increases the difficulty of use and limits the flexibility of the experimental system. We showed previously that the resonance FK effect is one to two orders of magnitude stronger than the electric-field-modulated free-carrier effect or the off-resonance effect. This increase in the amplitude of the modulation of the index of refraction means that the effect of applied fields on reverse biased junctions in IC can be derived from the measurement of the intensity of a single reflected beam. For the simple pulsed laser electroreflectance system shown in Fig. 17, Paniccia *et al.* [8] found that a detectable time-varying signal can be measured from the backside of a reverse biased p-n junction. This is a single-beam system, and the polarization components are used only to separate the incident and reflected beams of light outside the sample. The observation of detected signal levels at reasonable signal to noise depends on the resonant enhancement of the FK effect at the measurement wavelength of 1.064 μm. This system would be less sensitive if the laser wavelength was not well matched to the resonance. For the 1.064-μm laser, if the junction temperature was 150 °C higher or lower, the signal would be much smaller. Using the system in Fig. 17, it was shown that the amplitude of the reflected signal is linear with respect to the applied voltage. This is surprising since theory and previous experimental studies of the FK effect suggested that the magnitude of the effect depends nonlinearly on the applied bias voltage as V^x, where $x = 1.33$ from theory and between 1.4 and 1.9 from experiment [22]. In spite of this quantitative

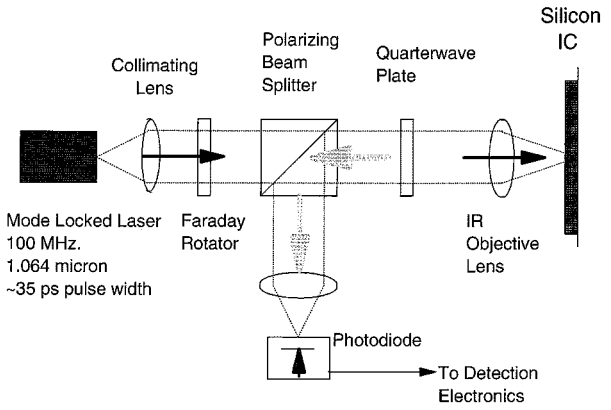

Fig. 17. A single beam, 1.064-μm laser voltage probe system for using the Franz Keldysh effect to measure electrical activity in a Si-integrated circuit [8].

disagreement, the measured reflectivity changes can clearly be used to measure electrical activity in an FET.

IX. Laser Voltage Probes for Si Integrated Circuits

In the previous section, it was shown that a simple laser probe system can measure changes in the voltage across depletion regions of ICs from the wafer backside if the laser wavelength is resonant with the silicon bandgap. The signal levels, and the picosecond switching times characteristic of current ICs, prevent the measurement of voltage levels in working operating circuits by simply monitoring the time-varying intensity of the reflected beam of a continuous 1.064-μm laser. These conditions require the use of synchronized sampling methods with a picosecond pulsed laser, integrated over many cycles of the operation of the test device. It is not possible to increase the intensity of the laser probe to arbitrarily high levels, increasing the signal linearly, since the 1.064-μm light is absorbed in the sample, and the carriers generated by the absorption can modify the circuit operation. The constraint of low power levels for the probe beam means that adequate signal-to-noise ratios must be obtained through averaging of multiple sampling measurements.

A mode-locked laser generating short light pulses is used as a source for a laser voltage probe (LVP) system because of its temporally narrow pulses and small jitter. It provides the basis for stroboscopic measurements since data are obtained only when a light pulse is probing the sample. The bandwidth of the technique is related to the temporal width of the laser pulse and its jitter. If the laser generates a train of 35-ps-wide pulses with a jitter of 10 ps, a measurement bandwidth of 12 GHz is possible [8]. The time dependence of the waveform being measured is obtained by shifting the relative delay of the sampling pulses with respect to the electrical stimulation of the chip. The system in Fig. 17 uses a 1.064-μm output mode-locked YAG laser. The pulses are 35 ps wide with a repetition rate of 100 MHz. If the IC being tested operates at 100 MHz, shifting the time of arrival of the laser pulses on a particular p-n junction over 10 ns would provide a complete stroboscopic reconstruction of the voltage waveform.

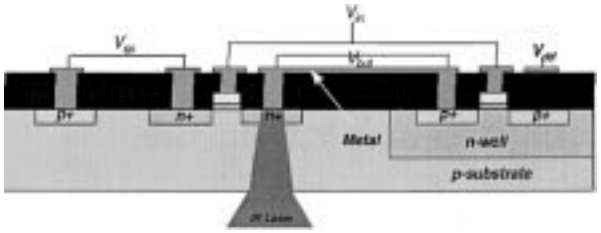

Fig. 18. Schematic representation of the geometry of the interaction of the probe beam in a laser probe system with a node in a CMOS gate [42].

If each sampling window was 50 ps wide, the full 10-ns waveform could be captured in 200 channels. Because of the low signal levels, many repetitions of the electrical waveform are required to reconstruct the waveform with good signal-to-noise. This system is assembled from commercial parts but can only be used to obtain electrical waveforms from chips that accept the mode-locked laser as their clock. The actual implementation of such a stroboscopic system for the measurement of state-of-the-art ICs, especially microprocessors, is complicated by the limited range of operating frequencies of the chips and the limited tunability of the repetition rate of mode-locked lasers. A practical LVP system must deal with two separate clock systems: one derived from the mode-locked laser and one from the tester operating the chip. The separate clocks must be synchronized so that the timing of the laser pulses is always in phase with the electrical waveform of the chip. This has been achieved by Winer and Paniccia [8], who phase locked a subharmonic of the output of the mode-locked laser to the clock of the tester. This is an efficient solution if the frequencies of the laser and the tester clock are very close or simple harmonics of each other. It can be inefficient if the tester and mode-locked laser frequencies have no simple common denominator. Although free-running mode-locked lasers today are capable of subpicosecond pulses, the phase locking of the laser to the tester clock for LVP results in significantly longer laser pulse widths, typically 35–40 ps. The probing laser pulse is then focused on the drain diffusion, as shown in Fig. 18 [42], and the intensity of the reflected beam measured. Using diffraction-limited optics, beam sizes of 0.75 μm are obtainable.

X. Laser Voltage Probe Measurements of Circuits

The application of an LVP system to the CMOS input buffer shown in Fig. 19 has been reported [42]. This image was obtained from the backside of the device substrate by a laser scanning microscope using a 100X microscope objective designed for backside studies. The Si substrate was thinned and polished to an optical finish. The dark lines are the gate diffusions. The larger structure on the left is the PMOS transistor, while the smaller structure on the right is the NMOS transistor. The gates were fabricated using a 0.35-μm technology. Fig. 20 shows four different LVP waveforms, each obtained over a few minutes using the optics of the confocal microscope. The complementary character of the voltages on the n- and pFETs, and the ability of the system to temporally resolve waveforms at

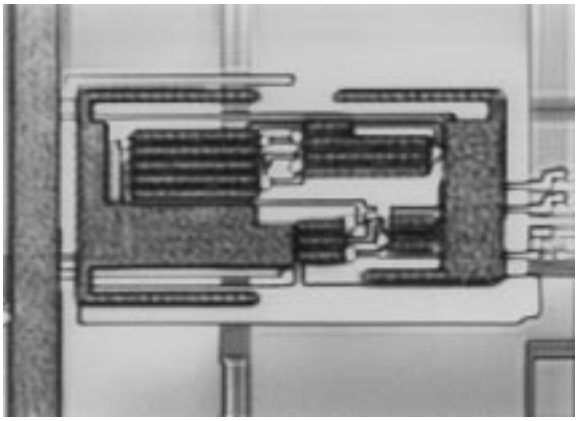

Fig. 19. Laser scanning microscope image of a 0.35-μm technology CMOS gate used to test a laser voltage probe system [42].

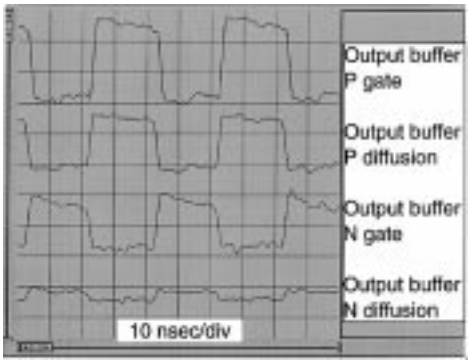

Fig. 20. Laser voltage probe waveforms obtained from the gate in Fig. 19 [42] The vertical axis represents changes in the laser reflectivity and, indirectly, the voltage.

the subnanosecond time scale from both n- and pFETS, are clearly shown.

XI. Summary and Conclusion

There is an urgent need for new laboratory methods to measure the timing of switching events in fully functional CMOS ICs from the backside of the chip. This need arises from the pressure in today's marketplace to rapidly produce competitive parts which optimize the use of both aggressive designs and process technologies. For example, the increasing importance of interconnects in limiting chip speeds and the uncertainties in existing synthesis tools for interconnect analysis, which "increase time to market, compromise performance, and boost cost penalties," [43] mean that the critical optimization of performance in high-speed chips will require physical measurements of the type discussed here. We have described two different solutions to this problem. Both techniques are completely compatible with modern wiring and packaging practices and can be used on flip-chip packaged circuits.

PICA can spatially resolve individual FETs in an IC, measure gate-to-gate delays with an accuracy of better than 10 ps, and do so for many devices in a single acquisition. Although the switching-induced hot carrier emission is very weak, the high speeds of modern ICs, and the sensitivity of commercially available detectors, allow useful measurements to be performed in reasonable periods of time. PICAs success also reflects our firm understanding of the physics of carriers in submicrometer FETs and recent achievements in developing optical techniques to detect and temporally resolve the weak optical signals found in laser fluorescence, Raman scattering, atomic trapping, and observational astronomy.

The principle weakness of PICA currently is the inefficiency of existing detectors, which means acquisition times of hours are required for backside measurements with test patterns that are more than a microsecond in length. Current detectors employ photocathodes, which are optimized for the visible, with weak response in the near infrared. These are not optimized for backside measurements of Si IC activity. One to two orders of magnitude improvements in performance will be obtained with the use of newer, infrared sensitive photocathodes [44].

At first blush, the 90–100 ps FWHM of the instrumental response of photomultiplier-based TCPC systems and the 0.7-μm spatial resolution limit for imaging by conventional optics appear to be significant challenges for applying PICA to deep submicrometer CMOS technologies. However, these limits apply to the ability to resolve temporal pairs that occur in the same location or spatial pairs that occur at the same time. Usually, there is sufficient time separation between emission pulses from the switching of nearby FETs that the emission pulses can be separated by the time signatures. Then, the emission pulses are not overlapping in space and time so that there is no interference between the pulses. Their spatial separation can then be determined by the centroids of the emission profiles, which can be measured with accuracy greater than the diffraction limit. Similarly, FETs that switch within 100 ps of each other will often be spatially separated by more than 0.7 μm, allowing them to be distinguished so that their relative times can also be determined from just the centroids of the optical waveforms.

PICA has been used to measure the electrical behavior of chips that are being fabricated today [38], [39], [51]. PICA waveforms have already been obtained on subquarter micrometer CMOS technologies operating at 1.5 V and lower [45]. In the future, devices will decrease in size and supply voltages will be smaller. Will hot electron emission be strong enough in future chips for PICA to be practical? The evolution of IC technology has been governed by scaling rules, which either keep the electric field distributions constant in devices or allow the field to increase as device sizes decrease [30], suggesting that high field effects will continue to be important and hot carrier emission will be detectable. In addition, recent Monte Carlo simulations of ultrasmall devices suggest that density fluctuations, which can create hot carriers, become stronger as devices shrink [46]. Both the scaling rules and the fluctuations will provide sufficient hot carriers to maintain the usefulness of PICA for future ICs.

LVP systems have measured single waveforms from signal nodes of ICs in 5 or 10 min. As a single point probe, the LVP technique is well suited to existing failure analysis methodologies. While LVP data can be obtained in

a noninvasive manner by using probe wavelengths below the absorption edge of silicon, this comes at the cost of increased experimental complexity and/or greater integration times. As a single-point probe technique, LVP sacrifices the advantage that other optical methods gain when they make use of the parallel processing provided by imaging. LVP probing appears to be vulnerable to the decreasing size of devices and structures in CMOS circuits. LVP requires that the probe laser spot be focused onto individual diffusions, and the size of these structures will soon be smaller than the diffraction limit in air. This will require the use of sophisticated advanced optical techniques such as solid immersion lenses [21]. Decreases in the sizes of devices and device structures will decrease LVP signals through the decreasing depths of diffusions in future CMOS ICs. Since the diffusions are capped by metallic-silicide layers, as the distance between the metal contact and the depletion layer decreases, the optical fields in the depletion layer become screened by the proximity of the metal and decrease the magnitude of the electric-field-induced changes in the reflectance and the LVP signals. The sensitivity of LVP will be improved if advances in laser technology produce mode-locked lasers capable of operating over broader repetition rates than currently available.

Both PICA and LVP are able to meet current needs and have the possibility of improvements to meet future needs. In our introduction, we briefly discussed the subject of BIST and other software- and tester-based methodologies. These have the ability to localize and characterize circuit failures electrically. However, BIST, for example, requires special circuits that take up space on the chip, add complexity due to the self-test circuits themselves, can reduce chip performance, and provide no analog information about the devices tested. The ability to include test circuits and test points in a commercial circuit poses interesting questions regarding the tradeoff between built-in test circuits and test points on the one hand and external testing techniques like PICA or LVP on the other. Built-in test circuits can provide a means of reducing the cycle time for test vectors, which will improve the efficiency of both PICA and LVP. Custom test points in conjunction with built-in test circuits can provide a means of efficiently extracting test information from a chip through either PICA or LVP, thus circumventing the bottleneck associated with the low bandwidths of the I/Os on modern chips. Failure analysis and debugging of future chip designs are likely to require optimal use of both electrical test techniques and external measurement techniques like LVP and PICA. In particular, applications of PICA to commercial chips have relied on electrical means to identify the existence of failures, software- and tester-based diagnostics to localize the fault to regions of the chip containing several thousand gates, and then PICA to identify the precise location and character of the fault [39], [51].

In this paper, we have concentrated on the development of optical tools for the study of switching in high-speed digital, CMOS ICs. We note that LVP has been used to obtain waveforms in bipolar transistors [7], and that hot electron effects are also present in bipolar [47] and BiCMOS transistors [48]. This suggests that both LVP and PICA can be applied to mixed-signal IC technologies, although the requirements for high-precision voltage measurements in the analog parts of mixed signal-chips pose difficult calibration problems for both LVP and PICA.

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James C. Tsang (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, in 1973.

He is a Research Staff Member at the Physical Sciences Department, IBM Thomas J. Watson Research Center, Yorktown Heights, NY. He has written more than 135 papers and holds several patents. His research has involved the optical properties of solids, including Raman scattering, and time-resolved studies of materials and devices.

Dr. Tsang is a Fellow of the American Physical Society and a Fellow of the American Association for the Advancement of Science. In 1993–1994, he was an AAAS-Alfred P. Sloan Foundation Executive Branch Science and Engineering Fellow at the White House Office of Science and Technology Policy. He has received three IBM Outstanding Achievement awards.

Jeffrey Alan Kash (Senior Member, IEEE) received the Ph.D. degree in physics from the University of California, Berkeley, in 1981.

He is a Research Staff Member at the Physical Sciences Department, IBM Thomas J. Watson Research Center, Yorktown Heights, NY. His primary areas of research have been ultrafast optical processes and hot electrons in semiconductors, with a recent emphasis on optical emission from silicon devices. He holds nine patents and has authored more than 90 publications.

Dr. Kash is a Fellow of the American Physical Society. He has received several Outstanding Innovation Awards from IBM.

David P. Vallett (Member, IEEE) received the B.S. degree in electrical engineering from the State University of New York, Buffalo, in 1982.

Since 1982, he has been with the IBM Microelectronics Division, Essex Junction, VT. He has worked in CMOS characterization and failure analysis in both engineering and management capacities, and is currently an Advisory Engineer in the Analytical Services Laboratory responsible for strategic development. He has authored several conference papers and journal articles, and has coauthored a book on microelectronics failure analysis and holds three U.S. patents in the field.

Mr. Vallett is a member of the Tau Beta Pi National Engineering Honor Society, the Electronic Device Failure Analysis Society, and is past chair of the SEMATECH Product Analysis Forum. He has received three best paper awards and an outstanding technical achievement award.