University of California, Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EE240B Spring 2018
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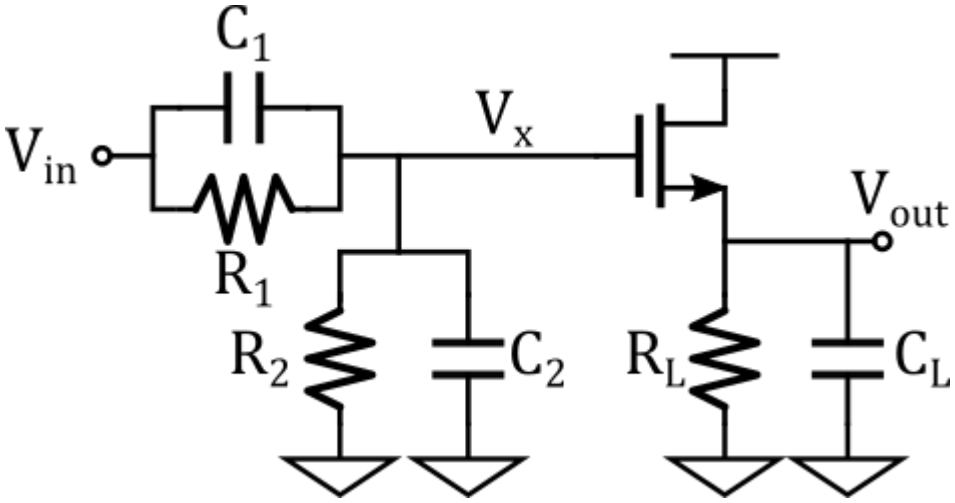
HW1
Due: Thursday, February 1 at 5pm PST

This is an individual assignment. Make sure that you explain all of your answers.
For these problems you may ignore body effect unless specifically told otherwise.

1. Transfer Function Analysis

Consider the following circuit:



a) Compute the s-domain transfer function and input impedance of this network as a function of R_1, R_2, C_1, C_2, R_L, C_L, g_m, and r_o. Consider only the capacitances shown.
b) Let $R_1 = R_2 = 5$ kΩ, $C_1 = 90$ fF, $C_2 = 10$ fF, $R_L = 400$ Ω, $C_L = 50$ fF, $g_m = 10$ mS, and $r_o = 2$ kΩ. Draw the bode plot of the transfer function and the input impedance. What is the mid-band gain (gain at intermediate frequencies)?
c) Using the values in part b, suppose now you want to halve the zero frequency without changing the mid-band gain and minimize pole frequency movement (a common scenario in high-speed link design). If you can only change one component value, which one will it be and what will be its new value? What is the new DC gain?

2. *Device Characterization*

In this problem, you will learn how to simulate and measure various properties of a transistor using Virtuoso ADEXL, which has very good parametric sweep support. ADEXL_tutorial.pdf contains instructions on how to setup and simulate the testbench using ADEXL for part a, with an optional (but highly recommended) section on how to automate the characterization process in Python using Berkeley Analog Generator (BAG).

Repeat parts a through c for transistors nmos4_lvt and pmos4_lvt in the BAG_prim library, with channel lengths of 45 nm, 90nm, and 180nm. For all parts, use $w = 0.5$ µm and $nf = 20$, which corresponds to a total width of 10 µm.

a) Run a DC simulation and measure the transistor bias current $I_{bias} = |I_{DS}|$. Tie the source and body of the transistor to ground (0V), and sweep $|V_{GS}|$ from 0.3 V to 1.2 V in steps of 50 mV, $|V_{DS}|$ from 0V to 1.2V in steps of 100 mV (Note that this means the gate and drain voltages of the PMOS will be negative). Generate 3D plots of the bias current for each transistor.

b) Using the data in part a, generate 3D plots of $g_m = \partial I_{DS}/\partial V_{GS}$, $g_{ds} = \partial I_{DS}/\partial V_{DS}$, and $V^* = 2I_{bias}/g_m$. If $V_{GS} = V_{DS}$, what value of V_{GS} will give you $V^* = 200$ mV?

   Note: to minimize numerical error, instead of using finite difference to approximate the derivatives, find derivatives of the 2-D spline interpolation of the bias current, using either Scipy or Matlab. For Scipy, the RectBivariateSpline class's __call__() method can compute derivatives for you.

c) Create a separate AC testbench (this is necessary for BAG to work) that measures the small signal current gain I_{ds}/I_g from 100 MHz to 1 THz with logarithmic sweep and 10 points/decade, with the same V_{GS} and V_{DS} sweeps as part a (with $V_{BS} = 0$ V). Generate 3D plots of the transit frequency f_T, which is the frequency at which the small signal current gain has magnitude 1. If $V_{GS} = V_{DS}$, what value of V_{GS} will maximize the product $g_m/I_D \cdot f_T$? What value of V^* does this corresponds to?

   Note: this will be a triple-parametric sweep, so expect this to take a while.

d) Setup an AC testbench for a common-source amplifier using the transistor nmos4_lvt with channel length 45 nm and an ideal current source load, with $V_{BS} = 0$ V, $V_{GS} = V_{DS} = 0.6$ V, an AC voltage source at the gate and a drain capacitance load of 10 fF. Sweep nf from 1 to 100 (remember to increase bias current too) and plot the 3-dB bandwidth of the amplifier. From this plot, estimate (using e.g. a least squares fit) C_{db}/w, the parasitic drain capacitance per µm of the transistor. (Technically this measurement includes C_{gd}, but we'll ignore that for now).

e) Measure the drain current noise density of nmos4_lvt with channel length 45nm, $V_{BS} = 0$ V, $V_{GS} = V_{DS} = 0.6$ V, and sweep the frequency from 1 MHz to 100 GHz. See noise_tutorial.pdf for instructions on how to setup the noise simulation. Find the total integrated current noise and the effective noise γ factor.

3. Amplifier Design Methodology

In this problem you will be developing a methodology to design resistively loaded common source amplifiers. The amplifiers you are designing will have the following (known) specifications, and you should use the data generated in problem 2 along with the specific values we provide below to execute your methodology on a representative design.

- Use nmos4_lvt with finger width of 0.5 µm.
    - Note that you are free to choose the channel length of your device, and you may want to run additional simulations to augment the data from problem 2. If you are unsure about how to choose the channel length, you can start by assuming 45nm, but you should then explain what limitations this will imply about the designs that your methodology can successfully realize.
- $V_{DD} = 1.2$ V.
- The amplifier will be driving some known capacitive load C_L. For the representative design, use $C_L = 50$ fF.
- The amplifier should have some minimum DC gain A_v and 3-dB bandwidth ω_{3dB}. For the representative design, $A_v > 2$, and $\omega_{3dB} > 2\pi \cdot 4$ GHz.
- You are free to choose the nominal input and output voltage levels (i.e., the "DC" bias at the input of the amplifier is up to you to choose), as long as it's between 0 and V_{DD}.
- Minimize power.

An ideal submission for this problem would be a script (in e.g. Python of Matlab) that performs the computations need to design the amplifier. For the representative design, you should print out all of the relevant sizing results (e.g., total transistor width, transistor length, load resistor value, DC input/output voltages/currents, etc.), and you should compute the error between the specified performance (i.e., A_v, ω_{3dB}, and bias current) and a simulation of the design.

For best practice, your design script should defines a top level function **`design_cs_amp()`**, with the following arguments:

- `data_dir`: the directory name containing characterization data files for each channel length.
- `vdd`: the supply voltage.
- `cload`: the load capacitance.
- `gain_min`: the minimum DC gain specification, in V/V.
- `bw_min`: the minimum 3-db bandwidth specification, in Hz.