University of California, Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EE240B Spring 2018
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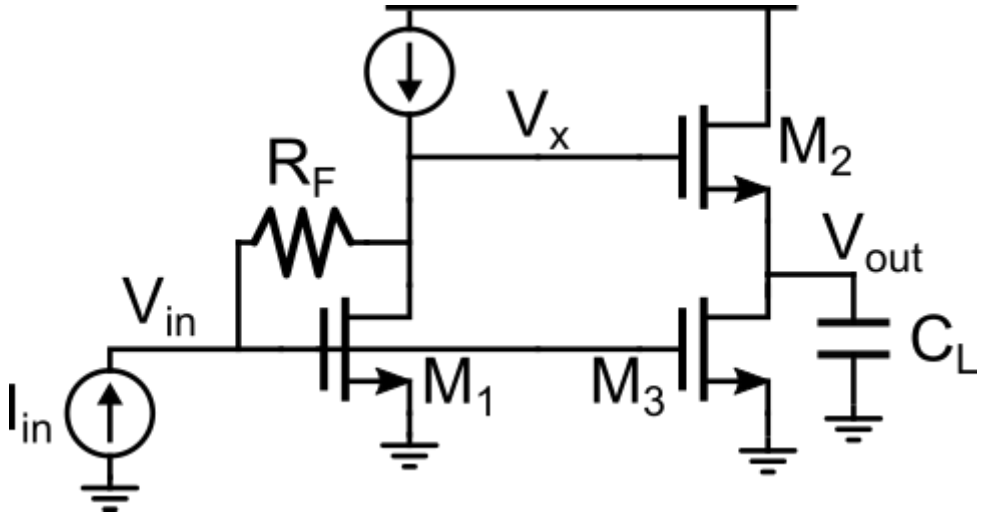
HW2
Due: Thursday, February 15 at 5pm PST

This is an individual assignment. Make sure that you explain all of your answers.
For these problems you may ignore body effect unless specifically told otherwise.

1. TIA Noise analysis

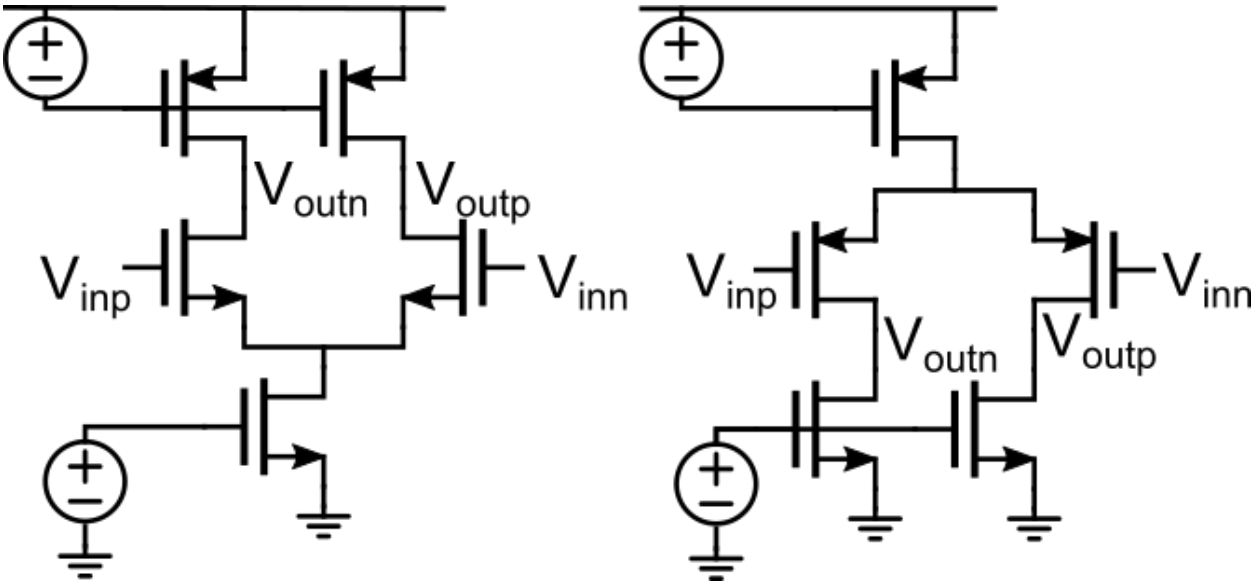
Consider the following circuit. Ignore all capacitors not explicitly drawn, and assume that all transistors have infinite r_o. Further, please assume that M1 and M3 have the same g_m (g_{m1}), but that M_2 has a different g_m (g_{m2}). (We will look at how to pick this g_{m2} relative to g_{m1} as a part of this problem.)



a) Compute v_{in}/i_{in} and v_x/i_{in}.
b) Compute v_{in}/i_{n1} and v_x/i_{n1}, where i_{n1} is the noise current of M1.
c) Find the transfer function v_{out}/i_{in} and the integrated output noise voltage variance due to i_{n1}.
d) Relative to g_{m1}, what value of g_{m2} minimizes the output voltage noise variance due to i_{n1}?
e) Now assume that the C_{gg}'s associated with M1 and M3 add some total capacitance C_{in} to the input node V_{in}. Using the same (relative) value of g_{m2} you found in part d), repeat parts b) and c). Why is the result so qualitatively different than the minimum noise variance you found in part d)?

2. *Noise-limited Design Methodology (Simple OTA)*

In this problem you will be developing a methodology to design a simple CMOS OTA based on either total integrated noise or output noise density constraints. Two example of such a simple OTA (one with PMOS input and one with NMOS input) are shown below. As this design has many degrees of freedom (just like in practical circuit), please feel free to include additional constraints/assumptions to make the design process easier (especially when you first start). However, you should clearly state these constraints/assumptions, and briefly explain under which conditions these constraints/assumptions may result in a sub-optimal design.



As a reminder, if you wish to get accurate matching between calculation and simulation, feel free to generate additional characterization tables for your design – e.g., characterizing the noise γ factor across various bias points.

As usual, the goal for your methodology should be to minimize the power dissipated by the circuit. The input specifications for your design methodology (generator) are listed below. Along with each specification, for those that are input parameters, we will provide in parentheses representative values that you should use for preliminary evaluations of your methodology.

- Use transistor finger widths of only 0.5µm. You are free to choose the channel length of your device. However, you must only use one channel length for all transistors.
- Supply voltage V_{DD}. (*Example value:* $V_{DD} = 1.2V$)
- You are free to choose your input common mode voltage, as long as it is between 0 and V_{DD}.
- Minimum load capacitance C_{load}. This represents the minimum capacitance at the output of your OTA; you may add extra load capacitance beyond this if you wish. (*Example value:* $C_{load} = 10fF$)

- Output common mode voltage V_{outcm}. Note that this common mode voltage specification is measured with zero differential input voltage and the input common mode at whatever value you have chosen. (*Example value:* $V_{outcm} = 600mV$)
- Minimum tail current source $V_{DS,min}$. Set the tail transistor's V^* to match that of the input transistors. (*Example value:* $V_{DS,min} = 200mV$)
- Input-referred maximum linear amplitude V_{imax}. You can either use this specification to directly set the V^* of the input devices (as discussed in lecture), or you can instead use an either large signal or small signal gain variation specification. (*Example value:* $V_{imax} = 150\ mV$)
- Minimum DC gain A_{min}. (*Example value:* $A_{min} = 8\ V/V$).
- The sinusoidal input signal amplitude V_{sig}. (*Example values:* $V_{sig} = 50\ mV$ *for integrated noise, and* $V_{sig} = 20\ mV$ *for noise density*)
- Minimum 3-dB bandwidth f_{3dB}. (*Example values:* f_{3db}*= 10GHz for integrated noise,* f_{3db} *= 2GHz for noise density*)
- Noise integration interval $[f_{start}, f_{stop}]$. (*Example values: for integrated noise, [1MHz, 100GHz]; for noise density, [1.4GHz, 1.6GHz]*)
  NOTE: for simulating total integrated noise, the exact integration interval often depends on the application. However, for most circuits, a general guideline is to set f_{start} to be 3 to 6 decades below the signal bandwidth, and set f_{stop} to 1 to 3 decades above the signal bandwidth.
- Minimum SNR SNR_{min}. (*Example value:* $SNR_{min} = 50dB$).

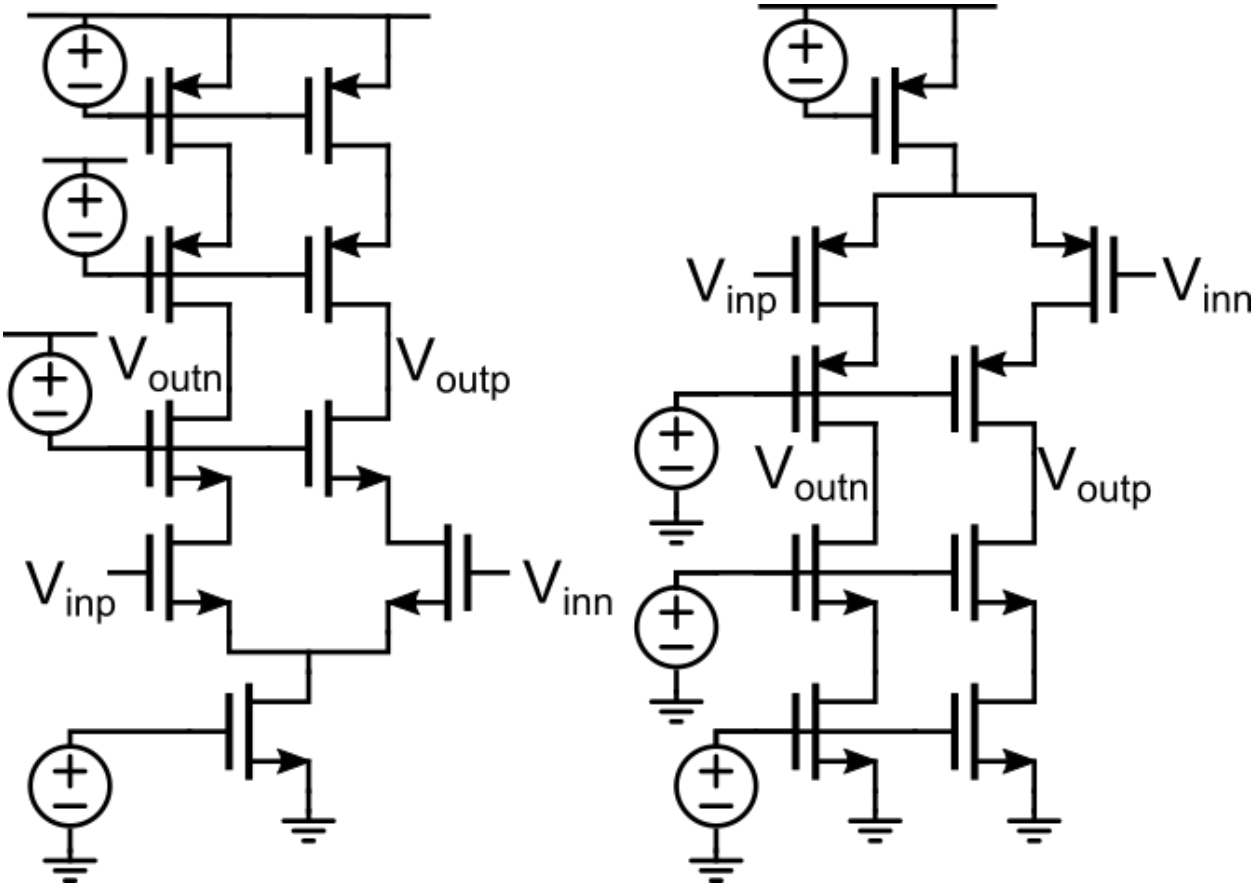
As usual, please submit a single script file that performs the computations need to design the amplifier. For the representative input values, you should print out all of the relevant sizing/biasing results, and you should compute the error between the specified performance and a simulation of the design.

NOTE: In this technology, if you use minimum channel length device, flicker-noise is very high, so your noise calculation for the total-integrated noise case may deviate significantly from simulation (up to 2X) if you do not take flicker noise in to account. If you didn't do anything special to account for flicker-noise, don't worry about it.

3. Noise-limited Design Methodology (Cascode)

In this problem we will develop a design methodology (much like we did in problem 2) for a telescopic cascoded differential OTA. Unlike problem 2 however, for the sake of simplicity, this time we will develop a methodology only for the noise density-limited case. As shown in the example schematic below, you are free to use ideal voltage sources for the cascode gate biases, and you are free to set the values of those voltage sources (as long as they are between 0 and V_{DD}). To simplify your methodology (and for layout-related reasons that we will discuss later in

class), your cascode transistors must use finger widths of 0.5µm (just like all of the other transistors), but the total width of the cascode devices must be between 1-4X the total width of the transistor that it is stacked on top of (e.g., for an NMOS input OTA, the NMOS cascode devices must have 1-4X the total width of the NMOS input devices). The input specifications (parameters) for this design should be identical to problem 2, but you should use the following example values to evaluate your methodology:



- C_{load} = 10fF.
- V_{outcm} 600mV.
- $V_{DST,min}$ = 150mV.
- V_{imax} = 150 mV.
- A_{min} = 30 V/V
- SNR_{min} 50 dB.
- V_{sig} = 10 mV
- f_{3db} = 500 MHz
- $[f_{start}, f_{stop}]$ = [100MHz, 200MHz]