University of California, Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EE240B Spring 2018
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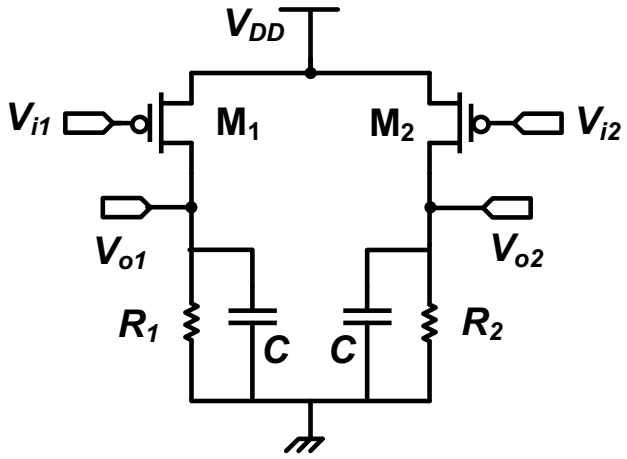
HW3
Due: Thursday, March 1st at 5pm PST

This is an individual assignment. Make sure that you explain all of your answers.
For these problems you may ignore body effect unless specifically told otherwise.

1. Pole-Zero Doublets

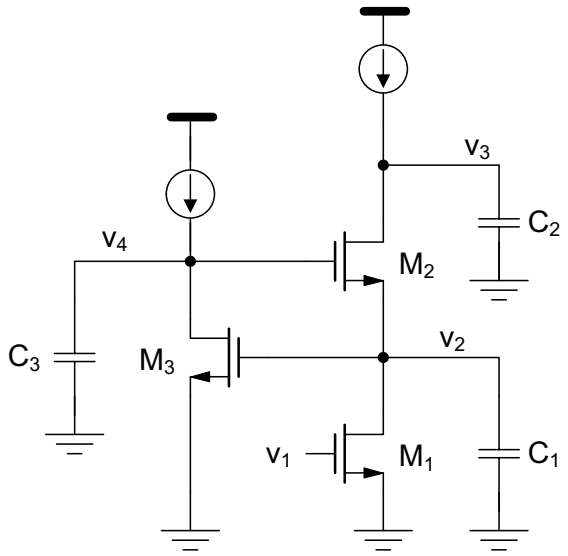
In this problem we will be looking at the behavior of the pseudo-differential amplifier shown below to gain some intuition into the origin and response of pole-zero doublets. You can assume that M_1 and M_2 form a differential pair (i.e. their small signal model parameters are identical) with infinite r_o. Moreover, you can assume that R_1 is larger than R_2, and that all capacitors are negligible with the exception of the ones explicitly draw in the diagram.



a) Derive an expression for the transfer functions $H_{11}(s) = V_{o1}(s)/V_{i1}(s)$ and $H_{22}(s) = V_{o2}(s)/V_{i2}(s)$ in terms of R_1, R_2, C, and the transistors' g_m.
b) Sketch the magnitudes of H_{11} and H_{22} versus frequency on the same plot.
c) Now derive and sketch the time-domain voltage response of V_{o1} to a voltage step on V_{i1}. Similarly, derive and sketch the time-domain voltage response of V_{o2} to a voltage step on V_{i2}.
d) Using the results from part a) and part b), sketch the magnitude of the transfer function for differential gain $H(s) = (V_{o2} - V_{o1})/(V_{i1} - V_{i2})$.
e) Now sketch the time-domain voltage response of the differential output $V_{o2} - V_{o1}$ to a differential voltage step $V_{i1} - V_{i2}$. While you can certainly derive this response using inverse Laplace transforms and partial fractions, you may find it significantly easier to use your answers from previous sections instead.

2. *Gain Boosted Cascode*

This problem will focus on the gain-boosted cascode amplifier shown below. To simplify the analysis, you can ignore the r_o of the transistors and all of the capacitors except for those explicitly drawn in the diagram.



a) What is the frequency response $H(s) = v_3(s)/v_1(s)$ of this amplifier? Approximately what is the unity gain frequency of the amplifier?

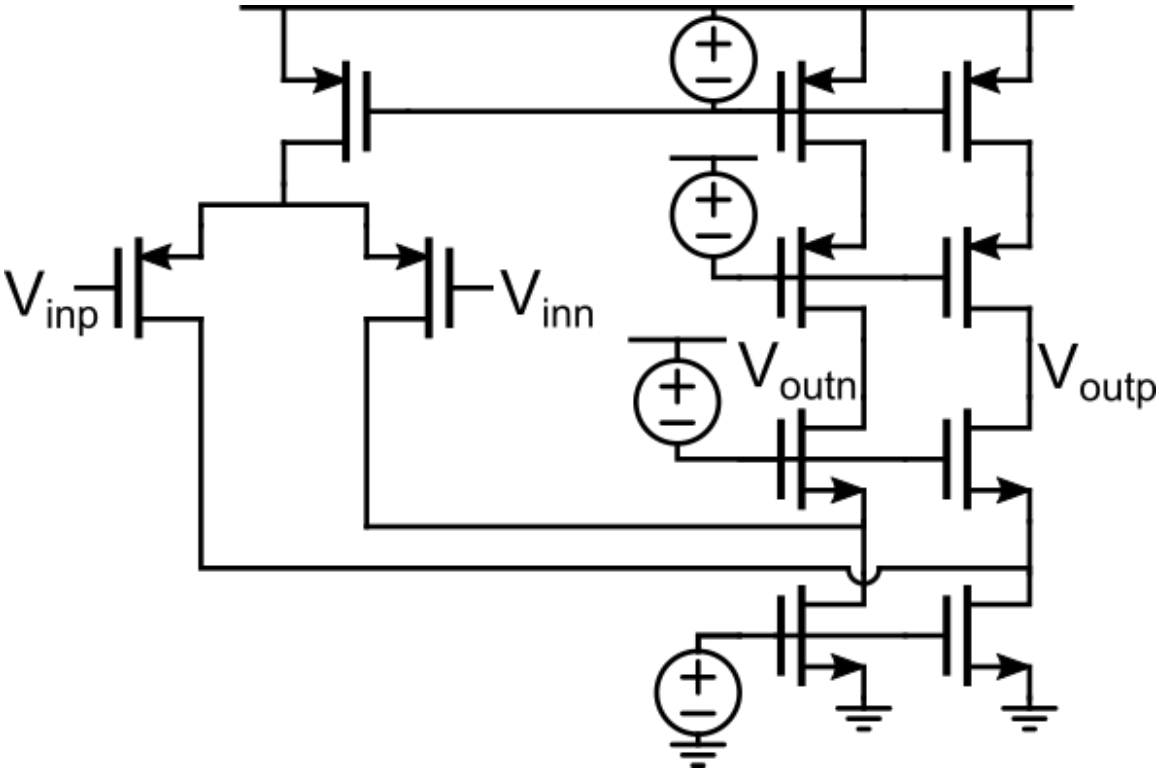
b) Approximately what conditions are required to guarantee that the gain boosting feedback loop maintains at least 45º of phase margin? You should provide your answer in terms of g_{m1}, g_{m2}, g_{m3}, C_1, C_2, and C_3. What conditions would we obtain if at least 60º of phase margin are required instead?

c) Assuming this amplifier is used in unity gain feedback, what conditions are required to guarantee that the gain boosting feedback loop does not introduce any significant pole-zero doublets that might limit the settling response?

d) Assume now that C_1=50 fF, C_3=40 fF, C_2=1.0 pF, $V_{m1}^* = 200$ mV, and $V_{m2}^* = 150$ mV. In order to achieve at least 60º phase margin and the criteria from part c), what are the minimum and maximum g_{m3}/g_{m1}?

3. Folded-cascode OTA design methodology

In this problem, you will be developing a design methodology for a folded-cascode OTA (shown in the schematic below) given a settling time constraint. Feel free to include additional constraints/assumptions to make the design process easier (especially when you first start). However, you should clearly state these constraints/assumptions, and briefly explain under which conditions these constraints/assumptions may result in a sub-optimal design.



The goal for your methodology should be to minimize the power dissipated by the circuit. The input specifications for your design methodology (generator) are listed below. Along with each specification, for those that are input parameters, we will provide in parentheses representative values that you should use for preliminary evaluations of your methodology.

- Use transistor finger widths of only 0.5µm. You are free to choose the channel length of your device.
- All matched transistors must have the same V^*, channel length, and threshold flavor.
- The OTA must be unity-gain feedback stable. You may add additional load capacitance if you need to stabilize the amplifier.
- Supply voltage V_{DD}. (*Example value:* $V_{DD} = 1.2\ V$)
- The input common mode voltage V_{incm} . (*Example value:* $V_{incm} = 600\ mV$).
- Output common mode voltage V_{outcm}. Note that this common mode voltage specification is measured with zero differential input voltage and the input

common mode at whatever value you have chosen. (*Example value:* V_{outcm} = *600 mV*).

- Minimum load capacitance C_{load}. (*Example value:* C_{load} = *100 fF*)
- The unity-gain feedback settling time t_{settle}. The settling time is measured as the time it takes the output to settle to $(1 \pm k) \cdot V_{step}$ under unity-gain feedback with an input step of amplitude V_{step}. Note that with this definition, both dynamic and static errors are included in the settling time calculation. For this problem, the input step is guaranteed to be small, so you shouldn't have to worry about slew rate issues. (*Example value:* t_{settle} = *20 ns, k=0.04,* V_{step} = *20 mV*).

As usual, please submit a single script file that performs the computations need to design the amplifier. For the representative input values, you should print out all of the relevant sizing/biasing results, and you should compute the error between the specified performance and a simulation of the design.