University of California, Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EE240B Spring 2018
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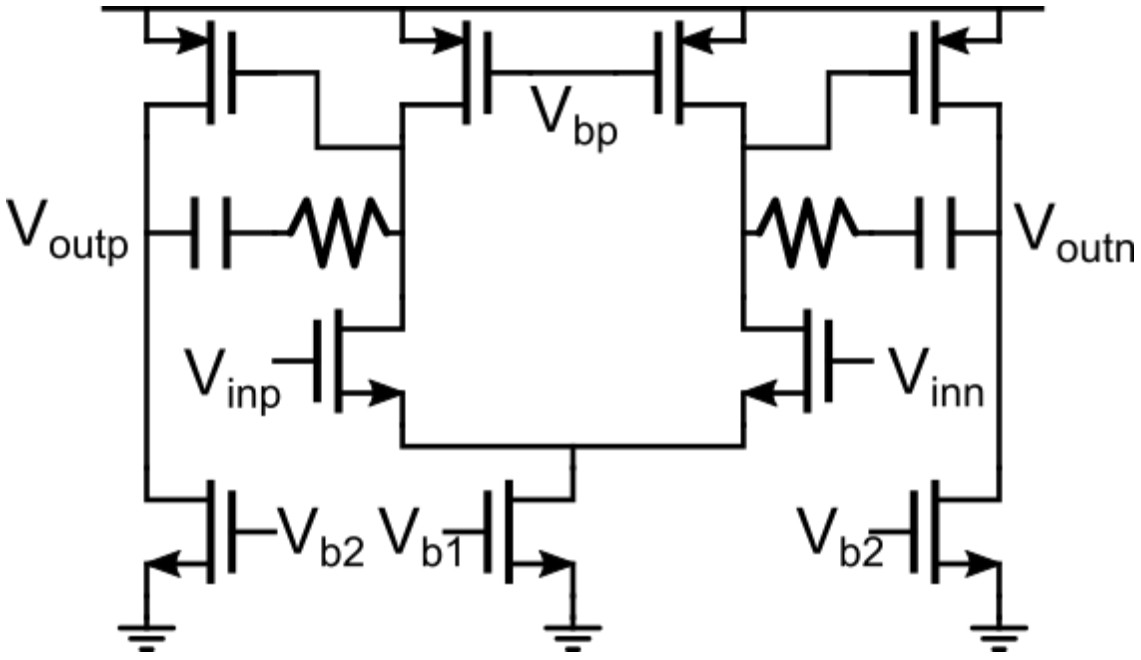
HW4
Due: Thursday, March 22nd at 5pm PST

This is an individual assignment. Make sure that you explain all of your answers.
For these problems you may ignore body effect unless specifically told otherwise.

1. Two-stage OTA design methodology

In this problem, you will be developing a design methodology for a two-stage OTA (shown in the schematic below) given a unity-gain bandwidth, phase margin, and CMRR constraints. Feel free to include additional constraints/assumptions to make the design process easier (especially when you first start). However, you should clearly state these constraints/assumptions, and briefly explain under which conditions these constraints/assumptions may result in a sub-optimal design.



The goal for your methodology should be to minimize the power dissipated by the circuit. The input specifications for your design methodology (generator) are listed below. Along with each specification, for those that are input parameters, we will provide in parentheses representative values that you should use for preliminary evaluations of your methodology.

- Use transistor finger widths of only 0.5µm. You are free to choose the channel length of your device.
- All matched transistors must have the same V^*, channel length, and threshold flavor.
- Since both of the fully differential stages are high output impedance, you must use common-mode feedback to set the biasing for both the first and the second stage. You can assume that V_{bp} is fixed however you'd like it to be, but you should use CMFB to set V_{b1} and V_{b2}.
- Assume resistors have +/- 20% variation in resistance, and the amplifier must meet phase margin/bandwidth constraints in all cases.
- Supply voltage V_{DD}. (*Example value:* V_{DD} *= 1.2 V*).
- Both input and output common mode voltages will be $V_{DD}/2$. You are free to set the common-mode at the output of the first stage however.
- Minimum load capacitance C_{load}. (*Example value:* C_{load} *= 100 fF*)
- The minimum DC gain A_{DC}. (*Example value:* A_{DC} *= 50*).
- The feedback factor F, closed-loop bandwidth f_{CL} and phase margin θ_{PM}. (*Example values: F=0.5,* f_{CL} *= 100 MHz,* $\theta_{PM} = 45°$).
- The minimum value of the common-mode rejection ratio $CMRR_{direct}$. This value must be maintained across the entire closed-loop bandwidth of the OTA. (*Example value:* $CMRR_{direct}$ *= 60 dB*). If you are unsure about how to partition the overall $CMRR_{direct}$ between the two common-mode feedback loops of the two stages, try fixing the $CMRR_{direct}$ of the second stage to 10-20 dB. (Note that without CMFB, the second stage's $CMRR_{direct}$ would be 0 dB, and hence this specification provides the constraints needed to design the second stage CMFB loop.)