EE 240B – Spring 2018

Advanced Analog Integrated Circuits

Lecture 2: MOS Transistor Models

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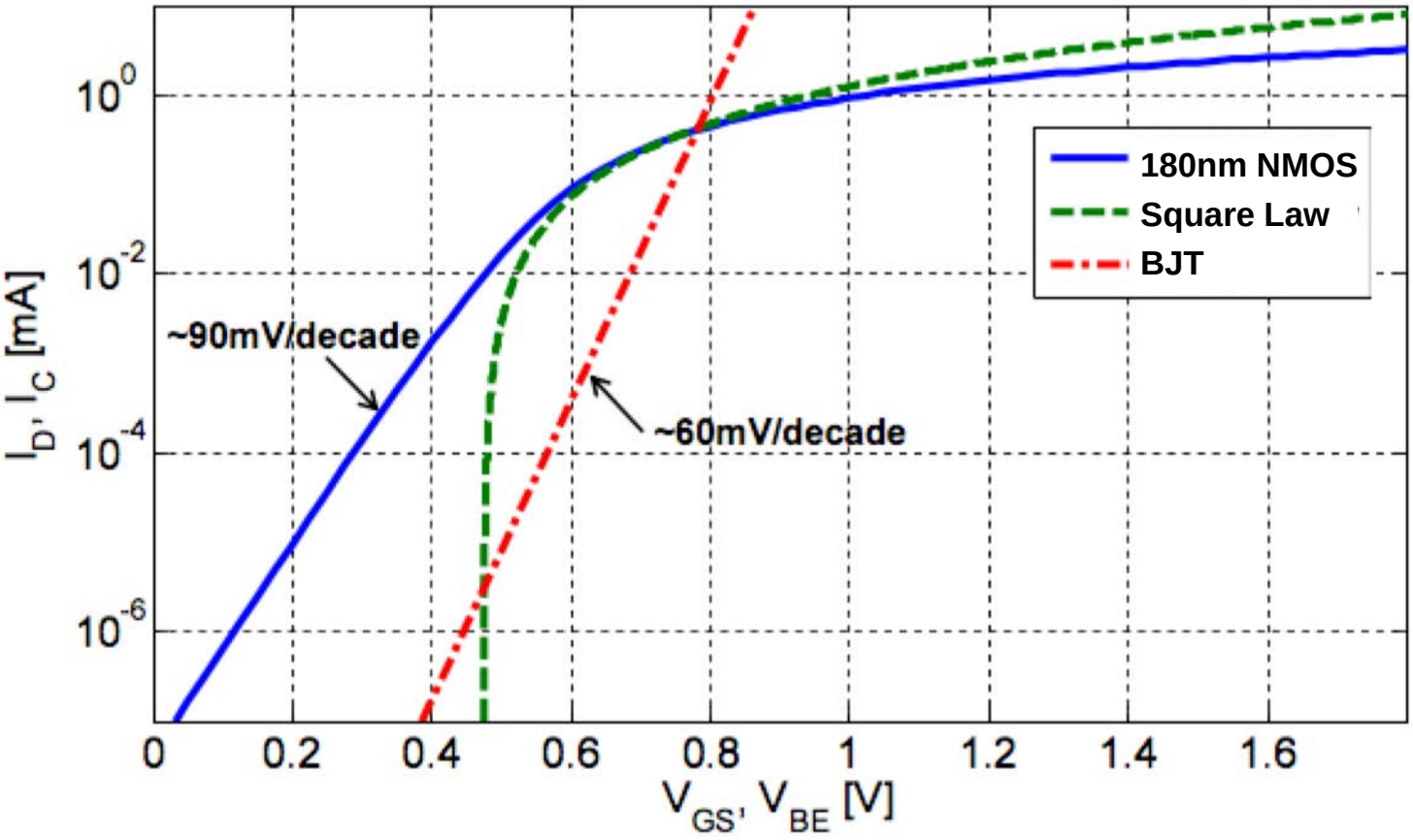
Square Law Model?

$$I_{D,sat} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{th}\right)^2$$

- **Assumptions made to come up with this model:**
  - Charge density determined only by vertical field
  - Drift velocity set only by lateral field
  - Neglects diffusion currents (“magic” Vth)
  - Constant mobility
  - And about 10^2 – 10^3 more parameters in a real SPICE model…

Graphically



[B. Murmann]

Better Hand Models?

- **There are better (less inaccurate) "hand" models out there**
  - Velocity saturation
  - Alpha-power law
  - EKV
  - …
- **But all of them either (1) neglect certain effects or (2) are too unwieldy to be useful for hand analysis**
  - This is particularly true if you want to say anything about r_o (which we do typically care about in analog)

Taking a Step Back

- **Reminder: the model you use should be tailored to the question you are trying to answer**
- **“Hand” models are good for building intuition, and to a lesser extent, checking reasonableness of simulation results**
- **Simulation models are the ones you will have to use to “sign off” on your design**
  - So our design methodology should be using the results from the full simulation models too

Basic Small Signal Transistor Model (for Design)

Biasing…

- **In quadratic model, $V_{od} = (V_{GS} – V_{TH})$ told us a lot about important biasing tradeoffs:**
  - $g_m = 2*I_D/V_{od}$
  - r_o "large" for $V_{DS} > V_{od}$
    - "Boundary between saturation and triode"
  - $\omega_T = g_m/C_{gg} \propto V_{od}$

- **But real transistors clearly aren't quadratic**
  - And even worse, there is no way to actually measure V_{od}

- **Idea: work with a new (measurable) transistor FoM inspired by V_{od}…**

Transistor FoM #1: V* (g_m/I_D)

- **Define:**

$$V^* = \frac{2I_D}{g_m} \quad \Leftrightarrow \quad \frac{g_m}{I_D} = \frac{2}{V^*}$$

e.g. V* = 200mV → g_m/I_D = 10 V^{-1}

- **Inspired by the fact that V* = V_{od} for square law**
- **Devices definitely not square law, but can measure V***
  - It will (by definition) set current efficiency
  - And (approximately) give you insight in to other parameters (r_o, ω_T, etc.)

Simplest Possible Usage of V*

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“Best” Possible V*?

Tradeoff for Low V*

Transistor FoM #2: ω_T

- **Reminder: ω_T defined by $||i_g(\omega_T)|| = ||i_d(\omega_T)||$**
  - Measureable both in simulation and in hardware
  - In our simplified small-signal model, $\omega_T = g_m/C_{gg}$
    - (C_{dd} usually some fixed multiple relative to C_{gg}, so ω_T is a good FoM to capture this too.)

- **Lower V* results in better current efficiency, but lower ω_T**
  - Best balance depends on transistor characteristics, desired gain-bandwidth
  - More on that next lecture

What About L?

- **How does transistor L affect V*?**

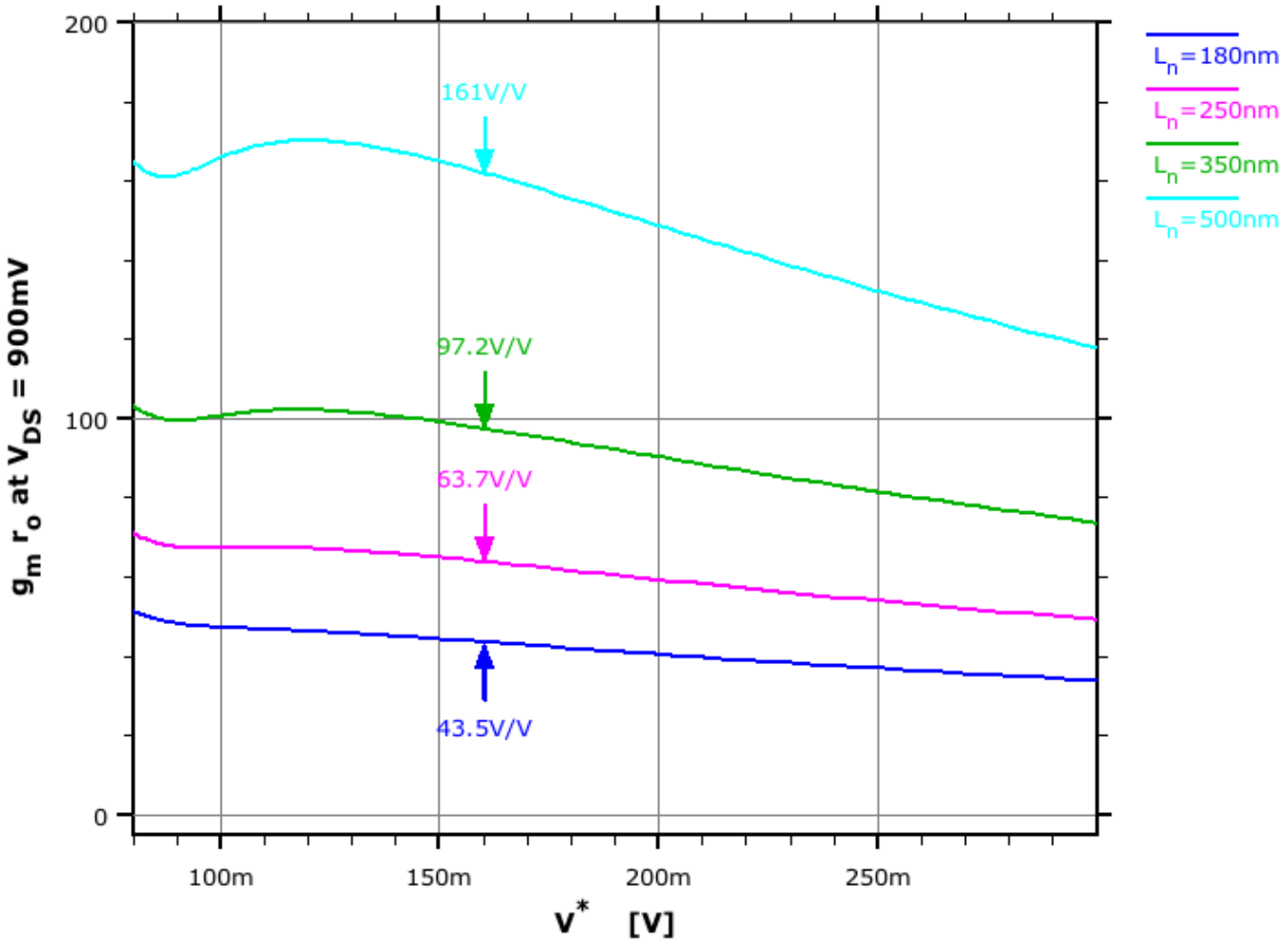
- **How does transistor L affect ω_T?**

Transistor FoM #3: a_{v0}

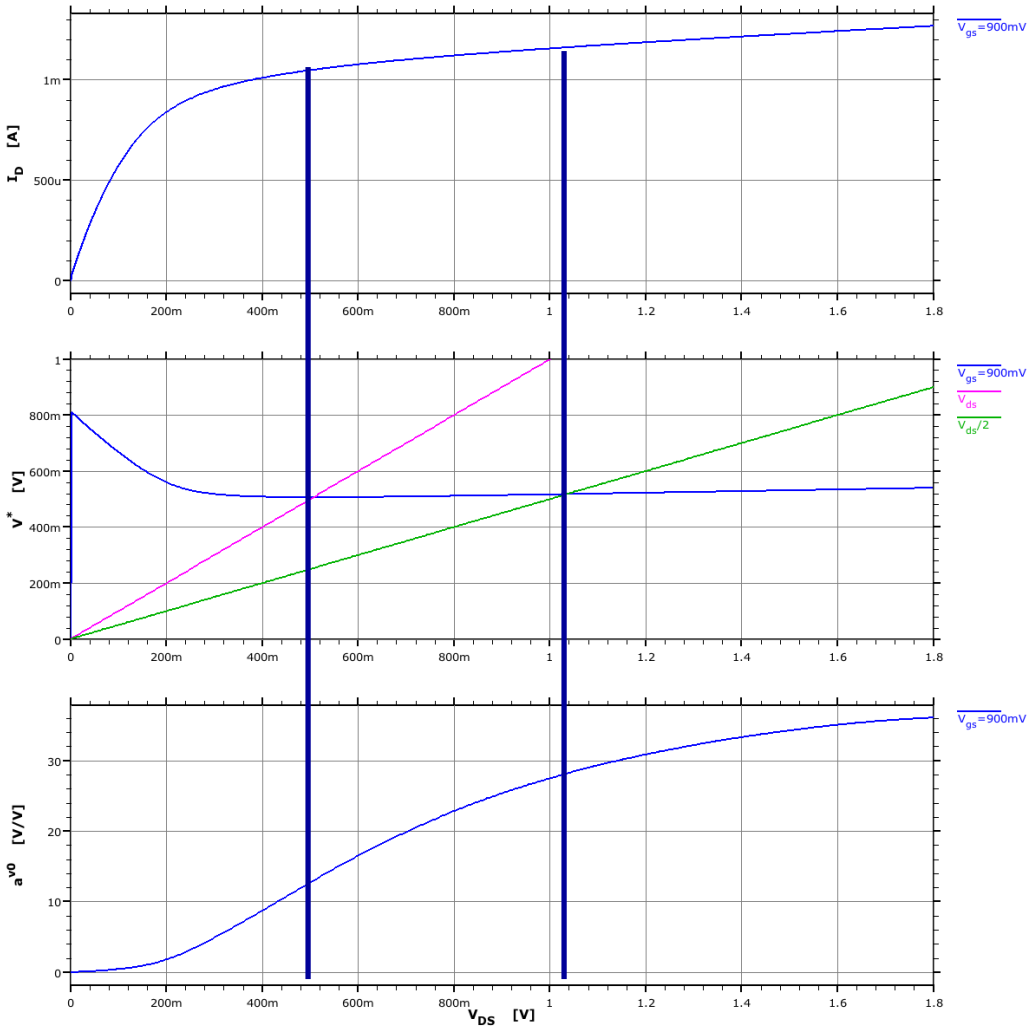
- **Most of the time you don't actually care about value of r_o itself**
  - Just care about how it impacts circuit-level specifications
  - Most commonly, gain (A_V)
- **So, often use intrinsic gain $a_{v0} = g_m * r_o$ instead**
  - Still measurable (from I-V curves) in both simulation and hardware

Example Usage of a_{v0}

Intrinsic Gain vs. L



Intrinsic Gain vs. V_{DS}

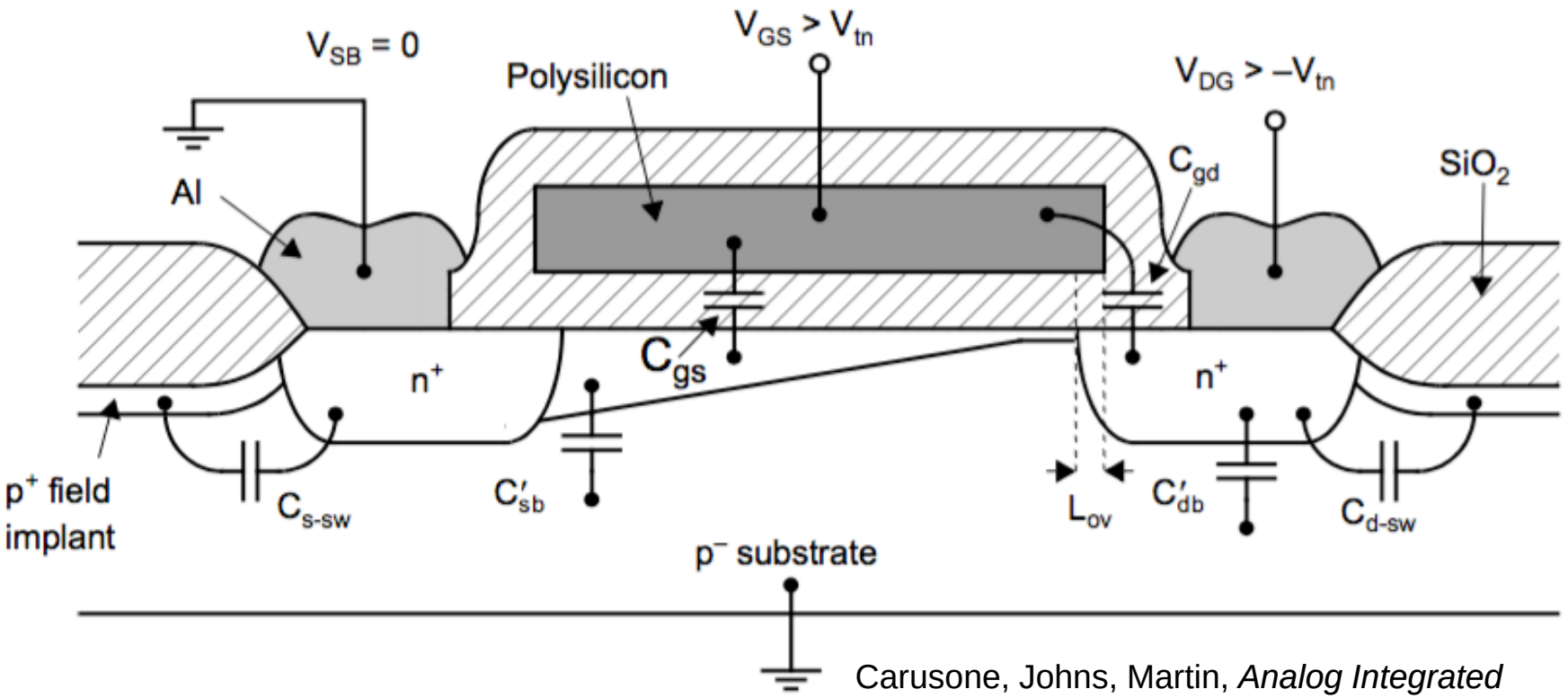


Loose End #1

- **Talked about transistors so far as if they all have the same FoMs for given W, L, V_{GS}, V_{DS}, …**
- **If you have 5 billion transistors on a single chip, do you think all of those transistors behave exactly the same?**
- **If you ship 100 million chips, do you think all of those chips will have the same specifications?**

Process Corners

Loose End #2



Carusone, Johns, Martin, *Analog Integrated Circuit Design,* 2nd Edition, Wiley, 2011, p. 31.

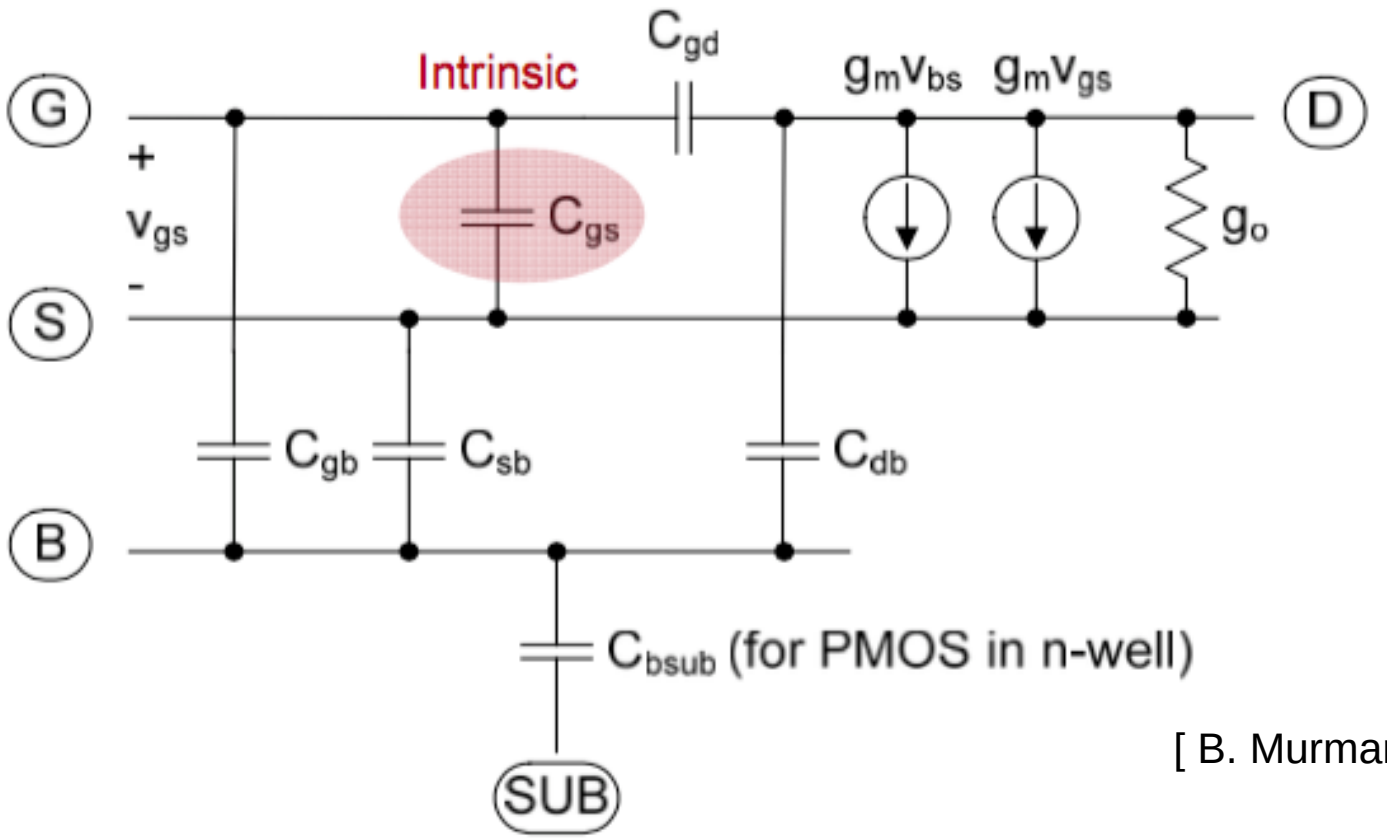
Small Signal Capacitances

	Subthreshold	Triode	Saturation
C_{GS}	C_{ol}	$C_{GC}/2 + C_{ol}$	$2/3\ C_{GC} + C_{ol}$
C_{GD}	C_{ol}	$C_{GC}/2 + C_{ol}$	C_{ol}
C_{GB}	$C_{GC} \parallel C_{CB}$	0	0
C_{SB}	C_{jSB}	$C_{jsB} + C_{CB}/2$	$C_{jsB} + 2/3\ C_{CB}$
C_{DB}	C_{jDB}	$C_{jDB} + C_{CB}/2$	C_{jDB}

$$C_{GC} = C_{ox}WL$$

$$C_{CB} = \frac{\varepsilon_{Si}}{x_d}WL$$

“Complete” Small Signal Model



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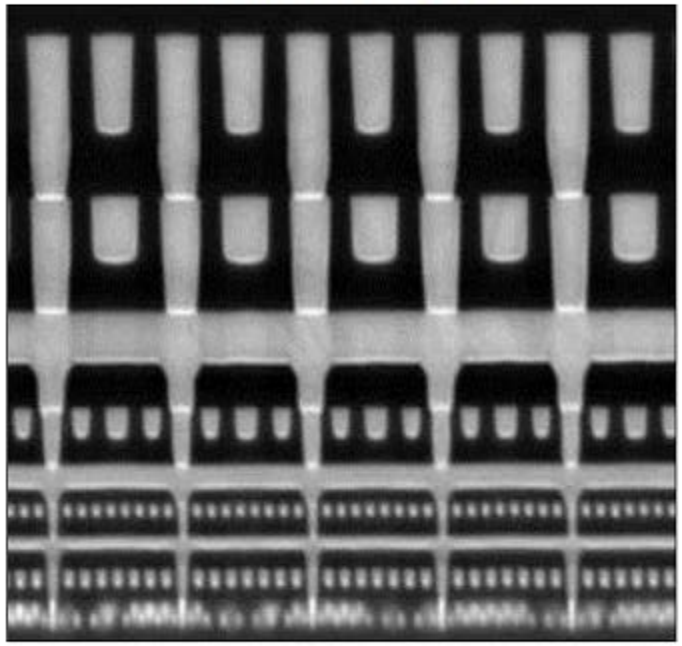
$$C_{gg} = C_{gs} + C_{gb} + C_{gd} \qquad C_{dd} = C_{db} + C_{gd}$$

To Make Matters Worse…

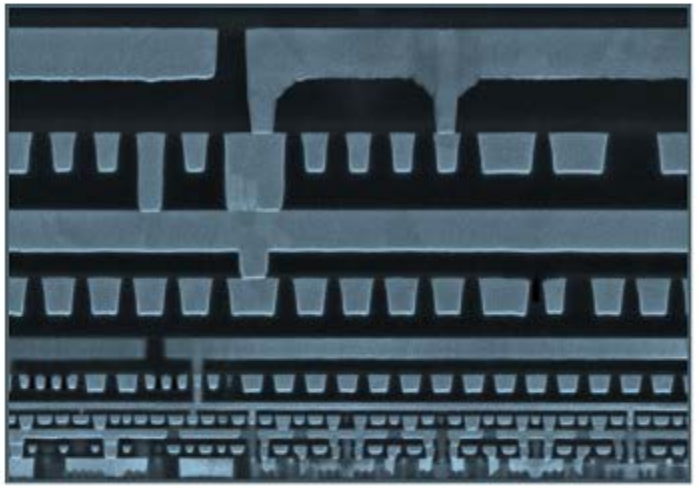
Interconnects

22 nm Process



80 nm minimum pitch

14 nm Process



52 nm (0.65x) minimum pitch

Image from Intel/www.legitreviews.com

“More Complete” Small Signal Model

So What Do We Do?

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Final Note on Simplified Small Signal Model