

# EE 240B – Spring 2018

---

## Advanced Analog Integrated Circuits Lecture 10: Settling-Limited Amplifier Design Methodology



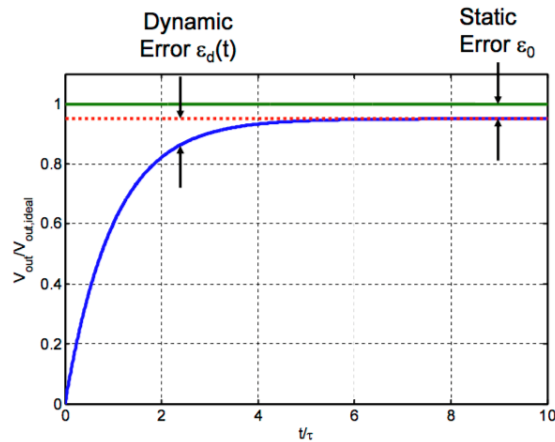
Elad Alon  
Dept. of EECS

## Why “Settling”?

---

- **Really (time-domain) waveform fidelity that is of interest**
  - Often important not just in oscilloscopes
- **Step-response used as a means to characterize this**
  - Sometimes actually dealing with “inputs” that actually look like steps (e.g., switched-capacitor circuits – more later)

## Step Response: Error Breakdown

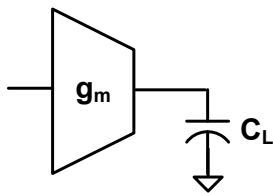


EE 240B

Lecture 10

3

## Simple Settling Limited Amplifier Design Methodology



- **Input specifications:**
  - Supply voltage  $V_{dd}$
  - Minimum small signal gain  $A_v$
  - Maximum relative dynamic settling error  $\epsilon_{dyn}$
- **Goal: minimize power**

EE 240B

Lecture 10

4

## Dynamic Settling Error: Single Pole System

---

EE 240B

Lecture 10

5

## Dynamic Settling Error

---

$\epsilon_d$	$T_{settle}/\tau$
1%	4.6
0.1%	6.9
0.01%	9.2
$10^{-6}$	13.8

EE 240B

Lecture 10

6

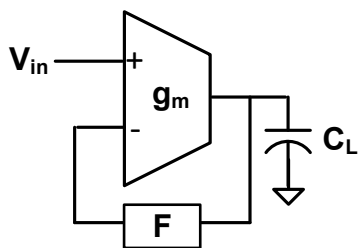
## Methodology Implication

EE 240B

Lecture 10

7

## Settling Limited Amplifier Design Methodology (w/Feedback)



- **Input specifications:**
  - Supply voltage  $V_{dd}$
  - Known “feedback factor”  $F$
  - Maximum relative static settling error  $\epsilon_{stat}$
  - Maximum relative dynamic settling error  $\epsilon_{dyn}$
- **Goal: minimize power**

EE 240B

Lecture 10

8

## **Step Response**

---

EE 240B

Lecture 10

9

## **Static Error**

---

EE 240B

Lecture 10

10

## **Side Note**

---

EE 240B

Lecture 10

11

## **Dynamic Error**

---

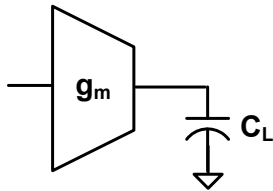
EE 240B

Lecture 10

12

## Simple Settling Limited Amplifier Design Methodology

---



- **Input specifications:**
  - Supply voltage  $V_{dd}$
  - Minimum small signal gain  $A_v$
  - Total settling error  $\epsilon_{dyn} + \epsilon_{stat}$
- **Goal: minimize power**
- **How to allocate between static and dynamic errors?**

EE 240B

Lecture 10

13

## Patching Some Things Up

---

- **Basic methodology doesn't really change**
  - Just that dynamic settling in particular will be affected by things like zeros and additional poles in the OTA
- **Look at these effects next**
  - Good news: (linear) dynamic settling still basically set by OTA  $g_m$  – just get some extra scale factors
  - (Slewing is a little different – will look at that too)

EE 240B

Lecture 10

14

## **Feedforward Zero**

EE 240B

Lecture 10

15

## **Feedforward Example**

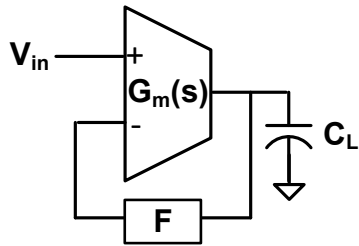
EE 240B

Lecture 10

16



## Second-Order OTA (Cascode)



- Model with:

$$G_m(s) = \frac{g_m}{1 + s/\omega_{p2}}$$

$$\omega_{p2} = K\omega_u$$

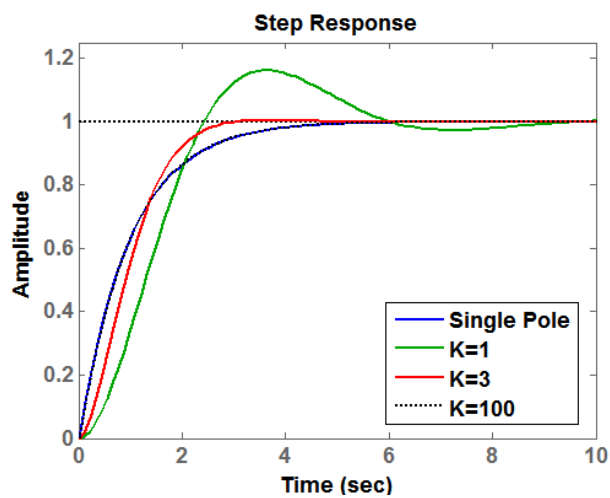
$\omega_u$  is unity gain bandwidth of  $T(s)$

EE 240B

Lecture 10

17

## Step Response

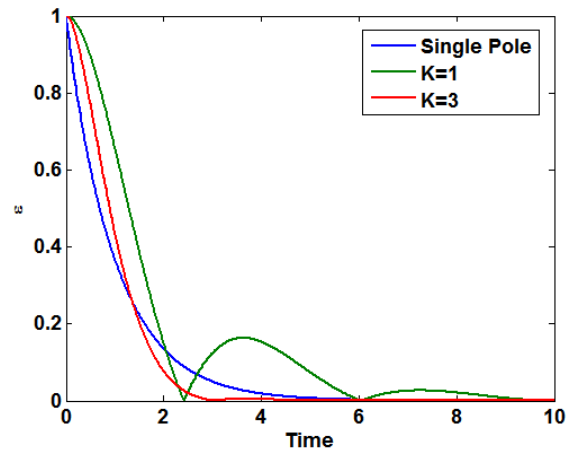


EE 240B

Lecture 10

18

## Dynamic Error

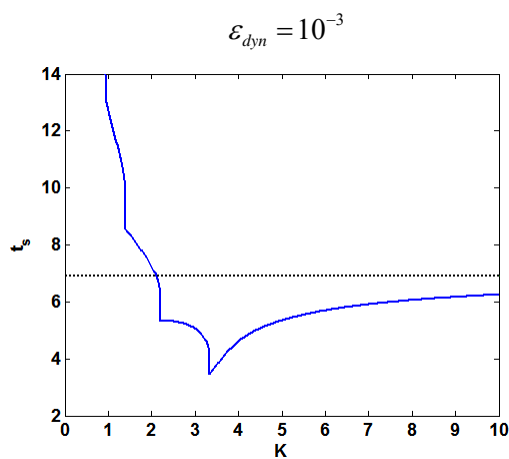


EE 240B

Lecture 10

19

## Settling Time



• Optimum at  $K=3.3$

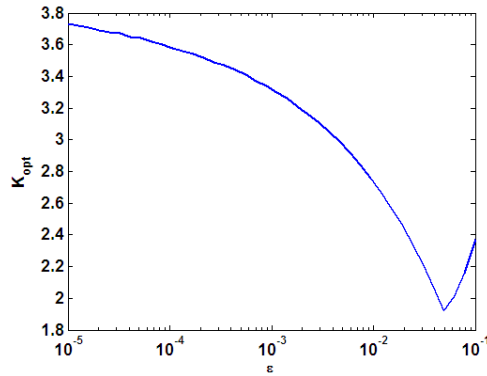
EE 240B

Lecture 10

20

## Optimal K

---



- Optimum K depends on required accuracy
- But always want to avoid  $K < \sim 2$

## Side Note: Pole-Zero Doublets

---

## Feedback and Slewing

---

- **Use of feedback allows you to decouple  $V^*$  from overall “amplifier” linearity**
  - Often intentionally want low  $V^*$  for the  $g_m$  (for current efficiency)
- **When first apply an input step, actual input to OTA may exceed  $V^*$** 
  - This is the source of slewing

## Slewing Model

---

## **Settling Time with Slewing**

EE 240B

Lecture 10

25

## **Putting It All Together**

EE 240B

Lecture 10

26

# Methodology

---