EE 240B – Spring 2018

Advanced Analog Integrated Circuits

Lecture 12: Interference

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Course Material Outline

- **Except for a couple of items we'll look at later, now basically done with "core" amplifier functionality**
- **In many cases though, amplifier design driven not just by core functionality, but by robustness to external interference**
  - Cover some of the sources of interference and how to mitigate them today/next lecture

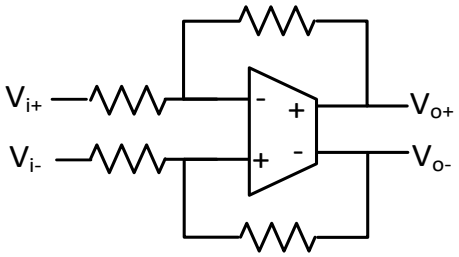
Interference

Typical Interferers

- **Power supplies**
- **Clocks**
- **Digital signals**

- **Electrical interferers can couple in to your circuit:**
  - Directly by capacitive coupling (most common on IC)
  - Directly by inductive coupling (more common on PCB)
  - Indirectly due to finite supply impedance (common everywhere)

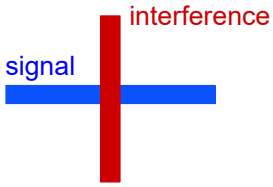
Fully Differential Circuits



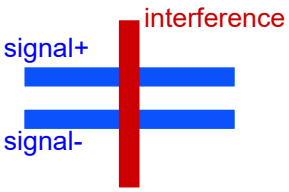
- **Fully differential circuits:**
  - $V_{id} = V_{i+} - V_{i-}$ $\quad V_{ic} = (V_{i+} + V_{i-})/2$
- **Try to make all interfering signals affect only common mode**
  - And "reject" common mode as much as possible

Example

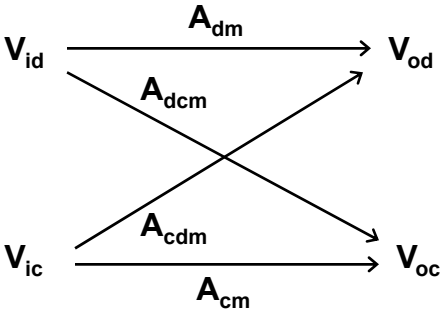
Single Ended



Differential



Fully Differential Amplifier Gains



$$A_{dm} = \frac{v_{od}}{v_{id}} \to \infty$$

$$A_{cm} = \frac{v_{oc}}{v_{ic}} \to 0$$

$$A_{cdm} = \frac{v_{od}}{v_{ic}} \to 0$$

$$A_{VDD} = \frac{v_{od}}{v_{DD}} \to 0$$

$$A_{VSS} = \frac{v_{od}}{v_{SS}} \to 0$$

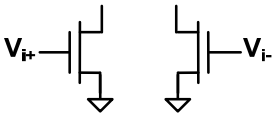
CMRR, PSRR, …

$$CMRR_{direct} = \left|\frac{A_{dm}}{A_{cm}}\right| \to \infty \qquad PSRR_{VDD} = \left|\frac{A_{dm}}{A_{VDD}}\right| \to \infty$$

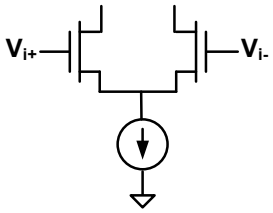
$$CMRR_{cross} = \left|\frac{A_{dm}}{A_{cdm}}\right| \to \infty \qquad PSRR_{VSS} = \left|\frac{A_{dm}}{A_{VSS}}\right| \to \infty$$

PSRR Example

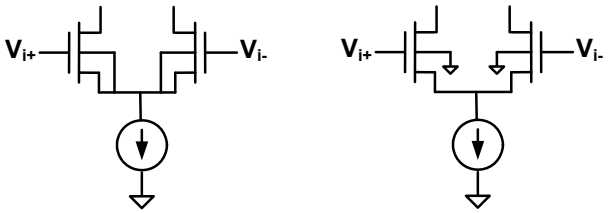
Differential Input Stage Options



Differential Input Stage Options



Side Note



Design Methodology Implications

- **Can "add" a $CMRR_{direct}$ spec to any of our methodologies**
  - Since I_{ss} is fixed by g_m, only degrees of freedom are V_{tail}* and L_{tail}
- **How would you pick V_{tail}* and L_{tail}?**

Design Methodology Implications

- **In practice, need to specify $CMRR_{direct}(f)$ requirement**
  - Could be pairs of f and CMRR, worst-case across range of f, etc.
- **High-f CMRR may limit allowable V_{tail}* and L_{tail}**
  - Sometimes cascode tail for this reason, although can still be hard to maintain high-f CMRR
  - Is there anything else we can do?