EE 240B – Spring 2018

Advanced Analog Integrated Circuits
Lecture 16: Comparators I

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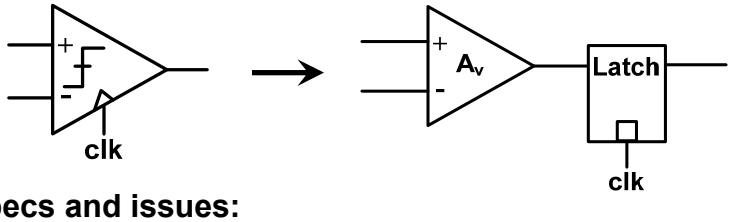
Comparator



- Specs and issues:
  - Clock rate f_s
  - Offset
  - Resolution
  - Hysteresis
  - Input cap
  - Power dissipation
  - CM rejection
  - Kickback noise
  - …

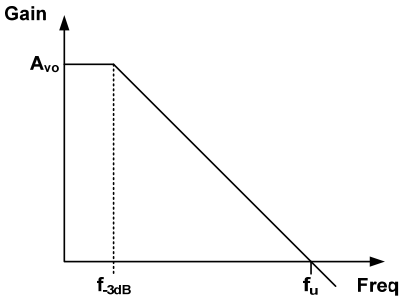
Comparator Gain-Bandwidth

Example:

- **10Gb/s link**
- **Minimum ΔV: 1mV**
- **Vdd = 1V**

→ A_v > 1V / 1mV = 1000 in < 100ps!

Operational Amplifier?

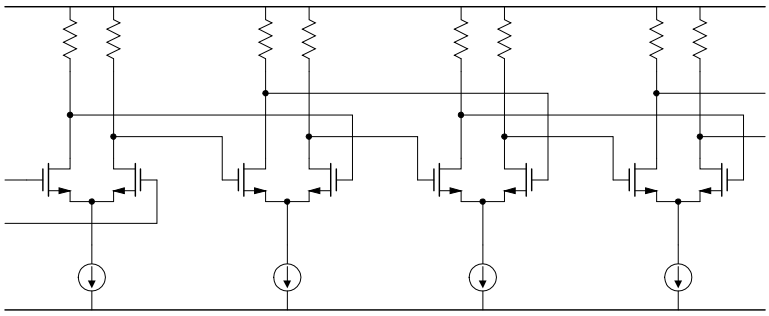


$$f_{-3dB} = \frac{f_u}{A_{vo}} = \frac{2}{3}\frac{1}{T_{bit}}$$

$$f_u = \frac{2A_{vo}}{3T_{bit}}$$

$$= \frac{2}{3}\frac{1000}{100ps} = \underline{6.67THz}$$

Open-Loop Amplifier Cascade



Cascaded Amplifier

- **Simplified bandwidth analysis:**
  - Open-circuit time constants
  - (Not most accurate, but leads to nearly the right answer for design optimization)

Bandwidth/Gain Optimization

Bandwidth/Gain Optimization

Power Consumption

Regenerative Latch

CML Comparator (Latch)

CML Comparator Analysis (1)

CML Comparator Analysis (2)

CML Comparator Design