EE 240B – Spring 2018

Advanced Analog Integrated Circuits
Lecture 18: Matching I

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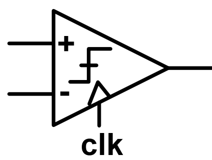
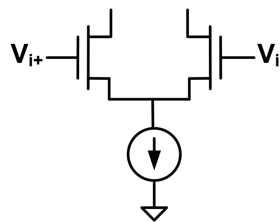
Offset





- **To achieve zero offset, comparator devices must be perfectly matched to each other**
- **How well-matched can the devices be made?**
  - Not arbitrary – direct function of design choices

Device Mismatch Categories

- **Die-to-die**
  - All devices on same chip (or wafer) have same characteristics
- **Within die (long-range)**
  - All devices within certain region have same characteristics
- **Local (short-range)**
  - Every device different, random
  - Usually most important source of mismatch

Sources of Local Variation

- **Deterministic sources:**
  - Local poly density, stress, litho interactions, …
- **Random sources:**
  - Dopant fluctuations
  - Line-edge roughness
  - Oxide traps
- **Focus our modeling on random variations**
  - Deterministic handled with good layout practices

Local Mismatch Statistics

- **Total mismatch set by composite of many single, independent events**
  - Correlation distance << device dimensions
  - E.g., number of dopant atoms implanted into the channel
- **Individual effects are small: linear superposition holds**
- **→ Mismatch is zero mean, Gaussian distribution**

Mismatch Basics

Ref: M. Pelgrom, "Matching Properties of MOS Transistors," JSCC, Oct. 1989

Parameter Mismatch Model

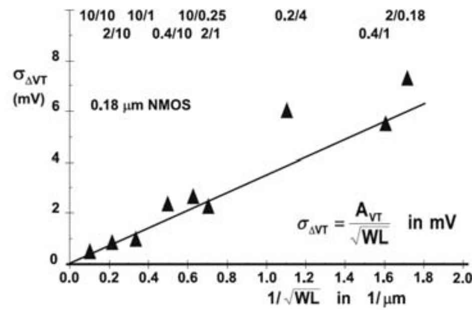
$$\sigma^2(\Delta P) = \frac{A_P^2}{A_D} + S_P^2 D_x^2$$

$\sigma^2(\Delta P)$:	variance of P
A_D :	active device area
D_x :	distance between device centers
A_P :	measured area proportionality constant
S_P :	measured distance proportionality constant,
:	$\cong 0$ for "good" layout

Example Parameters (180nm)

Parameter	Value
A_{Vt} (MOS)	5 mV-μm
A_{β} (MOS)	1 %-μm
$A_{\Delta C/C}$ (MIM capacitor)	1 %-μm
$A_{\Delta R/R}$ (Poly resistor)	3 %-μm

A_{Vt} Data for 180nm



Ref: M. Pelgrom et al, "A designer's view on mismatch," Chapter 13 in Nyquist A/D Converters, Sensors, and Robustness, Springer 2012, pp. 245-67.

- **Good match between model and data, except:**
  - Minimum channel length (actual L smaller than drawn)
  - Very narrow device

Edge Roughness

Edge Roughness Model

Example: β Mismatch

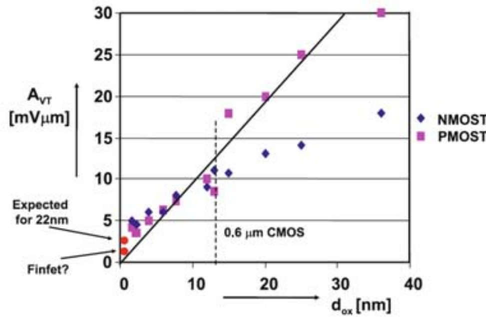
$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{\sigma^2(W)}{W^2} + \frac{\sigma^2(L)}{L^2} + \frac{\sigma^2(C_{ox})}{C_{ox}^2} + \frac{\sigma^2(\mu_n)}{\mu_n^2}$$

For: $\sigma^2(W) \propto 1/L$ and $\sigma^2(L) \propto 1/W$

Simplifies to:

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_L^2}{WL^2} + \frac{A_W^2}{W^2L} + \frac{A_{C_{ox}}^2}{WL} + \frac{A_\mu^2}{WL}$$

Process Dependence



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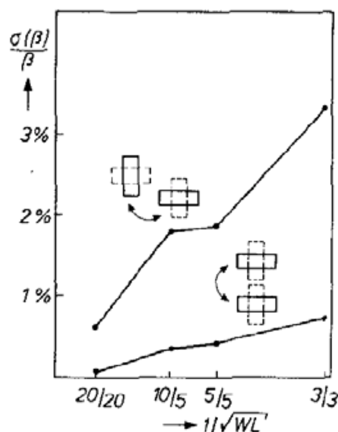
- **A_{Vt} drops by ~1mV*μm for every 1nm drop in gate insulator thickness ("t_{ox}")**
- **Watch out for edge effects in small devices**
- **Fully-depleted channels (FinFET, FDSOI) get 1.5-2X benefit over bulk**

Avoiding Systematic Issues: Orientation Effects



- **Si and transistors are not (perfectly) isotropic**
- **→ keep direction of current flow same!**

"Golden Rule" of Layout for Matching

- **Everything you can think of might matter**
  - **Even whether or not there is metal above the devices**
- **How to avoid systematic errors?**

Ref: **A. Hastings, "The art of analog layout," Prentice Hall, 2001**

Common Centroid Layout

- **Cancels linear gradients**
- **Required for "large" structures (arrays)**