EE 240B – Spring 2018

Advanced Analog Integrated Circuits
Lecture 19: Matching II

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Computing Mismatch Variance

- **Same basic approach as noise computations**
  - Assume each mismatch source is “small” and adds to the others linearly
  - So can use superposition to find effect of each source and then add them all up

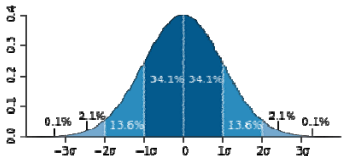
Current Matching

Voltage Matching

Yield

- **Just like noise, can only put a statistical bound on mismatch**
  - So define "yield" as fraction of parts with target parameter being less than some specification

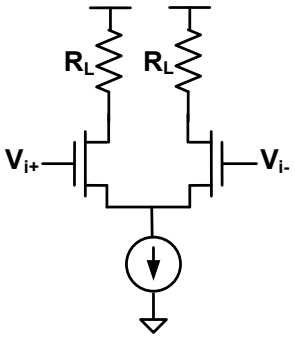
Interval	Yield	Fraction Bad
2σ	95.4%	1/22
3σ	99.7%	1/370
4σ	99.99%	1/16,000
5σ	99.999%	1/1,700,000
6σ	99.999 999 8%	1/507,000,000



- **Given target parameter and yield:**
  - $N_{\sigma,yield}\sigma_{\Delta P} = \Delta P_{targ}$

Note About Yield

Mismatch-Limited Design Methodology



- **Input specifications:**
  - Minimum small signal gain A_v
  - Minimum 3dB bandwidth ω_{bw}
  - Fixed capacitive load C_L
  - Supply voltage V_{dd}
  - Maximum input-referred offset V_{off} at required yield level c_{yield}
- **Goal: minimize power**

Mismatch-Limited Design Methodology

Mismatch-Limited Design Methodology

Important Things To Note

How to Simulate Mismatch

- **Brute force: Monte Carlo**
  - **HSPICE "throws the dice"…**

How I Handle Mismatch

Note About Extracting Mismatch Parameters from Simulation