EE 240B – Spring 2018

Advanced Analog Integrated Circuits
Lecture 22: Discrete Time Circuits

Elad Alon
Dept. of EECS

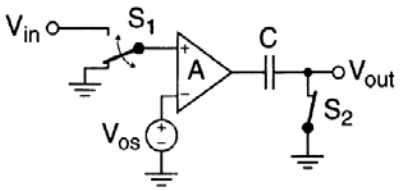
Discrete Time Systems

- **Focused on everything in continuous time so far**
  - But most communication systems (like our link) are of course discrete time
  - And even sensor systems usually end up going through some sampling process at the end (usually for data-conversion)
- **Can we make use of the fact that signals are discrete-time to improve our circuits?**
  - Or at least get around some of the issues we've encountered before?

Ex 1: Offset Cancellation

- **Don't want to store offset on capacitors for extended time periods**
  - But if refresh the capacitor value every sample, may not be so bad…
  - General category of these techniques known as "correlated double sampling"

CDS #1: Output Offset Cancellation



Phase 1:

$$V_C = -AV_{os}$$

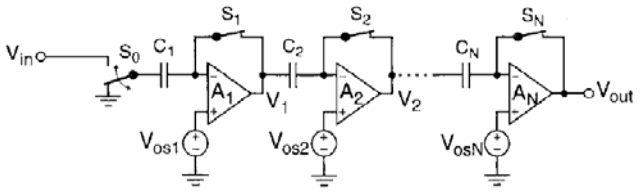
Phase 2:

$$V_{out} = A(V_{in} - V_{os}) - V_C$$
$$= AV_{in}$$

- **Relatively insensitive to switch errors**
  - **Storing amplified offset**
- **But, what happens if gain is large?**

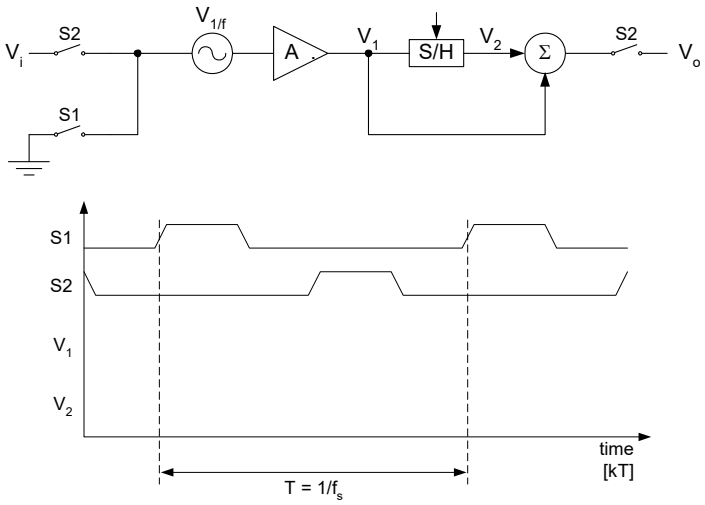
CDS #2: Input Offset Cancellation

Multistage Cancellation



- Open switches left to right
  - Errors from S_1 … S_{N-1} cancelled by final stage
- Application: continuous time comparators

CDS and Flicker Noise



Flicker Noise Analysis

$$V_o(kT) = A\left\{\underbrace{V_i(kT)}_{\text{signal}} + \underbrace{V_{1/f}(kT) - V_{1/f}\left(kT - \frac{T}{2}\right)}_{\text{input referred error } V_{nieq}}\right\}$$

Laplace Transform

Delay by t_d $\rightarrow$ e^{-st_d}

$$V_{nieq}(s) = V_{1/f}(s)\underbrace{\left\{1 - e^{-s\frac{T}{2}}\right\}}_{H_n(s)}$$

Ex 2: Large Resistors

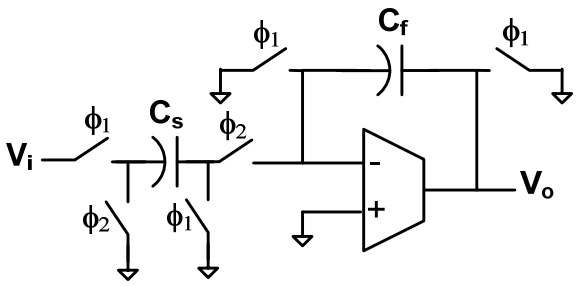
- **Saw that we wanted large resistors in e.g. common-mode extractor or feedback network (to minimize OTA DC gain reduction)**
  - Not uncommon to want resistors in the MΩ to GΩ range…
  - These kinds of resistors usually take a lot of area, hence have high parasitic capacitance…

Switched Cap. Resistor

Aside: Switched Cap Low-Pass Filter

Switched-Cap. R Feedback?

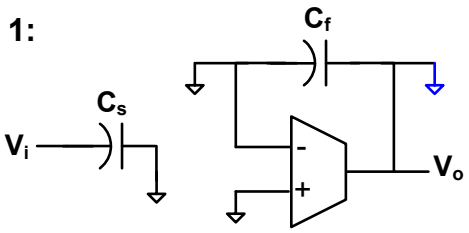
Switched-Capacitor Gain Stage



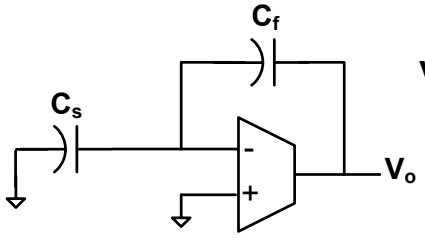
- **Many possible topologies – one example shown here**
- **Clocks generally non-overlapping**

SC Gain Stage Phases

- **Phase 1:**



- **Phase 2:**



V_o/V_i =

SC Gain Stage Noise

SC Gain Design Methodology

Ex 3: Lowering Power

Alternative Waveform

Typical Implementation

Current Integration Design Methodology (GBW)

Current Integration Design Methodology (Noise)

Current Integration Design Methodology (Noise)