EE 240B – Spring 2018

Advanced Analog Integrated Circuits
Lecture 24: Sampling in CMOS

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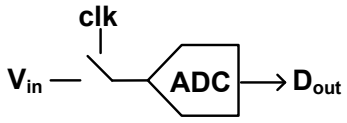
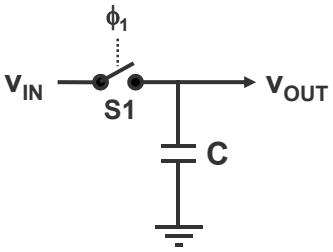
Sampling

- **Even in a communication system where signal was originally discrete time**
  - Any non-idealities in the communication channel or circuits will result in continuous time variations
- **So, often want or need to sample the signal so that it actually becomes constant over some period**
  - Most often achieved with a switch



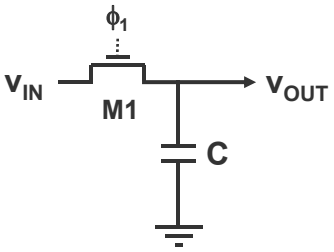
MOS Track & Hold

Ideal Sampling



- Grab exact value of V_{in} when switch turns off

Practical Sampling

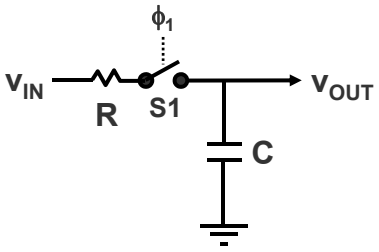


- kT/C noise
- Limited bandwidth
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection
- Clock jitter, leakage, …

Switch Resistance

Acquisition Bandwidth

- **Finite switch R → finite bandwidth**
- **Assuming constant V_{in} and C starts at 0V:**

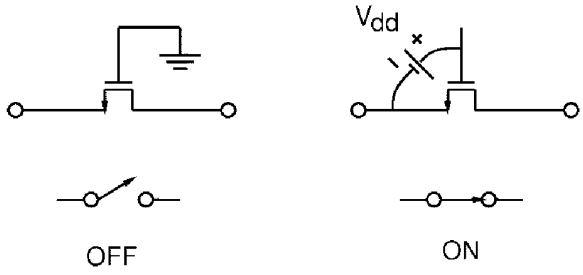


$$v_{out}(t) = v_{in}\left(1 - e^{-t/\tau}\right)$$

- **Leads to min. switch size for given bandwidth, resolution**
  - Linear settling calc. – remember may only get T/2
- **(Will C always start at 0V?)**

Switch R_{on} Non-Linearity

Constant V_{GS} Sampling



- Switch overdrive voltage is independent of signal
- Error from finite R_{ON} is linear (to first order)

Constant V_{GS} Sampling Circuit

Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

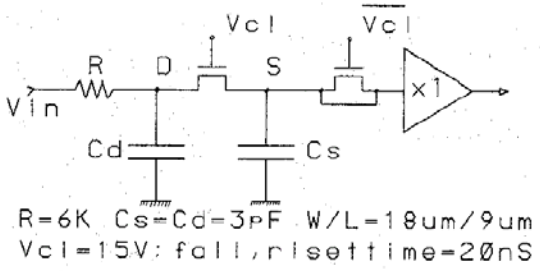
Charge Injection

- **"Extra" charge dumped onto holding capacitor**
  - Channel charge has to go somewhere
  - (Also get charge from parasitic gate capacitance)
- **Problems:**
  - Offset
  - Distortion (error charge is function of V_{IN})

Charge Injection Analysis

Ref: Wegmann, "Charge Injection in Analog MOS Switches," JSSC, Dec. 1987.

Dummy Switch



Vin	UNCOMPENSATED SWITCH	COMPENSATED WITH DUMMY	BALANCED SWITCH
0v	-160mV	-45mV	6mV
5v	-105mV	-30mV	1mV
10v	-40mV	-11mV	0.5mV

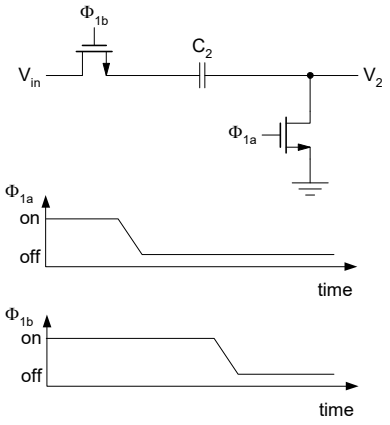
- **Dummy switch is half width**
- **Depends on equal charge split between source and drain**

Ref: Bienstman et al, JSSC 12/1980, pp. 1051.

Eichenberger et al, JSSC 8/1989, pp. 1143.

Rejecting Injection Error

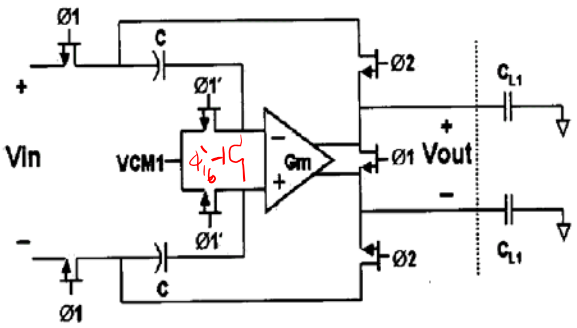
Bottom-Plate Sampling



- Turn off Φ_{1a} first
  - Injected charge is constant
  - Removed in differential output
- Switch Φ_{1b} opens later
  - C_2 disconnected → "zero" charge injected
- Is this useful?
  - V2 = 0V…

Using Bottom-Plate Sampling

Flip-Around Track and Hold



Ref: W. Yang, D. Kelly, I. Mehr, M. T. Sayuk, and L. Singer, "A 3-V 340mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE Journal of Solid-State Circuits,* vol. 36, pp. 1931 - 1936, December 2001.