University of California, Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EE240B Spring 2018
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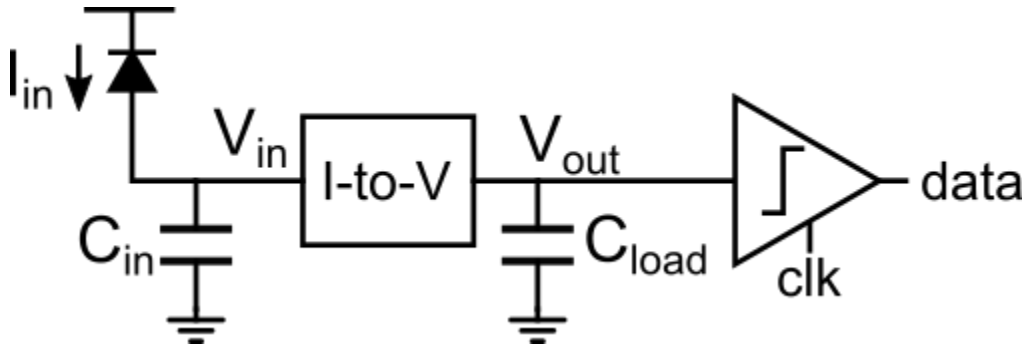
Project Phase I
Due: Thursday, April 5th at 5pm PST

For this project, you are allowed to use technologies other than GPDK 45nm if you have access to them. Please be warned however that our ability to support you on with specific setup-related issues on processes other GPDK 45nm may be limited.

In this first phase of the project, we will be exploring the design of a TIA for a high speed photonic link. Below is a conceptual schematic showing how this amplifier is used.



As with previous homeworks, during the project you are expected to develop a design methodology for this photonic link given input specifications. Since the full link will eventually be complex enough that you will want to build you methodology in a hierarchical manner, we will give you a taste of that by breaking this phase down in to two parts that will be described next.

1. Amplifier Design Methodology

In this part, you will develop a design methodology for the TIA given gain-bandwidth constraints, with the goal of minimizing power. To prove that your design methodology is flexible with input specifications, you will need to submit two instances of your TIA targeting the following two sets of specifications. Note that the phase margin specification is only applicable if you use a feedback-based topology.

Supply voltage V_{DD}	1.2 V	1.2 V
Trans-impedance gain R_{dc}	8 kΩ	3 kΩ
3-dB bandwidth f_{3dB}	4.0 GHz	4.0 GHz
Phase margin ϕ_{PM}	45°	45°
Photo-diode capacitance C_{in}	20 fF	100 fF
Load capacitance C_{load}	40 fF	40 fF

(Please note that if you use a process technology other than the 45nm GPDK, this particular set of specifications may or may not be feasible. Especially if you are using a substantially different process, please consult with the teaching staff early on about what an appropriate set of specs to target would be.)

Your submission for this part should include:

1. A single design script file that executes your design methodology. If you introduce any extra constraints/constants in addition to the specifications list above (i.e. V^*, channel length, threshold voltage flavor, etc.) to simplify your design process, list their values clearly at the beginning of your script.
2. A concise, clear description of your design script. Somewhere between 1-3 paragraphs should be sufficient.
3. Two clearly labeled schematics of your design for the two sets of specifications. Include device sizes, nominal bias current/voltages, and component values in your schematic.
4. The following simulation plots for both sets of specifications.
    a. A Bode plot including both magnitude and phase response. Clearly label the DC gain and the 3-dB bandwidth of the TIA.
    b. If you use a feedback-based topology, any simulation plots that shows the phase margin specification is met. You can either use stability analysis in ADEXL, or the Middlebrook method discussed in class.

2. High-speed Photonic Link Design Methodology

In this part, you will develop a design methodology for the photonic receiver above, using an ideal comparator (zero delay, works with any positive inputs amplitude and bias voltage). You will need to design your TIA for minimum power while meeting the two sets of specifications below:

Supply voltage V_{DD}	1.2 V	1.2 V
Bit period T_{per}	200 ps	200 ps
Bit error rate BER	10^{-12}	10^{-12}
Input peak-to-peak swing I_{sw}	10 μA	20 μA
Comparator offset V_{off}	20 mV	20 mV
Photo-diode capacitance C_{in}	20 fF	100 fF
Comparator input capacitance C_{load}	40 fF	40 fF

For this part, you should take advantage of your design script from part 1. Your submission should include:

1. A single design script file that executes your design methodology. If you introduce any extra constraints/constants in addition to the specifications list above (i.e. V^*, channel length, threshold voltage flavor, etc.) to simplify your design process, list their values clearly at the beginning of your script.
2. A concise, clear description of your design script. Somewhere between 1-3 paragraphs should be sufficient.
3. Two clearly labeled schematics of your design for the two sets of specifications. Include device sizes, nominal bias current/voltages, and component values in your schematic.
4. The following simulation plots for both sets of specifications.
    a. A Bode plot including both magnitude and phase response. Clearly label the DC gain and the 3-dB bandwidth of the TIA.
    b. The transient output eye diagram with PRBS7 input data, with the width/height of the eye clearly labeled. A separate tutorial will be posted on the website on how to perform this measurement.
    c. The output noise power spectral density and the output voltage standard deviation.