EE241B : Advanced Digital Circuits

Lecture 23 – Energy Optimization

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Spending $50B on the Chip Industry is a Challenge, EETimes

Chip industry executives have a huge collective challenge: deciding how to prioritize the $50 billion in support promised by President Joseph R. Biden in an executive order. Semiconductor industry executives met virtually with President Biden to discuss the issues around chip capacity and supply chain. Neither the Semiconductor Industry Association (SIA) nor the White House readouts of the meeting told us anything new. The President did acknowledge however that the $50 billion support package is not likely to be enough, stating, “We are seeking a significant investment in this piece of legislation. It’s important, but we know it’s not sufficient.”

Announcements

• Assignment 4 due this Friday
  • Quiz next Tuesday
• Final next Thursday, April 29, 9:40-11
  • In class, 80 min
• Project reports due on Monday, May 3, 9am
  • Presentations on Monday afternoon
Outline

• Optimal thresholds and supplies
• Clock generation

5.0 Optimal $V_{DD}$, $V_{Th}$
Adapting $V_{DD}$ and $V_{TH}$

- Adapting both $V_{DD}$ and $V_{TH}$ during runtime
- $V_{TH}$ is much less sensitive

Miyazaki, ISSCC’02
Adapting $V_{DD}$ and $V_{TH}$

- Adjusting $V_{DD}$, $V_{TH}$ trades of energy and delay
- We studied energy-limited design
  - And alternate ways for optimizing energy and delay together
  - E.g. energy-delay product (EDP)
  - Or $E^nD^m$, $n,m > 1$
Optimal EDP Contours

- Plot of EDP curves in $V_{dd}$, $V_{th}$ plane

Gonzalez, JSSC 8/97

Sizing, Supply, Threshold Optimization

Reference Design:
$D_{ref} (V_{dd}^{max}, V_{th}^{ref})$

<table>
<thead>
<tr>
<th>Topology</th>
<th>Inverter</th>
<th>Adder</th>
<th>Decoder</th>
</tr>
</thead>
<tbody>
<tr>
<td>(E_{L}/E_{Sw})^{ref}</td>
<td>0.1%</td>
<td>1%</td>
<td>10%</td>
</tr>
</tbody>
</table>

Large variation in optimal circuit parameters $V_{dd}^{opt}$, $V_{th}^{opt}$, $w^{opt}$

Technology parameters $(V_{dd}^{max}$, $V_{th}^{ref})$ rarely optimal
**Result: E-D Tradeoff in an Adder**

Energy-efficient curve $f(W,Vdd,Vth)$

<table>
<thead>
<tr>
<th>Sensitivity</th>
<th>W</th>
<th>Vdd</th>
<th>Vth</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{ref}, E_{ref}$</td>
<td>$\infty$</td>
<td>1.5</td>
<td>0.2</td>
</tr>
<tr>
<td>$D_{ref}, E_{min}$</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$D_{min}, E_{ref}$</td>
<td>22</td>
<td>16</td>
<td>22</td>
</tr>
</tbody>
</table>

- **80% of energy saved without delay penalty**
- **40% delay improvement without energy penalty**

**Energy-constrained delay**

- **Active power**
  \[ P_{act} = \alpha f CV_{DD}^2 \]
  \[ f = 1/LDt_p \]

- **Leakage power**
  \[ P_{\text{leak}} = I_0 e^{-\frac{V_{th} - \gamma V_{DD}}{s}} V_{DD} \]

- Eliminate one variable ($V_{th}$) and find $P_{\text{min}}(V_{DD})$

Nose, ASP-DAC'00
Minimum energy: \( E_{Sw} = 2E_{Lk} \)

- Large \( \frac{E_{Lk}}{E_{Sw}} \) \( \)opt
- Flat \( E_{Op} \) minimum
- Topology dependent

\[
\left( \frac{E_{Lk}}{E_{Sw}} \right)_{opt} = \frac{2}{\ln \left( \frac{L_d}{\alpha_{avg}} \right) - K}
\]

Optimal designs have high leakage \( \frac{E_{Lk}}{E_{Sw}} \approx 0.5 \)

Subthreshold Optimum

\( f = 30kHz \)

Minimum is independent of \( V_T \)

Calhoun, JSSC 9/05
6. Clocks and Supplies

Clock Subsystem

- Clock Generation
- Clock Distribution
- Synchronization
Clock Subsystem

- Intel Xeon – Bowhill, ISSCC’15
  - Independent clocks for 4-18 cores
- Self-biased (SB) and LC PLLs

6.B Clock Generation
Clock Generation

Delay-Locked Loop (Delay Line Based)

Phase-Locked Loop (VCO/DCO-Based)

PLL Signals
Loop Performance

- Ideal clock
- Clock with jitter
- Phase offset, peak-to-peak jitter, RMS jitter
- Bandwidth, locking time, frequency range

Phase Detector

- Detects the phase difference

\[ V_{out} = K_{PD} \cdot \Delta \phi \]
Delay-Locked Loop

- First order loop: inherently stable
- No filtering of input jitter
- Constant frequency (no synthesis)
- No phase error accumulation

KPD

Charge Pump \( I_{CP} \)

KDL

\( f_{REF} \)

\( f_{O} \)

\( K_F \)

DLL Locking

\( F_{REF} \)

\( \Delta PH \)

Phase detect

Charge pump

\( V_{CTRL} \)

VCDL

\( F_O \)

REF

OUT

UP

DN

\( \Delta PH \)

\( V_{CTRL} \)

Delay

Delay-Locked Loop

\[ \frac{D_O(s)}{D_I(s) - D_O(s)} = K_{PD} \frac{1}{sC} I_{CP} K_{DL} F_{REF} = \frac{1}{s} K_{PD} K_F K_{DL} \]

Closed loop transfer function

\[ H(s) = \frac{D_O(s)}{D_I(s)} = \frac{K_{PD} K_F K_{DL}}{s + K_{PD} K_F K_{DL}} \]

- \( \omega_N > \) an order of magnitude below \( F_{REF} \)
- Use of DLLs requires low-jitter input
- VCDL must span adequate delay range + reset to min delay
- Noise sources:
  - Delay line (Supply sensitivity)
  - Clock buffers that follow
  - Device noise (small)
Voltage-Controlled Delay Line

- Delay controlled by voltage with proportionality $K_{DL}$
Next Lecture

• Optimal supplies and thresholds
• Clocking