EE C245 – ME C218
Introduction to MEMS Design
Fall 2007

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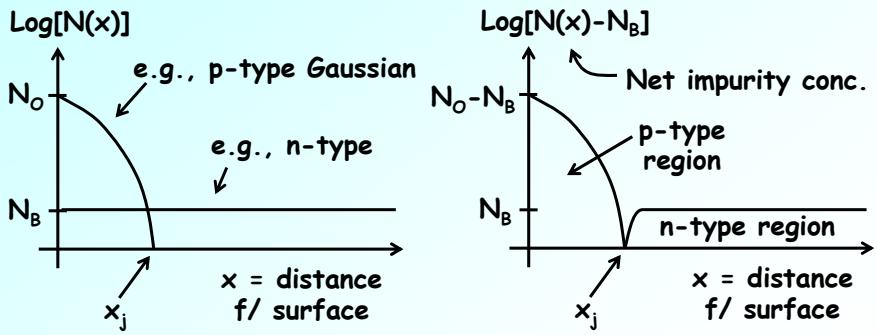
Lecture 8: Surface Micromachining

Lecture Outline

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handout: "Surface Micromachining for Microelectromechanical Systems"
- Lecture Topics:
  - Finish diffusion
  - Polysilicon surface micromachining
  - Stiction
  - Residual stress
  - Topography issues
  - Nickel metal surface micromachining
  - 3D "pop-up" MEMS
  - Foundry MEMS: the "MUMPS" process
  - The Sandia SUMMIT process

Metallurgical Junction Depth, x_j

x_j = point at which diffused impurity profile intersects the background concentration, N_B



Expressions for x_j

- Assuming a Gaussian dopant profile: (the most common case)

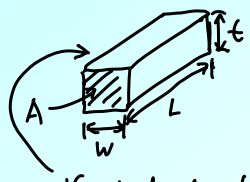
$$N(x_j,t) = N_o \exp\left[-\left(\frac{x_j}{2\sqrt{Dt}}\right)^2\right] = N_B \quad \rightarrow \quad x_j = 2\sqrt{Dt\ln\left(\frac{N_o}{N_B}\right)}$$

- For a complementary error function profile:

$$N(x_j,t) = N_o \mathrm{erfc}\left(\frac{x_j}{2\sqrt{Dt}}\right) = N_B \quad \rightarrow \quad x_j = 2\sqrt{Dt}\,\mathrm{erfc}^{-1}\left(\frac{N_B}{N_o}\right)$$

Sheet Resistance

- Sheet resistance provides a simple way to determine the resistance of a given conductive trace by merely counting the number of effective squares
- <u>Definition</u>:



uniformly doped material w/ resistivity $\rho = \frac{1}{\sigma}$

σ = conductivity = $q(\mu_n n + \mu_p p)$

$$R = \frac{\rho L}{A} = \left(\frac{\rho}{t}\right)\frac{L}{W} = R_s\left(\frac{L}{W}\right)$$

[A = tW]

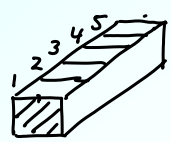
sheet resistance

unit squares of material in the resistor

ohms per square

Ω/□

e.g.,

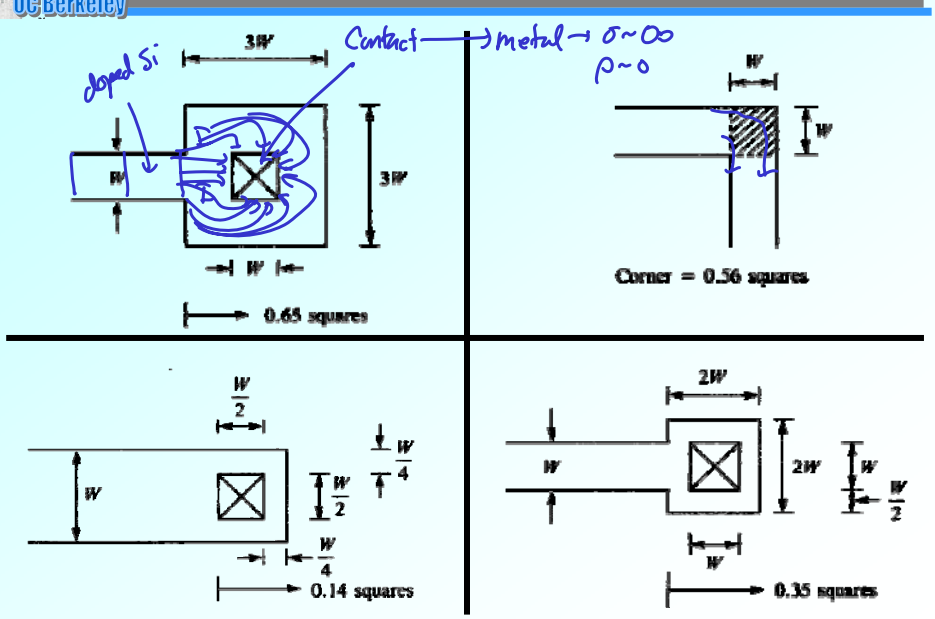


→ 5 □'s of material

∴ $R = R_s \times 5$

- What if the trace is non-uniform? (e.g., a corner, contains a contact, etc.)

Squares From Non-Uniform Traces



Sheet Resistance of a Diffused Junction

- For diffused layers:

Majority carrier mobility

Sheet resistance

Effective resistivity

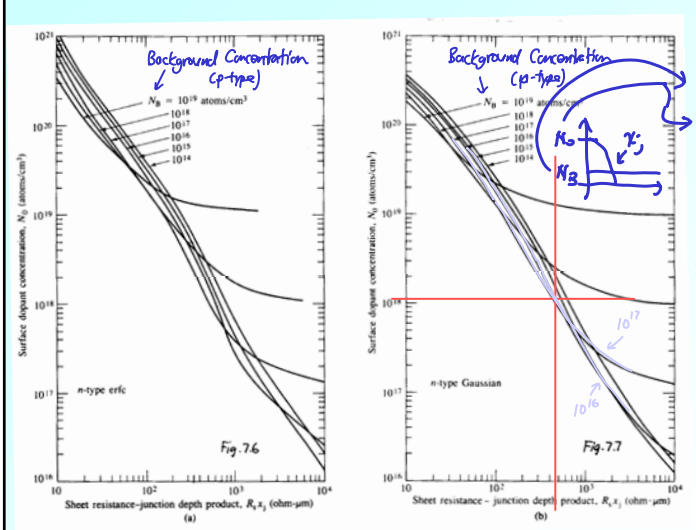
Net impurity concentration

$$R_s = \frac{\bar{\rho}}{x_j} = \left[\int_o^{x_j} \sigma(x)dx\right]^{-1} = \left[\int_o^{x_j} q\mu N(x)dx\right]^{-1}$$

[extrinsic material]

- This expression neglects depletion of carriers near the junction, x_j → thus, this gives a slightly lower value of resistance than actual
- Above expression was evaluated by Irvin and is plotted in "Irvin's curves" on next few slides
  - Illuminates the dependence of R_s on x_j, N_o (the surface concentration), and N_B (the substrate background conc.)

Irvin's Curves (for n-type diffusion)



Example.

Given: p-type

$N_B = 3\times10^{16}$ cm^{-3}

$N_o = 1.1\times10^{18}$ cm^{-3}

(n-type Gaussian)

$x_j = 2.77$ μm

Can determine these given known predep. and drive conditions

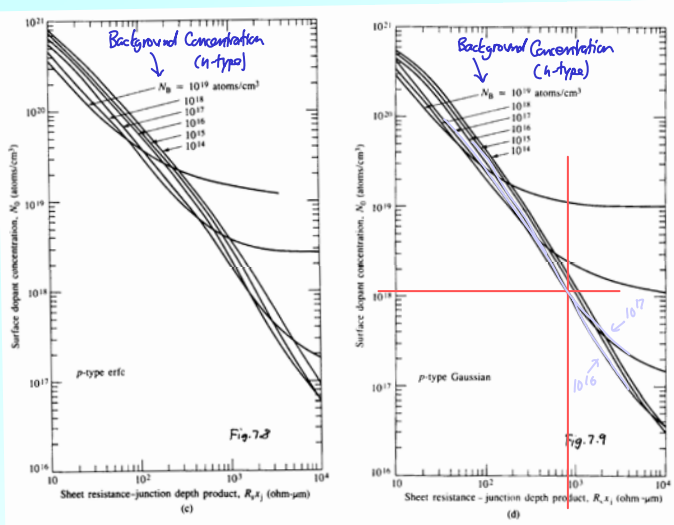
Determine the R_s.

Using Fig. 7.7:

$R_s x_j = 470\ \Omega\cdot\mu m$

$\therefore R_s = \frac{470}{2.77} = 170\ \Omega/\square$

Irvin's Curves (for p-type diffusion)



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(p-type Gaussian)

$x_j = 2.77$ μm

Can determine these given known predep. and drive conditions

Determine the R_s.

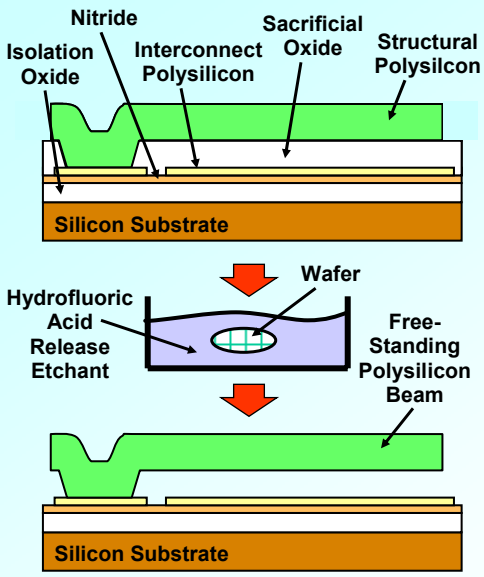
Using Fig. 7.9:

$R_s x_j = 800\,\Omega\cdot cm$

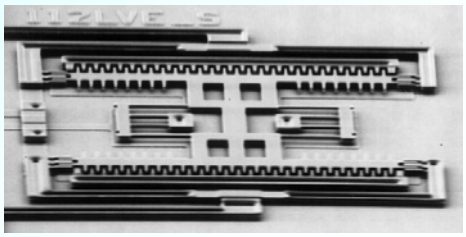
$\therefore R_s = \frac{800}{2.77} = 289\,\Omega/\square$

Surface Micromachining

Polysilicon Surface-Micromachining



- Uses IC fabrication instrumentation exclusively
- *Variations*: sacrificial layer thickness, fine- vs. large-grained polysilicon, *in situ* vs. $POCL_3$-doping



300 kHz Folded-Beam Micromechanical Resonator

Polysilicon

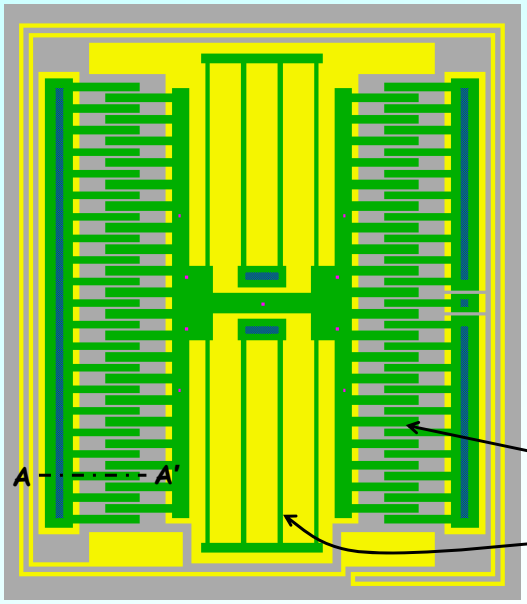
Why Polysilicon?

- Compatible with IC fabrication processes
  - Process parameters for gate polysilicon well known
  - Only slight alterations needed to control stress for MEMS applications
- Stronger than stainless steel: fracture strength of polySi ~ 2-3 GPa, steel ~ 0.2GPa-1GPa
- Young's Modulus ~ 140-190 GPa
- Extremely flexible: maximum strain before fracture ~ 0.5%
- Does not fatigue readily

- Several variations of polysilicon used for MEMS
  - LPCVD polysilicon deposited undoped, then doped via ion implantation, PSG source, $POCl_3$, or B-source doping
  - In situ-doped LPCVD polysilicon
  - Attempts made to use PECVD silicon, but quality not very good (yet) → etches too fast in HF, so release is difficult

Polysilicon Surface-Micromachining Process Flow

Layout and Masking Layers



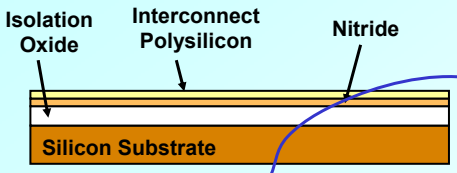
- At Left: Layout for a folded-beam capacitive comb-driven micromechanical resonator
- Masking Layers:
  - 1st Polysilicon
  - Anchor Opening
  - 2nd Polysilicon

Capacitive comb-drive for linear actuation

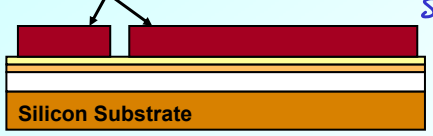
Folded-beam support structure for stress relief

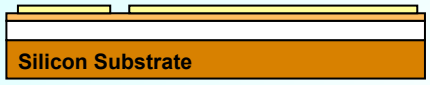
Surface-Micromachining Process Flow

Cross-sections through A-A'



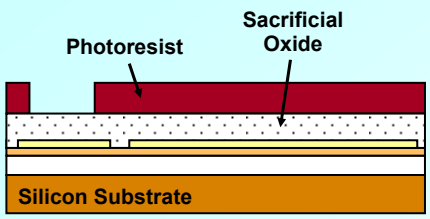
can go thicker w/ low stress nitride (Si rich) Si_xN_y



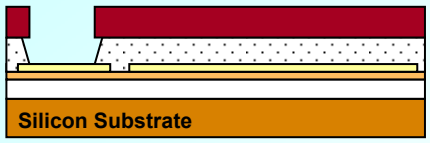


- Deposit isolation LTO (or PSG):
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the LTO (or PSG)
  - Anneal @950°C for 30 min.
- Deposit nitride: → Si_3N_4
  - Target = 100nm ← stay @ < 200 nm, otherwise stress problems
  - 22 min. LPCVD @800°C
- Deposit interconnect polySi:
  - Target = 300nm
  - In-situ Phosphorous-doped
  - 1 hr. 30 min. LPCVD @650°C
- Lithography to define poly1 interconnects
- RIE polysilicon interconnects:
  - $CCl_4/He/O_2$ @300W, 280mTorr
- Remove photoresist in PRS2000

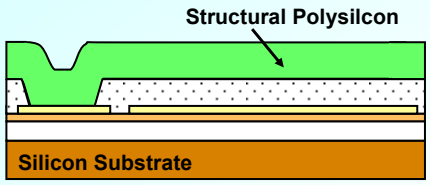
Surface-Micromachining Process Flow



- Deposit sacrificial PSG:
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the PSG
  - Anneal @950°C for 30 min.
- Lithography to define anchors

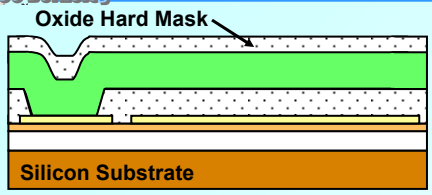


- Etch anchors
  - RIE using $CHF_3/CF_4/He$ @350W,2.8Torr
  - Remove PR in PRS2000
  - Quick wet dip in 10:1 HF to remove native oxide



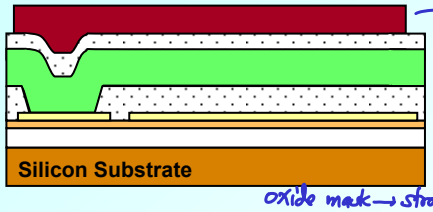
- Deposit structural polySi
  - Target = 2μm
  - In-situ Phosphorous-doped
  - 11 hrs. LPCVD @650°C

Surface-Micromachining Process Flow



- Deposit oxide hard mask (PSG)
  - Target = 500nm
  - 25 min. LPCVD @450°C
- Stress Anneal
  - 1 hr. @ 1050°C
  - Or RTA for 1 min. @ 1100°C in 50 sccm N_2

PR poly Si Etch poly Si



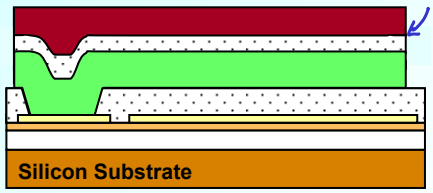
- Lithography to define poly2 structure (e.g., shuttle, springs, drive & sense electrodes)
  - Hard bake the PR longer to make it stronger

$S_{poly/PR} = 4:1$

- Etch oxide mask first
  - RIE using $CHF_3/CF_4/He$ @350W,2.8Torr

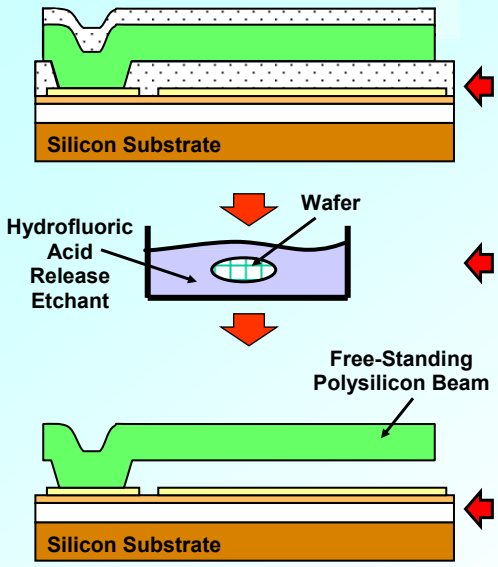
$S_{poly/ox} = 20:1$

oxide mask → straight sidewalls



- Etch structural polysilicon
  - RIE using $CCl_4/He/O_2$ @300W,280mTorr
  - Use 1 min. etch/1 min. rest increments to prevent excessive temperature

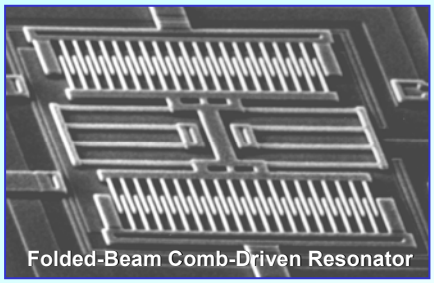
Surface-Micromachining Process Flow

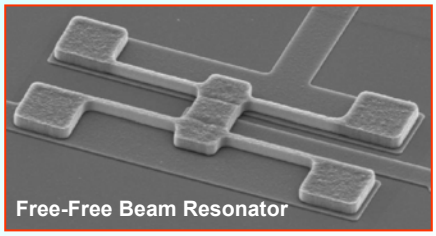


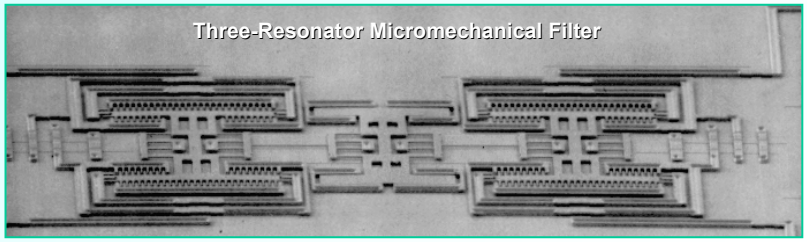
- Remove PR (more difficult)
  - Ash in O_2 plasma
  - Soak in PRS2000
- Release the structures
  - Wet etch in HF for a calculated time that insures complete undercutting
  - If 5:1 BHF, then ~ 30 min.
  - If 48.8 wt. % HF, ~ 1 min.
- Keep structures submerged in DI water after the etch
- Transfer structures to methanol
- Supercritical CO_2 dry release

Polysilicon Surface-Micromachined Examples

- Below: All surface-micromachined in polysilicon using variants of the described process flow


Folded-Beam Comb-Driven Resonator


Free-Free Beam Resonator


Three-Resonator Micromechanical Filter

Structural/Sacrifical Material Combinations

Structural Material	Sacrificial Material	Etchant
Poly-Si	SiO_2, PSG, LTO	HF, BHF
Al	Photoresist	O_2 plasma
SiO_2	Poly-Si	XeF_2
Al	Si	TMAH, XeF_2
Poly-SiGe	Poly-Ge	H_2O_2, hot H_2O

- Must consider other layers, too, as release etchants generally have a finite E.R. on any material
- Ex: concentrated HF (48.8 wt. %)
  - Polysilicon E.R. ~ 0
  - Silicon nitride E.R. ~ 1-14 nm/min
  - Wet thermal SiO_2 ~ 1.8-2.3 μm/min
  - Annealed PSG ~ 3.6 μm/min
  - Aluminum (Si rich) ~ 4 nm/min (much faster in other Al)

Wet Etch Rates (f/ K. Williams)

Wet-Etch Rates for Micromachining and IC Processing (Å/min)

The top etch rate was measured by the authors with fresh solutions, etc. The center and bottom values are the low and high etch rates observed by the authors and others in our lab under less carefully controlled conditions.

ETCHANT EQUIPMENT CONDITIONS	TARGET MATERIAL	MATERIAL SC Si <100>	Poly n+	Poly undop	Wet Ox	Dry Ox	LTO undop	PSG unanl	PSG annld	Stoic Nitrid	Low-σ Nitrid	Al/ 2% Si	Sput Tung	Sput Ti	Sput Ti/W	OCG 820PR	Olin HntPR
Concentrated HF (49%) Wet Sink Room Temperature	Silicon oxides	-	0	-	23k 18k 23k	F	>14k	F	36k	140	52 30 52	42 0 42	<50	F	-	P 0	P 0
10:1 HF Wet Sink Room Temperature	Silicon oxides	-	7	0	230	230	340	15k	4700	11	3	2500 2500 12k	0	11k	<70	0	0
25:1 HF Wet Sink Room Temperature	Silicon oxides	-	0	0	97	95	150	W	1500	6	1	W	0	-	-	0	0
5:1 BHF Wet Sink Room Temperature	Silicon oxides	-	9	2	1000 900 1080	1000	1200	6800	4400 3500 4400	9	4 3 4	1400	<20 0.25 20	F	1000	0	0
Phosphoric Acid (85%) Heated Bath with Reflux 160°C	Silicon nitrides	-	7	-	0.7	0.8	<1	37	24 9 24	28 28 42	19 19 42	9800	-	-	-	550	390
Silicon Etchant (126 HNO_3 : 60 H_2O : 5 NH_4F) Wet Sink Room Temperature	Silicon	1500	3100 1200 6000	1000	87	W	110	4000	1700	2	3	4000	130	3000	-	0	0
KOH (1 KOH : 2 H_2O by weight) Heated Stirred Bath 80°C	<100> Silicon	14k	>10k	F	77 41 77	-	94	W	380	0	0	F	0	-	-	F	F
Aluminum Etchant Type A (16 H_3PO_4 : 1 HNO_3 : 1 HAc : 2 H_2O) Heated Bath 50°C	Aluminum	-	<10	<9	0	0	0	-	<10	0	2	6600 2600 6600	-	0	-	0	0
Titanium Etchant (20 H_2O : 1 H_2O_2 : 1 HF) Wet Sink Room Temperature	Titanium	-	12	-	120	W	W	W	2100	8	4	W	0 0 <10	8800	-	0	0
H_2O_2 (30%) Wet Sink Room Temperature	Tungsten	-	0	0	0	0	0	0	0	0	0	<20	190 190 1000	0	60 60 150	<2	0
Piranha (~50 H_2SO_4 : 1 H_2O_2) Heated Bath 120°C	Cleaning off metals and organics	-	0	0	0	0	0	-	0	0	0	1800	-	2400	-	F	F
Acetone Wet Sink Room Temperature	Photoresist	-	0	0	0	0	0	-	0	0	0	0	-	0	-	>44k	>39k

Notation: - =test not performed; W=not performed, but known to Work (≥ 100 Å/min); F=not performed, but known to be *Fast* (≥ 10 kÅ/min); P=some of film *Peeled* during etch or when rinsed; A=film was visibly *Attacked* and roughened.
Etch areas are all of a 4-inch wafer for the transparent films and half of the wafer for single-crystal silicon and the metals.
Etch rates will vary with temperature and prior use of solution, area of exposure of film, other materials present (e.g., photoresist), film impurities and microstructure, etc. *Some variation should be expected.*

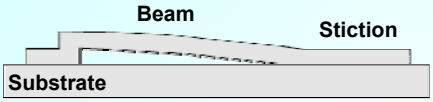
Film Etch Chemistries

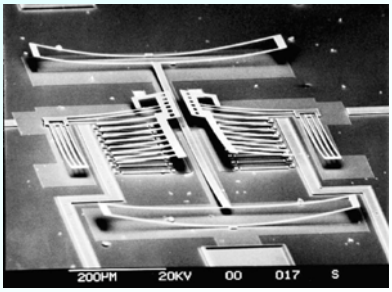
- For some popular films:

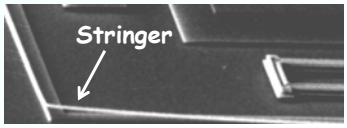
Material	Wet etchant	Etch rate [nm/min]	Dry etchant	Etch rate [nm/min]
Polysilicon	HNO_3:H_2O: NH_4F	120-600	SF_6 + He	170-920
Silicon nitride	H_3PO_4	5	SF_6	150-250
Silicon dioxide	HF	20-2000	CHF_3 + O_2	50-150
Aluminum	H_3PO_4:HNO_3: CH_3COOH	660	Cl_2 + $SiCl_4$	100-150
Photoresist	Acetone	>4000	O_2	35-3500
Gold	KI	40	n/a	n/a

Issues in Surface Micromachining

- Stiction: sticking of released devices to the substrate or to other on-chip structures
  - Difficult to tell if a structure is stuck to substrate by just looking through a microscope
- Residual Stress in Thin Films
  - Causes bending or warping of microstructures
  - Limits the sizes (and sometimes geometries) of structures
- Topography
  - Stringers can limit the number of structural levels







Microstructure Stiction

Microstructure Stiction

- Stiction: the unintended sticking of MEMS surfaces
- Release stiction:
  - Occurs during drying after a wet release etch
  - Capillary forces of droplets pull surfaces into contact
  - Very strong sticking forces, e.g., like two microscope slides w/ a droplet between
- In-use stiction: when device surfaces adhere during use due to:
  - Capillary condensation
  - Electrostatic forces
  - Hydrogen bonding
  - Van der Waals forces