PROBLEM SET #2

Issued: Tuesday, Sept. 13, 2011

Due (at 7 p.m.): Tuesday, Sept. 27, 2011, in the EE C245 HW box in 240 Cory.

1. Below in Figure 1.1 is a description of a DRIE silicon etch using the Marvell Nanolab's Centura Deep Silicon Etch DPS-DT, taken from that tool's lab manual:

DPS200- Oct 2008			
	STEP 1	STEP 2	STEP 3
STEP NAME	ST	PASS	ETCH
PURPOSE	stabilization	passivation	etch
C4F8	225sccm	225sccm	-
SF6	-	-	300sccm
O2	-	-	-
PRESSURE	40mT	40mT	60mT
BIAS	0W	0W	6W
PW	-	-	OFF
CW	-	-	ON
SOURCE	0W	1200W	1200W
TIME	10 sec	5 sec	7 sec
REPEAT	repeat step 2 to 3		
TYPICAL RESULTS			
ETCH RATE, micron/min:			6.30
% NON-UNIFORMITY (6in diam):			8%
% NON-UNIFORMITY (4in diam):			3%
PROFILE:			90deg +/- 0.5deg
SELECTIVITY, Si:Gline uvbake			125:1
% ARDE, 4 vs 20 micron differential			8.50%

Figure 1.1

Your goal is to etch a trench 10μm wide by 100μm long by 300μm deep into a 600μm silicon substrate.

(a) Draw a cross-section along the 10μm width of the trench immediately before the first etch step starts, showing the amount of photoresist needed for the masking layer and the etch opening created by lithography through the photoresist.

(b) Draw a cross section immediately after the first Step 3 etch. Assume the following:

i. The passivation layer in the mask opening (or directly below the mask opening) is immediately obliterated by ion bombardment at the beginning of each Step 3 Etch.

ii. The etch rate of Si NOT directly below the mask opening (not exposed to ion bombardment) is 1/100 the stated vertical etch rate and is isotropic.

iii. The etch rate of the passivation layer NOT directly below the mask opening is such that the passivation layer from the previous Step 2 is EXACTLY removed at the end

each Step 3 – i.e., the passivation layer from Step 2 remains on the sidewalls until the end of the Step 3, at which point it is completely removed.

(c) Draw a cross section after 1 minute of etching, clearly showing the dimensions of the "scallops" caused by the DRIE process. Same assumptions as in part b.

2. This problem explores the logistics of using backside wafer etches to create diaphragms used for example in pressure sensors. To start, you are given a (100) wafer with the vertical cross section shown in Figure 2.1 (not shown to scale).

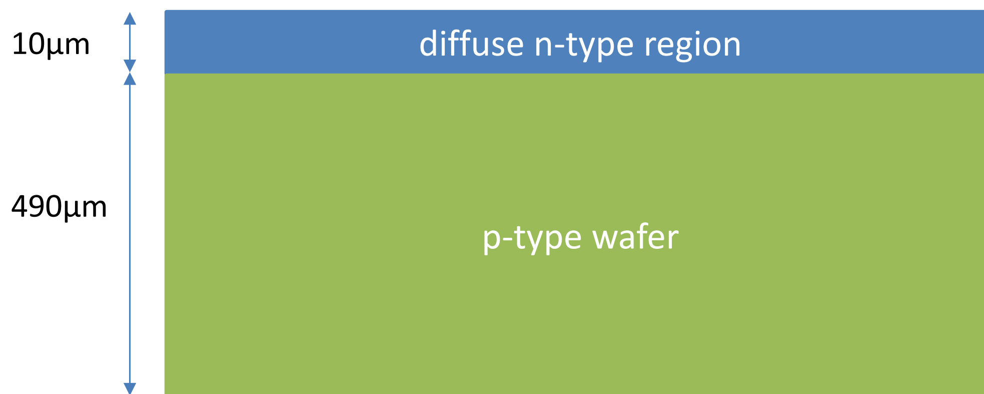

Figure 2.1

After spinning a layer of photoresist on the back-side of the wafer, you use photolithography to open up a square opening perfectly oriented to the <110> plane of the silicon wafer, such that the side of the square is exactly parallel to the <110> direction. You then perform a KOH anisotropic etch using the diffuse n-type region of the wafer as an electrochemical etch stop to achieve the cross section in Figure 2.2 (dimensions not to scale):

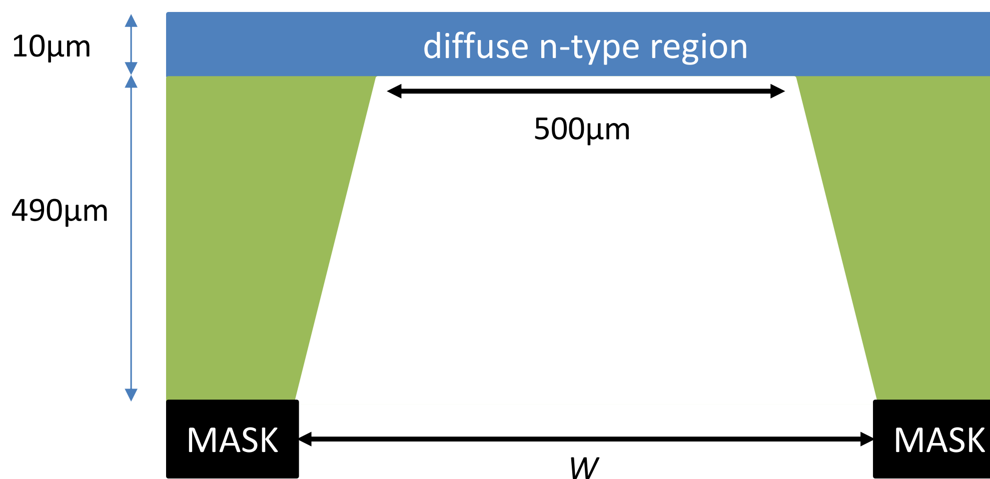

Figure 2.2

(a) Referring to Figure 2.2, find the necessary side width *W* for the square the mask opening to ensure that the final diaphragm is a 500μm × 500μm square? Assume the mask opening is perfectly aligned to the <110> planes of the wafer, as shown in the view of the backside of the wafer in Figure 2.3, and ignore etching of the <111> planes. (*Hint: Senturia section 3.3.4.2.)*

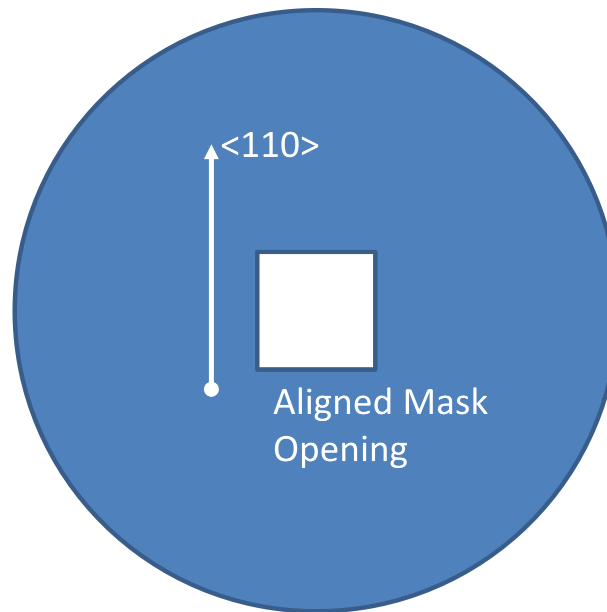

Figure 2.3

(b) Provide an equation that gives the diaphragm size as a function of wafer thickness. If the thickness of the wafer varies by ±1%, what is the corresponding variation in the size of the diaphragm?

(c) Provide an equation that gives the diaphragm size as a function of mask misalignment to the <110> plane in degrees. If the mask is misaligned to the <110> plane by 10°, what is the new size of the diaphragm?

3. Begin with two silicon wafers: the first has a uniform gallium concentration of 1×10^{15} cm^{-3} and the second has a uniform phosphorous concentration of 1×10^{15} cm^{-3}. Both wafers are then uniformly doped with a boron concentration of 2×10^{15} cm^{-3} without disturbing the original dopant profile. Note that, at this point, both wafers are net P-type. Next, the wafers are thermally oxidized in a dry environment to grow 0.2 µm of SiO_2 on the surface. The oxides of both wafers are then stripped and measurements are made to determine the doping type on the wafer surfaces.

(a) For the case of the phosphorus-doped wafer, is the resulting wafer surface N-type or P-type? Why? Draw a graph showing the approximate concentrations of each dopant as a function of distance from the wafer surface. If there is a junction, determine the junction depth. Use the charts provided in Figure 3.1. (*Hint: More info may be found in Jaeger, Chapter 3.4-3.5)*

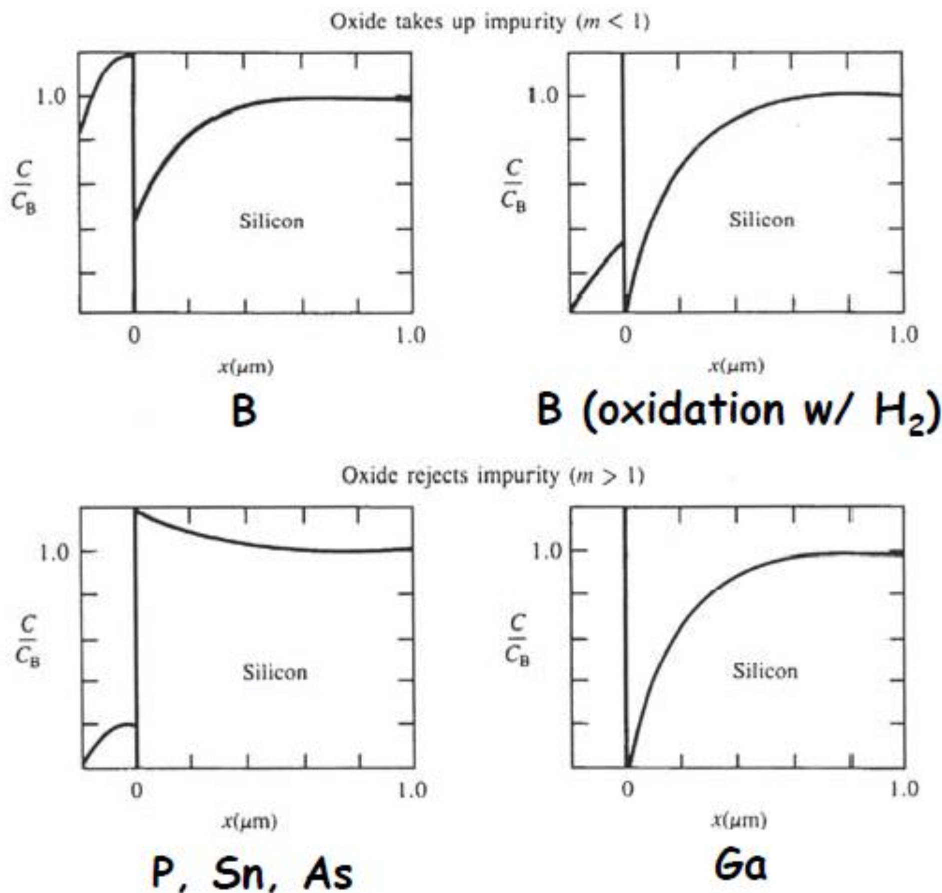

Figure 3.1 (Jaeger)

(b) For the case of the gallium-doped wafer, is the resulting wafer surface N-type or P-type? Why? Draw a graph showing the approximate concentrations of each dopant as a function of distance from the wafer surface. If there is a junction, determine the junction depth.

4. You are given a wafer with the cross section shown in Figure 4.1. Your goal is to perform a "release" etch leaving only the poly-silicon structure on top of the nitrite/oxide layer, along with the Tungsten ground contact. You have access to Etchant X and Etchant Y with the characteristics in Table 4.1:

	Vertical/Horizontal Etch Rates (µm/min)				
	PSG	**Poly-silicon**	**SiO_2**	**Nitride**	**W**
Etchant X	1/0.1	0.1/0.05	1/0.1	0.01/0.005	0.01/0.005
Etchant Y	0.1/0.1	0.01/0.01	1/1	0.1/0.1	0.01/0.01

Table 4.1

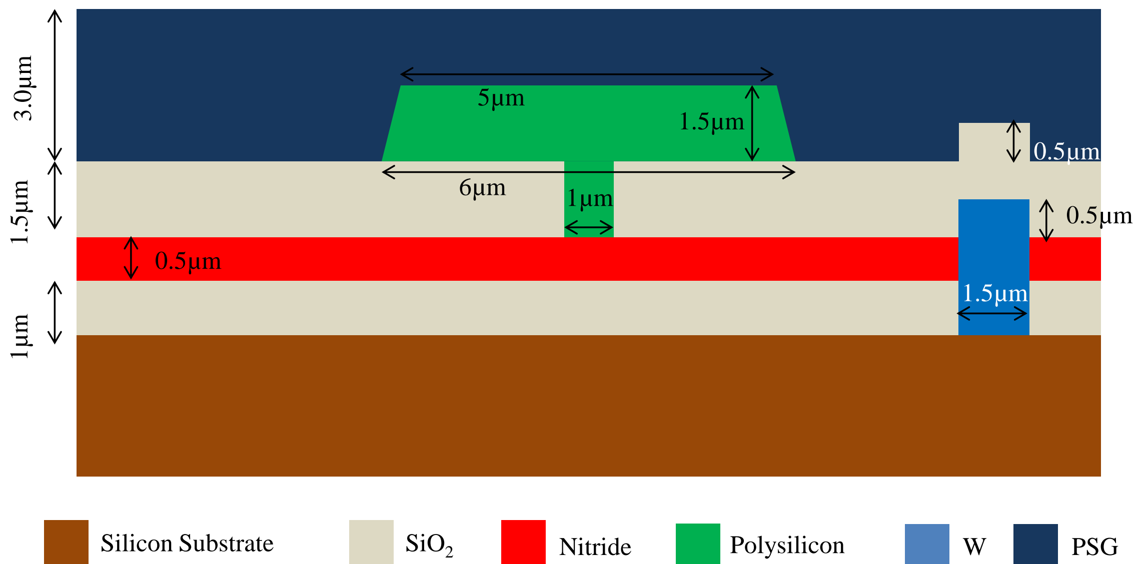

Figure 4.1

(a) The first step of the release is to use Etchant X for 3 minutes. Draw the new cross section after this release step, specifying all dimensions.

(b) The second step of the release is to use Etchant Y until the structure is "released" – i.e. no SiO_2 remains between the Poly-silicon structure and the nitride layer. Draw the new cross section after this release step, specifying all dimensions, and calculate the time required to complete this release step.