EE247
Lecture 20

ADC Converters

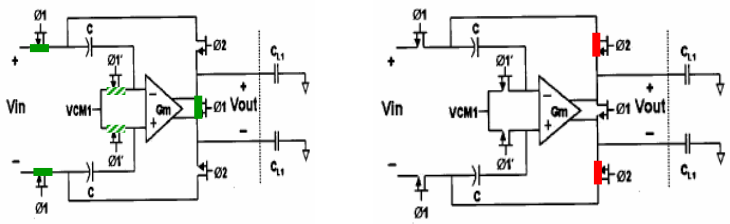
- Sampling (continued)
  - Track & hold circuits
  - T/H combined with summing/difference function
  - T/H circuit incorporating gain & offset cancellation
- Electro-Static Discharge (ESD) protection
- ADC architectures (today)
  - Serial- slope type
  - Successive approximation
  - Flash

Summary Last Lecture

ADC Converters

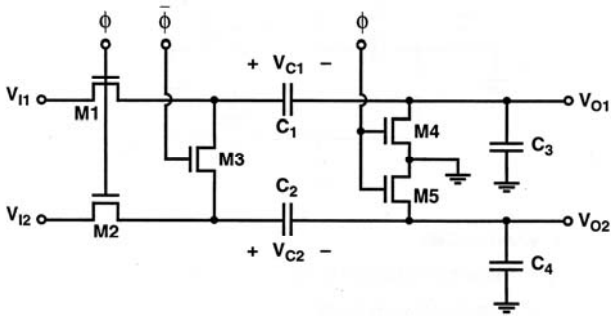
- Sampling (continued)
  - Clock boosters (continued)
  - Sampling switch charge injection & clock feedthrough
    - Complementary switch
    - Use of dummy device
    - Bottom-plate switching
  - Track & hold circuits

Differential Flip-Around T/H
Issues: Input Common-Mode Range



- $\Delta V_{in\text{-}cm} = V_{out_com} - V_{sig_com}$
  → Amplifier needs to have large input common-mode compliance

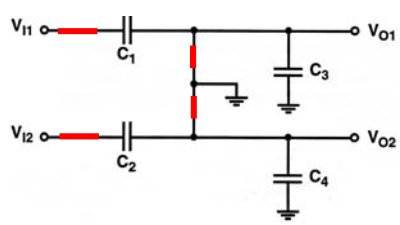
Input Common-Mode Cancellation

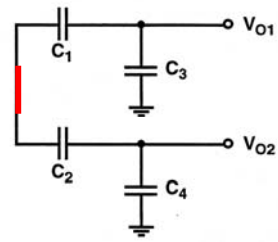


- Note: Shorting switch M3 added

Ref: R. Yen, *et al.* "A MOS Switched-Capacitor Instrumentation Amplifier," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-17, NO. 6,, DECEMBER 1982 1008

Input Common-Mode Cancellation



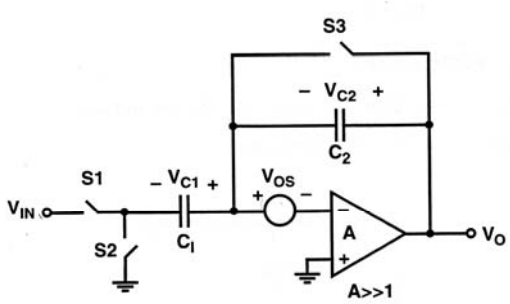


Track mode (ϕ high)
$V_{C1}=V_{I1}$, $V_{C2}=V_{I2}$
$V_{o1}=V_{o2}=0$

Hold mode (ϕ low)
$V_{o1}+V_{o2}=0$
$V_{o1}-V_{o2}= -(V_{I1}-V_{I2})(C_1/(C_1+C_3))$

→ Input common-mode level removed

T/H + Charge Redistribution Amplifier



Track mode: (S1, S3 →on S2→ off)

$V_{C1}=V_{os}-V_{IN}$, $V_{C2}=0$

$V_o=V_{os}$

T/H + Charge Redistribution Amplifier Hold Mode

$V_{C1} \longrightarrow V_{os}$

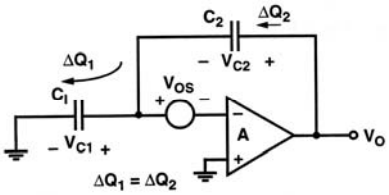
$\Delta V_{C1} = V_{os} - (V_{os} - V_{IN}) = V_{IN}$

$\Delta Q_1 = C_1 \Delta V_{C1} = C_1 V_{IN}$

$\Delta Q_2 = C_2 \Delta V_{C2} = \Delta Q_1$

$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right) V_{C1} = V_{C2}$

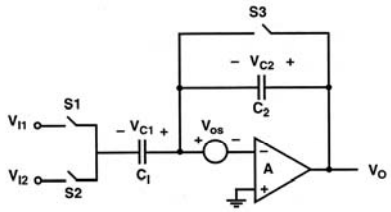
$V_O = V_{C2} + V_{os} = \left(\frac{C_1}{C_2}\right) V_{IN} + V_{os}$

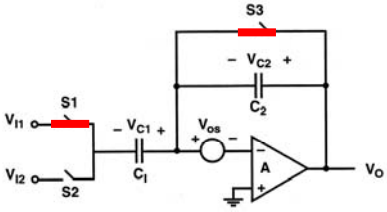


Hold/amplify mode (S1, S3 → off S2 → on)

→ Offset NOT cancelled, but not amplified
→ Input-referred offset $=(C_2/C_1) \times V_{OS}$, & often $C_2<C_1$

T/H & Input Difference Amplifier

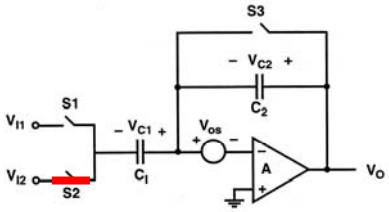




Sample mode (S1, S3 → on S2 → off)
$V_{C1}=V_{os} - V_{I1}$, $V_{C2}=0$
$V_o=V_{os}$

Input Difference Amplifier Cont'd

Subtract/Amplify mode (S1, S3 →off S2→ on)
During previous phase:
$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=0$
$V_o=V_{os}$



$$V_{C1} = V_{os} - V_{I2}$$

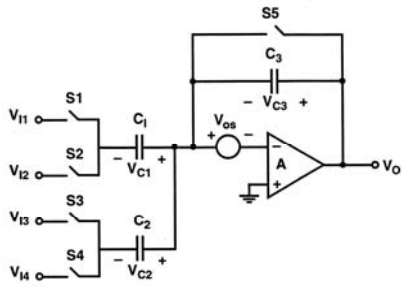
$$\Delta V_{C1} = (V_{os} - V_{I2}) - (V_{os} - V_{I1}) = V_{I1} - V_{I2}$$

$$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right)\Delta V_{C1} = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2})$$

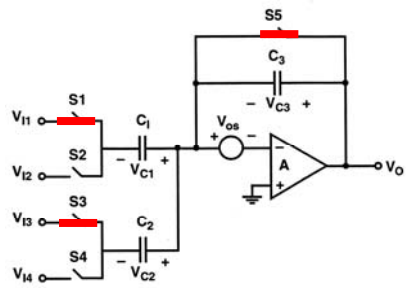
$$V_O = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2}) + V_{os}$$

→Offset NOT cancelled, but not amplified
→Input-referred offset $=(C_2/C_1)xV_{OS}$, & $C_2<C_1$

T/H & Summing Amplifier



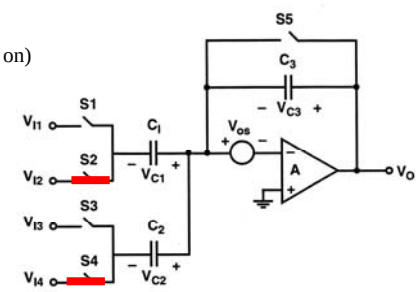
T/H & Summing Amplifier Cont'd



Sample mode (S1, S3, S5→on S2, S4→ off)
$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=V_{os}-V_{I3}$, $V_{C3}=0$
$V_o=V_{os}$

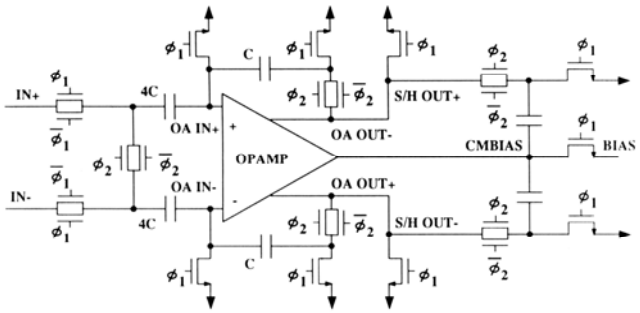
T/H & Summing Amplifier Cont'd

Amplify mode (S1, S3, S5→off, S2, S4→ on)



$$V_{C1}=V_{os}-V_{I2} \Rightarrow \Delta V_{C1}=V_{I1}-V_{I2}$$
$$V_{C2}=V_{os}-V_{I4} \Rightarrow \Delta V_{C2}=V_{I3}-V_{I4}$$
$$\Delta Q_3=\Delta Q_1+\Delta Q_2=C_1\Delta V_{C1}+C_2\Delta V_{C2}$$
$$\Delta V_{C3}=\frac{\Delta Q_3}{C_3}=\left(\frac{C_1}{C_3}\right)(V_{I1}-V_{I2})+\left(\frac{C_2}{C_3}\right)(V_{I3}-V_{I4})$$
$$V_O=\left(\frac{C_1}{C_3}\right)(V_{I1}-V_{I2})+\left(\frac{C_2}{C_3}\right)(V_{I3}-V_{I4})+V_{os}$$

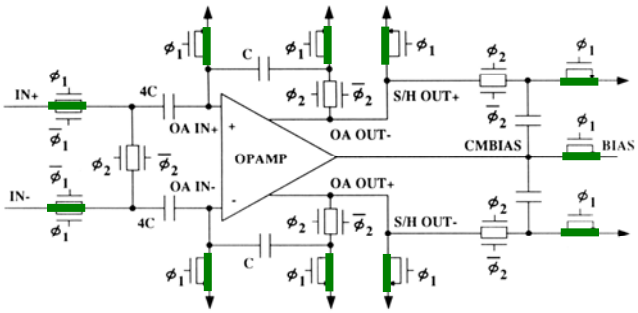
Differential T/H Combined with Gain Stage



Employs the previously discussed technique to eliminate the problem associated with high common-mode voltage excursion at the input of the opamp

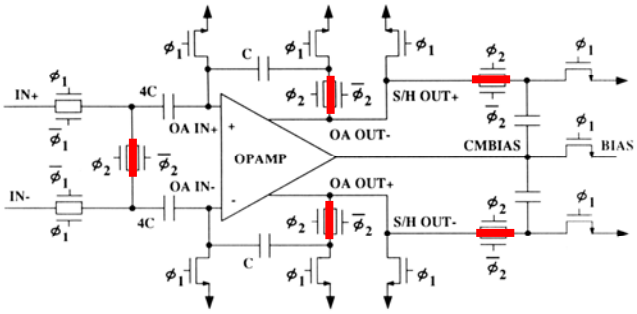
Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

Differential T/H Combined with Gain Stage
$\phi 1 \rightarrow$ High



Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

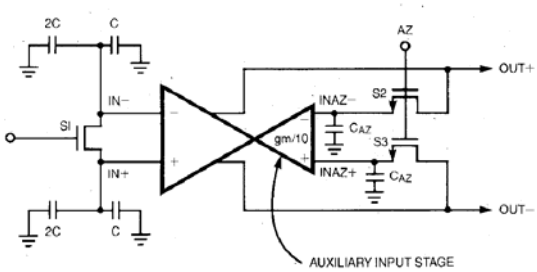
Differential T/H Combined with Gain Stage



- *Gain=4C/C=4*
- *Input voltage common-mode level removed → opamp can have low input common-mode compliance*
- *Amplifier offset NOT removed*

Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

Differential T/H Including Offset Cancellation

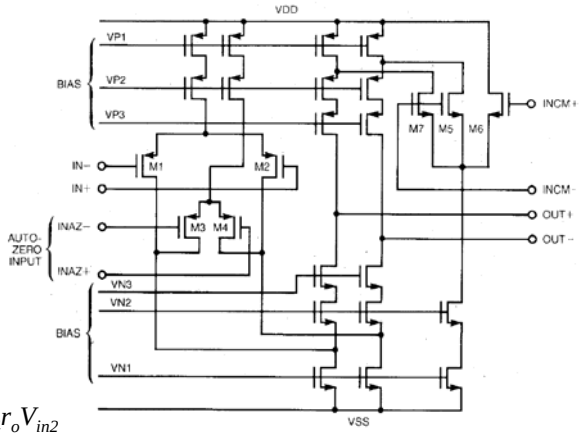


- Operation during offset cancellation phase shown
- Auxilary inputs added with A_{main}/A_{aux}.=10
- During offset cancellation phase:
  - Aux. amp configured in unity-gain mode: $V_{out}=V_{os}^{main}$ → offset stored on C_{AZ} & canceled

Ref: H. Ohara, et al., "A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE Journal of Solid-State Circuits,* vol. 22, pp. 930 - 938, December 1987.

Differential T/H Including Offset Cancellation Operational Amplifier

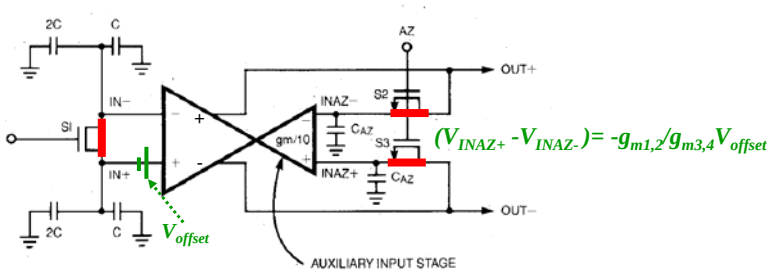
- Operational amplifier → dual input folded-cascode opamp
- M3,4 auxiliary input, M1,2 main input
- To achieve 1/10 gain ratio $W_{M3,4} = 1/10x\ W_{M1,2}$ & current sources are scaled by 1/10
- M5,6,7 → common-mode control
- Output stage → dual cascode → high DC gain



$$V_{out} = g_{m1,2} r_o V_{in1} + g_{m3,4} r_o V_{in2}$$

Ref: H. Ohara, et al., "A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE Journal of Solid-State Circuits,* vol. 22, pp. 930 - 938, December 1987.

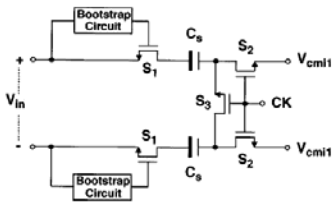
Differential T/H Including Offset Cancellation Phase

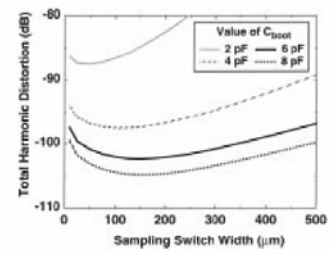


$$(V_{INAZ+} - V_{INAZ-}) = -g_{m1,2}/g_{m3,4} V_{offset}$$

- During offset cancellation phase AZ and S1 closed → main amplifier offset amplified by g_{m1}/g_{m2} & stored on C_{AZ}
- Auxiliary amp chosen to have lower gain so that:
  - ❑ Aux. amp charge injection associated with opening of switch AZ → reduced by $A_{aux}/A_{main} = 1/10$
  - ❑ Insignificant increase in power dissipation resulting from addition of aux. inputs
- Requires an extra auto-zero clock phase

Differential Flip-Around T/H
Choice of Sampling Switch Size

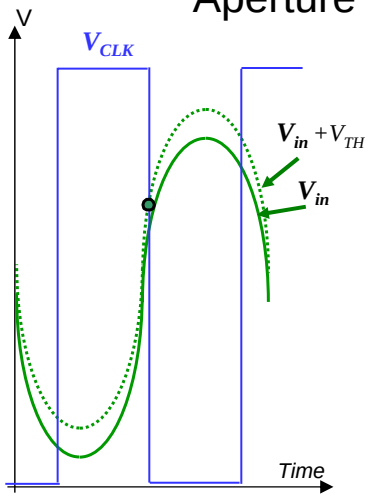


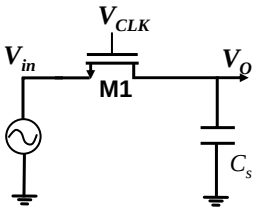


- THD simulated w/o sampling switch boosted clock → -45dB
- THD simulated with sampling switch boosted clock (see figure)

Ref: K. Vleugels et al, "A 2.5-V Sigma–Delta Modulator for Broadband Communications Applications " IEEE JSSC, VOL. 36, NO. 12, DECEMBER 2001, pp. 1887

Track & Hold
Aperture Time Error

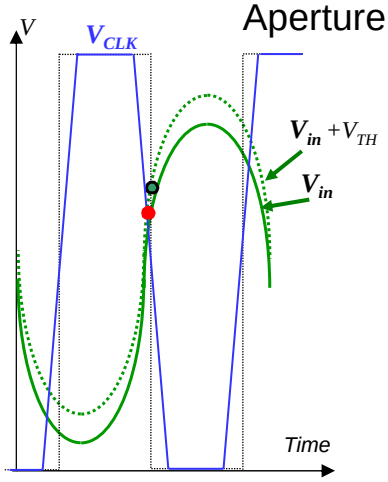




Transition from track to hold:
Occurs when device turns fully off
→ $V_{CLK}=V_{in}+V_{TH}$

Sharp fall-time wrt signal change
→ no aperture error

Track & Hold
Aperture Time Error



Slow clock → aperture error

$V_{in} = A \sin(2\pi f_{in} t)$

$\varepsilon = f_{in} x A x \ t_{fall} / V_{CLK}$

$SDR = -20 \log \varepsilon - 4$ [dB] (see Ref.)

Example: Nyquist rate *10-bit ADC* & $A = V_{CLK}/4$

→ *SQNR=62dB*

for SDR due to aperture error < quant error

→ $t_{fall} < 2x10^{-3}/f_{in}$

→ *Worst case:* $f_{in} = f_s/2$

→ $t_{fall} < 4x10^{-3}/f_s$

→ *e.g.* $f_s = 100MHz$ $t_{fall} < 40psec$

Ref: P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitance," *IEEE Journal of Solid-State Circuits,* vol. 26, pp. 643 - 651, April 1991.

Track & Hold
Aperture Time Error

- Aperture error analysis applies to simple sampling network
- Bottom plate sampling → minimizes aperture error
- Boosted clock → reduces aperture error
- In general: Clock fall/rise trade-off between switch charge injection versus aperture error

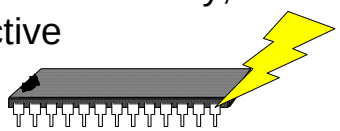
Ref: P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitance," *IEEE Journal of Solid-State Circuits,* vol. 26, pp. 643 - 651, April 1991.

ESD Protection

ADC Architectures

What is ESD?

- Electrostatic discharge
- Example: Charge built up on human body while walking on carpet...
- Charged objects near or touching IC pins can discharge through on-chip devices
- Without dedicated protection circuitry, ESD events could be destructive



Model and Protection Circuit

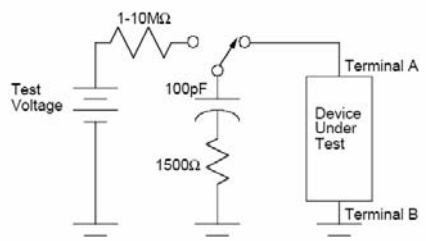
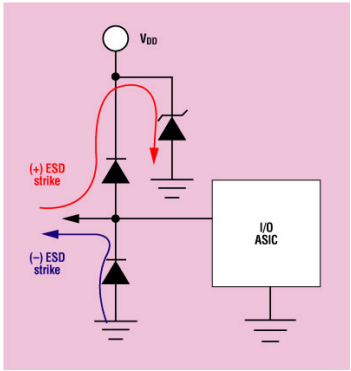


Figure 1. Human Body Model for ESD testing.

[http://www.idt.com/docs/AN_123.pdf]



[http://www.ce-mag.com/archive/03/ARG/dunnihoo.html]

Equivalent Circuit

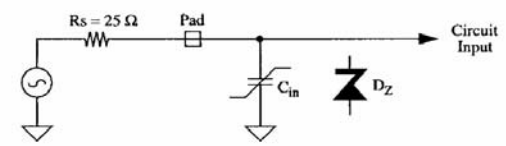


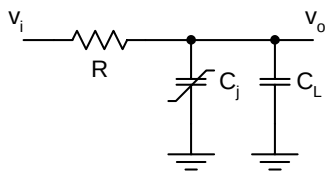
Fig. 1. Equivalent input circuit.

- Nonlinear capacitance causes distortion
- Distortion increases with frequency
  - Today's converters: High frequency, low distortion!

Ref: I. E. Opris, "Bootstrapped pad protection structure," IEEE J.Solid-State Circuits, pp. 300, Feb. 1998

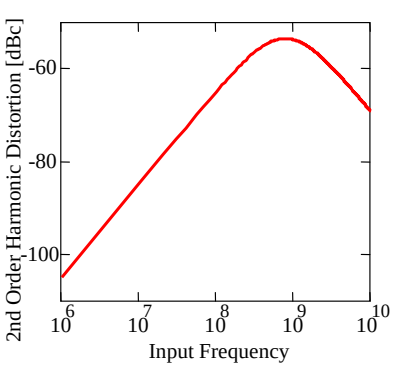
ESD Circuit Distortion

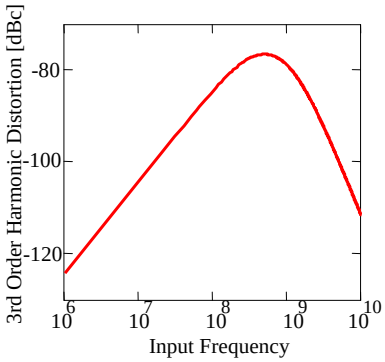
- Analysis:
  - Volterra Series
  - Or SPICE simulations
- Example:



$R=25\Omega$
$C_{jo}=1pF$
$C_L=5pF$
$V_{ipeak}=0.5V$

ESD Circuit Distortion





H_{D3}(@ 37.5MHz) = -92dB
H_{D3}(@ 100MHz) = -84dB

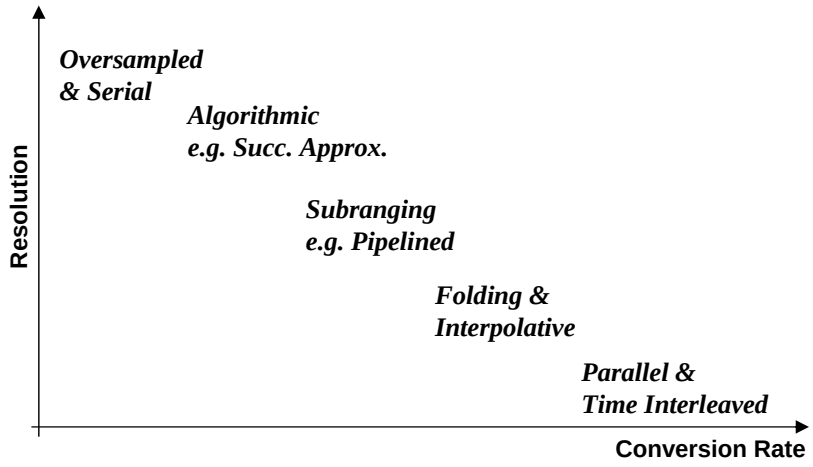
ESD Circuit Distortion

- Distortion from ESD circuits approaches state of-the-art ADC performance!
- If you are working on a new, record breaking ADC, better think about ESD now...
- Ref.: A. Wang, "Recent developments in ESD protection for RF IC," *Proc. DAC Conference*, Jan. 2003
- Solutions still pre-mature
- Lots of company intellectual property! (IP)

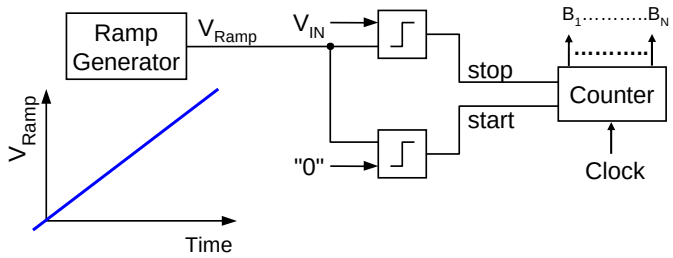
ADC Architectures

- Slope type converters
- Successive approximation
- Flash
- Time-interleaved / parallel converter
- Folding
- Residue type ADCs
  - Two-step
  - Pipeline
  - …
- Oversampled ADCs

Various ADC Architectures
Resolution/Conversion Rate



Serial ADC
Single Slope

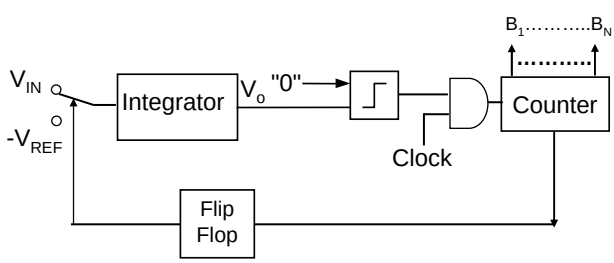


- Counter starts counting @ $V_{Ramp}=0$
- Counter stops counting for $V_{IN}=V_{Ramp}$
  → Counter output proportional to V_{IN}

Single Slope ADC

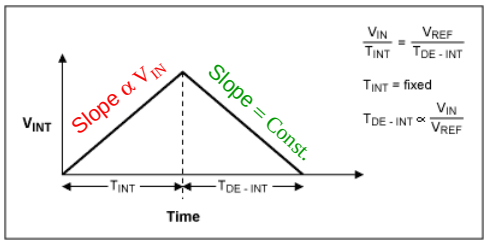
- Advantages:
  - Low complexity & simple
  - INL depends on ramp linearity & not component matching
  - Inherently monotonic
- Disadvantages:
  - Slow (2^N clock pulses for N-bit conversion)
  - Hard to generate precise ramp
  - Need to calibrate ramp slope versus V_{IN}
- Better: Dual Slope, Multi-Slope

Serial ADC Dual Slope



- First: V_{IN} is integrated for a fixed time ($2^N x T_{CLK}$)
  → $V_o = 2^N x T_{CLK}\ V_{IN}/\tau_{intg}$
- Next: V_o is de-integrated with V_{REF} until $V_o=0$
  → Counter output = $2^N\ V_{IN}/V_{REF}$

Dual Slope ADC



http://www.maxim-ic.com/appnotes.cfm/appnote_number/1041

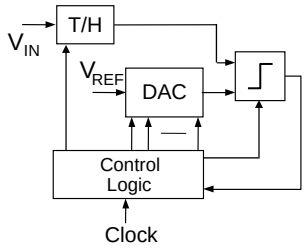
- Integrate V_{in} for fixed time (T_{INT}), de-integrate with V_{REF} applied → $T_{De\text{-}Int} \sim 2^{N} x T_{CLK} x V_{in}/V_{REF}$
- Most laboratory DVMs use this type of ADC

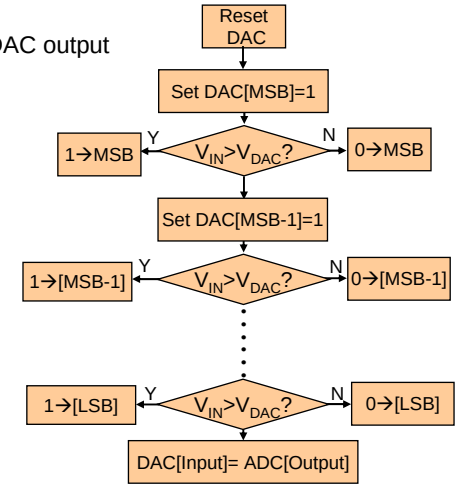
Dual Slope ADC

- Advantage:
  - Accuracy to 1st order independent of integrator time-constant and clock period
  - Comparator offset referred to input is attenuated by integrator high DC gain
  - Insensitive to most linear error sources
  - DNL is a function of clock jitter
  - Power supply (60Hz) xtalk effect on reading can be canceled by: choosing conversion time multiple of 1/60Hz
  - High accuracy achievable (16+bit)
- Disadvantage:
  - Slow (maximum $2x2^{N}xT_{clk}$ per conversion)
  - Integrator opamp offset results in ADC offset (can cancel)
  - Finite opamp gain gives rise to INL

Successive Approximation ADC
SAR

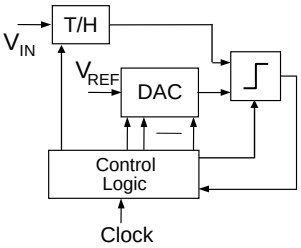
- Algorithmic type ADC
- Based on binary search over DAC output

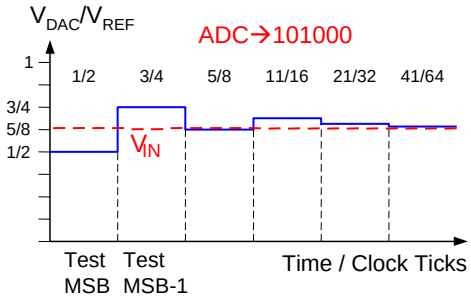




Successive Approximation ADC

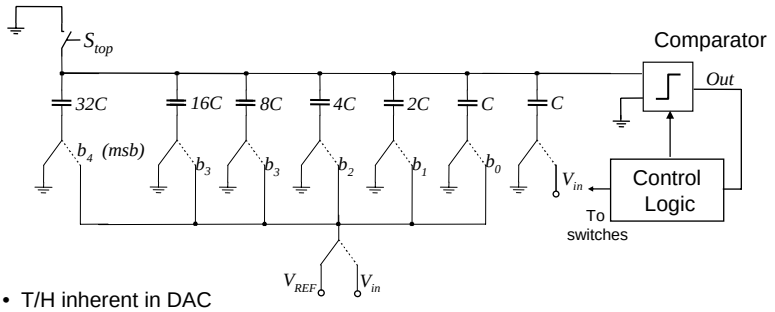
Example: 6-bit ADC & $V_{IN}=5/8V_{REF}$





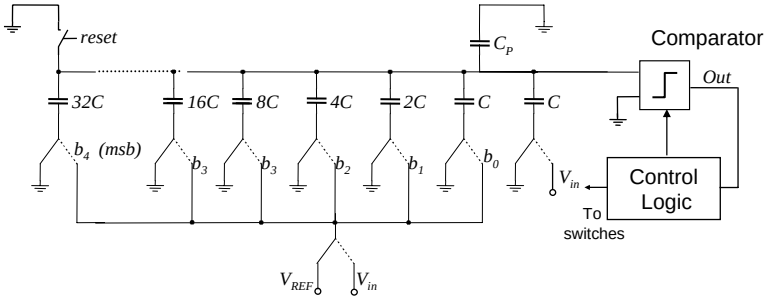
- High accuracy achievable (16+ Bits)
- Required N clock cycles for N-bit conversion (much faster than slope type)
- Moderate speed proportional to B (MHz range)

Example: SAR ADC
Charge Redistribution Type



- T/H inherent in DAC
- Operation starts by connecting all top plate to gnd and all bottom plates to Vin
- To test the MSB all top plate are opened bottom plate of 32C connected to V_{REF} & rest of bottom plates connected to ground → input to comparator= $-V_{in} + V_{REF}/2$
- Comparator is strobed to determine the polarity of input signal if - MSB=1 if + MSB=0
- The process continues until all bits are determined

Example: SAR ADC
Charge Redistribution Type

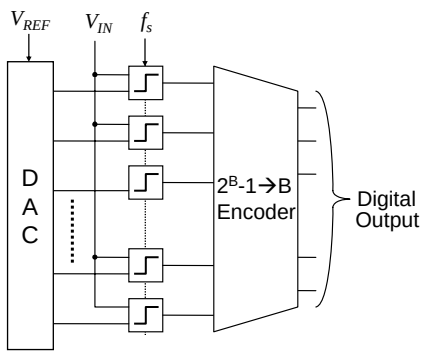


- To 1st order parasitic (C_p) insensitive since top plate driven from initial 0 to final 0 by the global negative feedback
- Linearity is a function of accuracy of C ratios
- Possible to add a C ratio calibration cycle (see ref.)

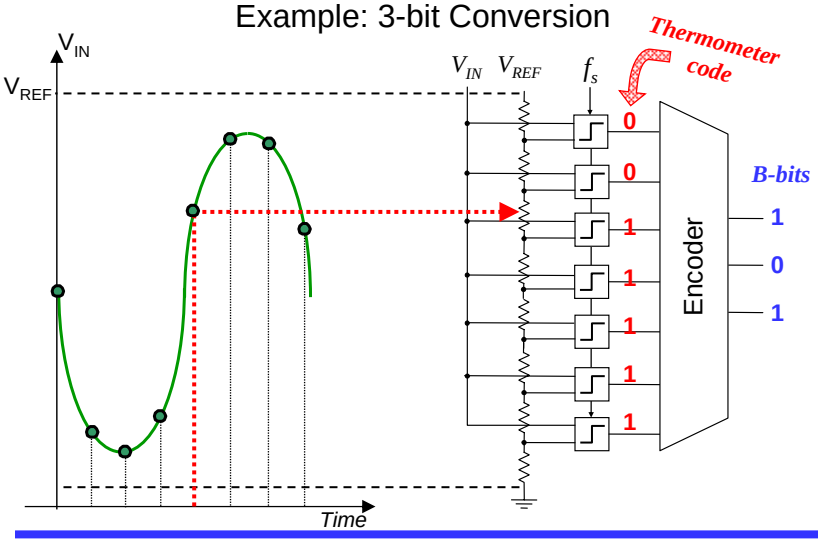
Ref: H. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrating 15 bit CMOS A/D converter," *IEEE Journal of Solid-State Circuits,* vol. 19, pp. 813 - 819, December 1984.

Flash ADC

- B-bit flash ADC:
  - DAC generates all possible 2^B -1 levels
  - 2^B-1 comparators compare V_{IN} to DAC outputs
  - Comparator output:
    - If $V_{DAC} < V_{IN} \rightarrow 0$
    - If $V_{DAC} > V_{IN} \rightarrow 1$
  - Comparator outputs form thermometer code
  - Encoder converts thermometer to binary code

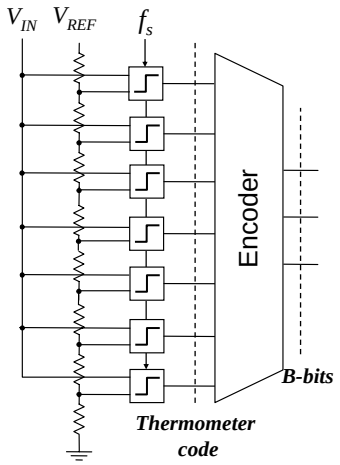


Flash ADC Converter
Example: 3-bit Conversion

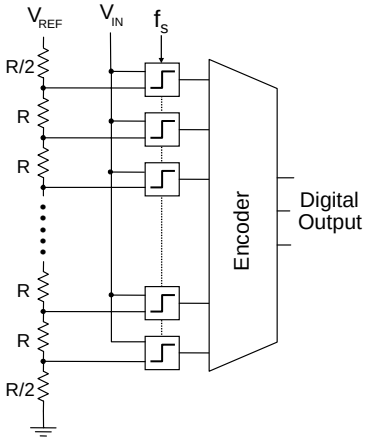


Flash Converter

- Very fast: only 1 clock cycle per conversion
  - Half cycle→ V_{IN} & V_{DAC} comparison
  - Half cycle→ 2^B -1 to B encoding
- High complexity: 2^B-1 comparators
- Input capacitance of 2^B-1 comparators connected to the input node:
  - → High capacitance @ input node



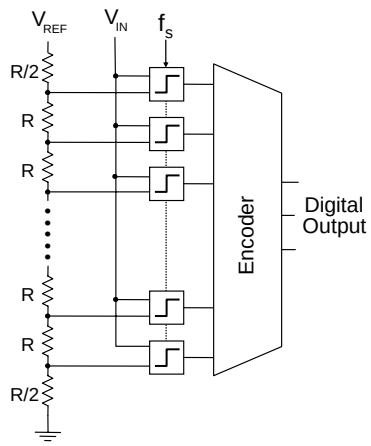
Flash Converter Sources of Error



- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time
- Comparator output:
  - Sparkle codes (… 111101000 …)
  - Metastability

Flash Converter
Example: 8-bits ADC

- 8-bits→ 255 comparators
- V_{REF}=1V → 1LSB=4mV
- DNL<1/2LSB → Comparator input referred offset < 2mV
- 2mV =6σ_{offset}
  → σ_{offset} < 0.33mV



Flash ADC Converter
Example: 8-bits ADC (continued)

→ $1\sigma_{Offset} < 0.33mV$

- Let us assume in the technology used:
  - Voffset-per-unit-sqrt(WxL)=$3\ mVx\ \mu$

$$V_{0\,ffset} = \frac{3mV}{\sqrt{W \times L}} = 0.33mV \quad \rightarrow W \times L = 83\mu^2$$

$$\text{Assuming: } C_{ox} = 9\,fF/\mu^2 \quad \rightarrow C_{GS} = \frac{2}{3} C_{ox} W \times L = 496\,fF$$

$$\rightarrow \text{Total input capacitance: } 255 \times 0.496 = 126.5\,pF\,!$$

  - Issues:
    - Si area quite large
    - Large input capacitance
    - Since depending on input voltage different number of comparator input transistors would be on/off- total input capacitance varies as input varies

    → Nonlinear input capacitance could give rise to signal distortion

Ref: M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits,* vol. 24, pp. 1433 - 1439, October 1989.

Flash ADC Converter
Example (continued)

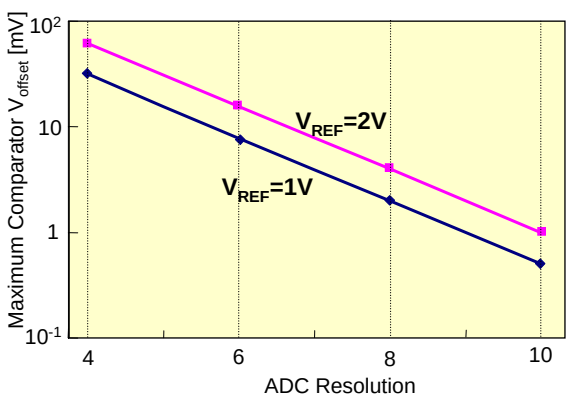
Trade-offs:

- Allowing larger DNL e.g. 1LSB instead of 0.5LSB:
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduces the input capacitance by a factor of 4!
- Reducing the ADC resolution by 1-bit
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduce the input capacitance by a factor of 4

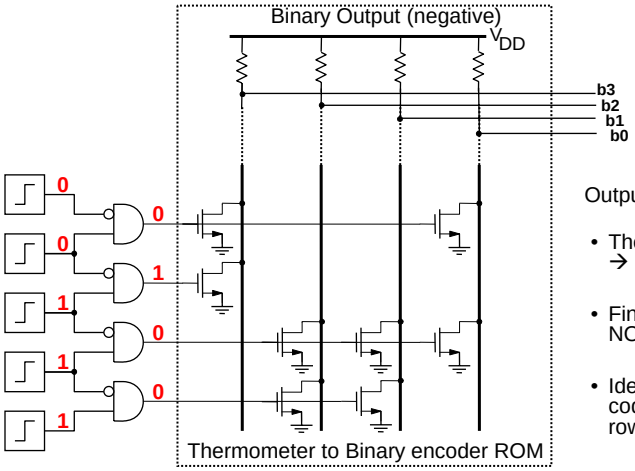
Flash Converter
Comparator Tolerable Maximum Offset versus ADC Resolution

Assumption:
$DNL=0.5LSB$

Note:
Graph shows offset, note that depending on min acceptable yield, the derived offset numbers are associated with 2σ to 6σ offset voltage



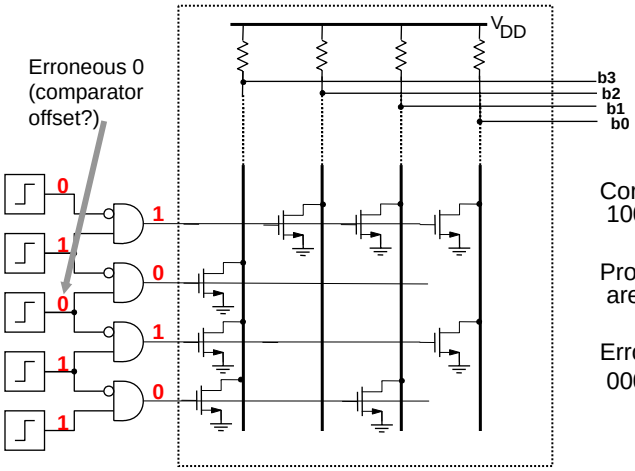
Typical Flash Output Encoder



	b3	b2	b1	b0
Output→	0	1	1	1

- Thermometer code → 1-of-n decoding
- Final encoding → NOR ROM
- Ideally, for each code, only one ROM row is on

Sparkle Codes

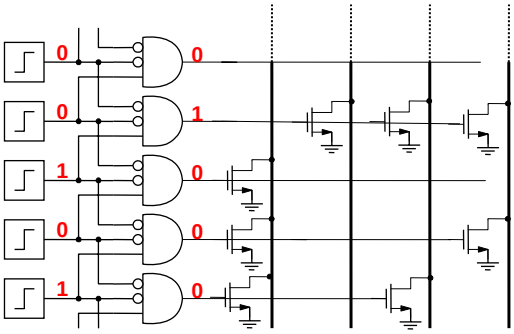


Correct Output: 1000

Problem: Two rows are on

Erroneous Output: 0000

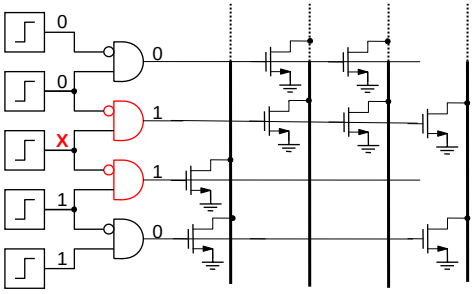
Sparkle Tolerant Encoder



Protects against a *single* sparkle.

Ref: C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," JSSC February 1990, pp. 997-1002

Meta-Stability



Different gates interpret metastable output X differently

Correct output: 1000

Erroneous output: 0000

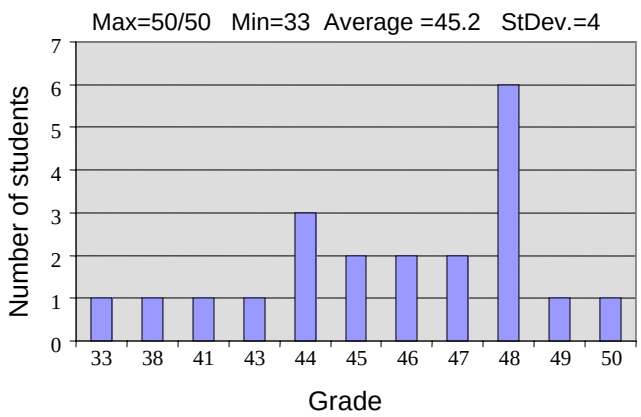
Solutions:
- –Latches (high power)
- –Gray encoding

Ref: C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," JSSC August 1996, pp. 1132-40

Gray Encoding

Thermometer Code							Gray			Binary		
T_1	T_2	T_3	T_4	T_5	T_6	T_7	G_3	G_2	G_1	B_3	B_2	B_1
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	0	0	1	1	0	1	0
1	1	1	0	0	0	0	0	1	0	0	1	1
1	1	1	1	0	0	0	1	1	0	1	0	0
1	1	1	1	1	0	0	1	1	1	1	0	1
1	1	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0	0	1	1	1

$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$
$$G_2 = T_2\overline{T_6}$$
$$G_3 = T_4$$

- Each T_i affects only one G_i
  → Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder

EE247 Fall 2006
Midterm Exam Grades