ADC Converters
- Comparator design
  - Single-stage open-loop amplifier
  - Cascade of open-loop amplifiers
  - Problem associated with DC offset
    - Cascaded output series cancellation
    - Input series cancellation
    - Offset cancellation through additional input pair plus offset storage capacitors
  - Latched comparators
  - Comparator examples

Summary Last Lecture
ADC Converters
- Sampling (continued)
  - Effect of clock jitter on sampling
- ADC architectures and design
  - Serial- slope type
  - Successive approximation
  - Flash
  - Flash ADC sources of error
    - Comparator offset
    - Sparkle code
    - Meta-stability
Voltage Comparators

Play an important role in majority of ADCs
Function: Compare the instantaneous value of two analog signals & generate a digital output voltage based on the sign of the difference:

\[ V_{\text{out}} = \begin{cases} 1 & \text{if } V_{i+} - V_{i-} > 0 \\ 0 & \text{if } V_{i+} - V_{i-} < 0 \end{cases} \]

Voltage Comparator Architectures

Comparator architectures:
- High gain amplifier with differential analog input & single-ended large swing output
  - Output swing has to be compatible with driving digital logic circuits
  - Open-loop amplification → no frequency compensation required
  - Precise gain not required

- Latched comparators; in response to a strobe (clock edge), input stage disabled & digital output stored in a latch till next strobe
  - Two options for implementation:
    • Latch-only comparator
    • Low-gain amplifier + high-sensitivity latch

- Sample-data comparators
  - T/H input
  - Offset cancellation
Comparators Built with High-Gain Amplifier

Amplify $V_{out}(\text{min})$ to $V_{DD}$
$\Rightarrow V_{out}(\text{min})$ determined by ADC resolution

Example: 12-bit ADC with:
- $V_{FS} = 1.5V \Rightarrow 1\text{LSB}=0.36mV$
- $V_{DD}=1.8V$

$\Rightarrow$ For 1.8V output & 0.5LSB precision:
$$A_{\text{Min}} = \frac{1.8V}{0.18mV} \approx 10,000$$

Comparators
1-Single-Stage Amplification

$f_u = \text{unity-gain frequency}, f_{\text{a}} = -3\text{dB frequency}$

$$f_u = \frac{f_a}{A}$$

Example: $f_u=10\text{GHz} \& A = 10,000$

$$f_u = \frac{10\text{GHz}}{10,000} = 1\text{MHz}$$

$$\tau_{\text{settling}} = \frac{1}{2\pi f_u} = 0.16\mu\text{sec}$$

Allow a few $\tau$ for output to settle

$$f_{\text{Clock}} \rightarrow \frac{1}{5\tau_{\text{settling}}} = 1.26\text{MHz}$$

Too slow for majority of applications!
$\Rightarrow$ Try cascade of lower gain stages to broaden frequency of operation
Comparators

2- Cascade of Open Loop Amplifiers

The stages identical $\rightarrow$ small-signal model for the cascades:

One stage:

$$|A_0(0)| = g_m R_L$$

$$\omega_0 = -3\text{dB frequency} = \frac{1}{R_L C_T}$$

$$\omega_u = -\text{unity gain frequency} = G \cdot \text{BW} = \frac{U_m}{C_T}$$

$$\omega_D = \frac{\omega_u}{|A_0(0)|}$$

Open Loop Cascade of Amplifiers

For an N-stage cascade:

$$A_T(j \omega) = |A_0(j \omega)|^N = \left|\frac{A_0(0)}{|A_0(0)|}\right|^N = \left[1 + \frac{1}{|A_0|}\right]^N$$

Define

$$\omega_{\text{in}} = -3\text{dB frequency of the N-stage cascade}$$

Then

$$|A_T(j \omega_{\text{in}})| = \left|\frac{A_0(0)}{|A_0(0)|}\right|^{\frac{N}{2}}$$

and

$$\omega_{\text{in}} = \omega_0 \sqrt{N - 1} = \frac{\omega_u}{|A_0(0)|} \sqrt{N - 1}$$

\[ \text{For specified } |A_0(0)| \]

$$|A_0(0)| = |A_T(0)|^{1/N}$$

$$\Rightarrow \omega_{\text{in}} = \frac{\omega_u}{|A_T(0)|^{1/N}} \sqrt{N - 1}$$

Thus,

$$\omega_{\text{in}} \left[\frac{n}{N}\right] = \frac{\omega_u}{|A_T(0)|^{1/N}} \sqrt{N - 1} \left[\frac{n}{N}\right]$$

$$= |A_T(0)| \left(\frac{N-1}{N}\right) \sqrt{N - 1}$$
Open Loop Cascade of Amplifiers

For $|A_T(\text{DC})|=10,000$

| $N$ | $\omega_0/\omega_o$ | $|A_T(0)|$ |
|-----|--------------------|-----------|
| 1   | 1                  | 10,000    |
| 2   | 64                 | 100       |
| 3   | 236                | 21.5      |
| 4   | 435                | 10        |
| 5   | 611                | 6.3       |
| 10  | 1067               | 2.5       |
| 20  | 1185               | 1.6       |

Example:

$N=3, f_o = 10\text{GHz}$ & $|A_T(0)|=10000$

$f_{oN} = \frac{10\text{GHz}}{(10,000)} \sqrt{2^{1/3}-1} = 237\text{MHz}$

$\tau_{\text{setting}} = \frac{1}{2\pi f_o} = 0.7\text{ns}$

Allow a few $\tau$ for output to settle

$f_{\text{clock}} \rightarrow \frac{1}{5\tau_{\text{setting}}} \approx 290\text{MHz}$

$f_{\text{max}}$ improved from $1.26\text{MHz}$ to $290\text{MHz} \rightarrow \times 236$

Open Loop Cascade of Amplifiers

Offset Voltage

- From offset point of view: high gain/stage is preferred

- Choice of # of stage
  \( \rightarrow \) bandwidth vs offset tradeoff

Input-referred offset

\[ V_{\text{in}} = V_{\text{in1}} + \frac{V_{\text{in2}}}{A_1} + \frac{V_{\text{in3}}}{A_1 \cdot A_2} \]
Open Loop Cascade of Amplifiers

Step Response

- Assuming linear behavior (not slew limited)

\[ v_{o1} = \frac{1}{C} \int_{0}^{t} g_m v_{in} dt = \frac{g_m}{C} v_{in} t \]

\[ v_{o2} = \frac{1}{C} \int_{0}^{t} g_m v_{o1} dt = \frac{g_m}{C} \left( \frac{g_m}{C} \right) v_{in} dt = \frac{1}{2} \left( \frac{g_m}{C} \right)^2 v_{in} t^2 \]

\[ v_{o3} = \frac{1}{C} \int_{0}^{t} g_m v_{o2} dt = \frac{g_m}{C} \left( \frac{1}{2} \left( \frac{g_m}{C} \right)^2 v_{in} t^2 \right) dt \]

\[ = \frac{1}{3} \left( \frac{g_m}{C} \right)^3 v_{in} t^3 \]

N Stages

\[ v_{on} = \left( \frac{g_m}{C} \right)^N \frac{N}{R_f} v_{in} \]

For the output to reach a specified \( v_{out} \) (i.e., \( v_{on} = v_{out} \)) the delay is

\[ \tau_D = \frac{C}{g_m} \left( \frac{N}{N!} \frac{v_{out}}{v_{in}} \right)^{1/N} \]
Open Loop Cascade of Amplifiers

\[ \text{Delay/(C/gm)} \]

- Minimum total delay broad function of N
- Relationship between # of stages resulting in minimize delay \((N_{opt})\) and gain \((V_{out}/V_{in})\) approximately:

\[ N_{opt} = 1 + \log_2 A_T \quad \text{for } A < 1000 \]

\[ N_{opt} = 1.2 \ln A_T \quad \text{for } A \geq 1000 \]

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Offset Cancellation

- In sampled-data cascade of amplifiers Vos can be cancelled
  → Store on ac-coupling caps in series with amp stages
- Offset associated with a specific amp can be cancelled by storing it in series with either the input or the output of that stage
- Offset can be cancelled by adding a pair of auxiliary inputs to the amplifier and storing the offset on capacitors connected to the aux. inputs during offset cancellation phase

Offset Cancellation
Output Series Cancellation

• Amp modeled as ideal
  + $V_{os}$ (input referred)

• Store offset:
  - $S1, S4 \rightarrow$ open
  - $S2, S3 \rightarrow$ closed
  → $V_C = A \cdot V_{os}$


Offset Cancellation
Output Series Cancellation

Amplify:
• S1, S4 → closed
• S2, S3 → open
→ $V_C = A \cdot V_{os}$

Circuit requirements:
• Amp not saturate during offset storage
• High-impedance (C) load → $C_C$ not discharged
• $C_C >> C_L$ to avoid attenuation
• $C_C >> C_{switch}$ avoid excessive offset due to charge injection

\[ V_{out} = A (V_{in} + V_{os}) - V_C \]
\[ = A (V_{in} + V_{os}) - A \cdot V_{os} \]
\[ = A \cdot V_{in} \]
Offset Cancellation
Cascaded Output Series Cancellation

Note: Offset storage capacitors in series with the amplifier outputs

1- S1 open, S2,3,4,5 closed

\[ V_{C1} = A_1 \times V_{os1} \]
\[ V_{C2} = A_2 \times V_{os2} \]
\[ V_{C3} = A_3 \times V_{os3} \]
Offset Cancellation
Cascaded Output Series Cancellation

2- S3 open first
- Feedthrough from S3 → offset on X
- Switch offset, ε, induced on node X
- Since S4 remains closed, offset associated with ε stored on C2

\[
V_x = \varepsilon_3 \\
V_{C1} = A_1 x V_{os1} - \varepsilon_3 \\
V_{C2} = A_2 x (V_{os2} + \varepsilon_3)
\]

Offset Cancellation
Cascaded Output Series Cancellation

3- S4 open
- Feedthrough from S4 → offset on Y
- Switch offset, ε, induces error on node Y
- Since S5 remains closed, offset associated with ε stored on C3

\[
V_y = \varepsilon_4 \\
V_{C2} = A_2 x (V_{os2} + \varepsilon_3) - \varepsilon_4 \\
V_{C3} = A_3 x (V_{os3} + \varepsilon_4)
\]
Offset Cancellation
Cascaded Output Series Cancellation

4- $S_2 \rightarrow$ open, $S_1 \rightarrow$ closed, $S_5 \rightarrow$ open

- $S_1$ closed & $S_2$ open $\rightarrow$ since input connected to low impedance source
  charge injection not of major concern
- Switch offset, $\varepsilon_3$ introduced due to $S_5$ opening

$V_x = A_1x(V_{in} + V_{os1}) - V_{C1}$
$= A_1x(V_{in} + V_{os1}) - (A_1 \cdot V_{os1} - \varepsilon_3)$
$= A_1 \cdot V_{in} + \varepsilon_3$

$V_y = A_2x(V_x + V_{os2}) - V_{C2}$
$= A_2x(A_1V_{in} + \varepsilon_3 + V_{os2}) - [A_2 \cdot (V_{os2} + \varepsilon_3) - \varepsilon_4]$}
$= A_1A_2 \cdot V_{in} + \varepsilon_4$

$V_{out} = A_3x(V_y + V_{os3}) - V_{C3}$
$= A_3(A_2 \cdot A_1 \cdot V_{in} + \varepsilon_4 + V_{os3}) - [A_3 \cdot (V_{os3} + \varepsilon_4) - \varepsilon_5]$}
$= A_1A_2A_3 \cdot V_{in} + \varepsilon_5$
Offset Cancellation
Cascaded Output Series Cancellation

\[ V_{\text{out}} = A_1A_2A_3(V_{\text{in}} + \frac{\varepsilon_5}{A_1A_2A_3}) \]
Input-Refereed Offset = \frac{\varepsilon_5}{A_1A_2A_3}

Example:
3-stage open-loop differential amplifier with offset cancellation + output amplifier (see Ref.)

\[ A_{\text{Total(DC)}} = 2 \times 10^6 = 126\text{dB} \]
Input-referred offset < 5\mu V


Offset Cancellation
Output Series Cancellation

- **Advantages:**
  - Almost compete cancellation
  - Closed-loop stability not required

- **Disadvantages:**
  - Gain per stage must be small
  - Offset storage C in the signal path- could slow down overall performance
Offset Cancellation
Input Series Cancellation

Amplify

\[ V_{\text{in}} - V_C + V_{\text{os}} \xrightarrow{S_2, S_3 \rightarrow \text{open}} A \xrightarrow{S_1 \rightarrow \text{closed}} V_{\text{out}} \]

\[
V_{\text{out}} = -A(V_{\text{in}} + V_C - V_{\text{os}}) = -A\left[V_{\text{in}} + V_{\text{os}}\left(\frac{A}{A+1} - 1\right)\right]
\]

\[ \therefore V_{\text{out}} = -A\left[V_{\text{in}} - \frac{V_{\text{os}}}{A+1}\right] \]

and

\[
\text{Input-Referred Offset} = \frac{V_{\text{os}}}{A+1}
\]

Example: \(A=4\)
\(\rightarrow\) Input-referred offset = \(V_{\text{os}}/5\)

Offset Cancellation
Cascaded Input Series Cancellation

\[
V_{\text{out}} = A_1A_2\left[V_{\text{in}} - V_{\text{os2}}\right] - \frac{\varepsilon_2}{A_1(A_2+1)}
\]

\[
\text{Input-Referred Offset} = \frac{V_{\text{os2}}}{A_1(A_2+1)} - \frac{\varepsilon_2}{A_1}
\]

\(\varepsilon_2\) charge injection associated with opening of \(S_4\)
Offset Cancellation
Input Series Cancellation

• Advantages:
  – In applications such as C-array successive approximation ADCs can use C-array to store offset

• Disadvantages:
  – Cancellation not complete
  – Requires closed loop stability
  – Offset storage C in the signal path- could slow down overall performance

CMOS Comparators
Cascade of Gain Stages

Fully differential gain stages → 1st order cancellation of switch feedthrough offset

1- Output series offset cancellation

2- Input series offset cancellation
CMOS Comparators
Cascade of Gain Stages

3-Combined input & output series offset cancellation

Offset Cancellation

- Cancel offset by additional pair of inputs (Lecture 19 slide 35-37)
Latched Comparators

Compares two input voltages at time $t_x$ & generates a digital output:

- If $V_{i+} - V_{i-} > 0 \rightarrow V_{out} = "1"$
- If $V_{i+} - V_{i-} < 0 \rightarrow V_{out} = "0"$

CMOS Latched Comparators

Comparatior amplification need not be linear
$\rightarrow$ can use a latch $\rightarrow$ regeneration

Latch $\rightarrow$ Amplification + positive feedback
Simplest Form of CMOS Latch

CMOS Latched Comparators
Small Signal Model

Latch can be modeled as a:
→ Single-pole amp + positive feedback
CMOS Latched Comparator

**Latch Delay**

\[ g_m V = \frac{V}{R_L} + C \frac{dV}{dt} \]

\[ g_m \left( 1 - \frac{1}{g_m R_L} \right) V = \frac{g_m}{C} \left( 1 - \frac{1}{g_m R_L} \right) \frac{dt}{V} = \frac{dV}{V} \]

Integrating both sides:

\[ g_m \left( 1 - \frac{1}{g_m R_L} \right) \int_{t_i}^{t_f} dt = \int_{V_i}^{V_f} \frac{1}{V} dV \]

\[ \left[ t_f - t_i \right] = \int_{V_i}^{V_f} \frac{1}{V} dV = \ln \frac{V_f}{V_i} = \ln a - \ln b = \ln \frac{a}{b} \]

**Latch Delay:**

\[ t_n = t_f - t_i = C \left( 1 - \frac{1}{g_m R_L} \right) \ln \left( \frac{V_f}{V_i} \right) \]

For \( g_m R_L \gg 1 \)

\[ t_n = \frac{C}{g_m} \ln \left( \frac{V_f}{V_i} \right) \]

**CMOS Latched Comparators**

**Normalized Latch Delay**

\[ t_n = \frac{C}{g_m} \ln \left( \frac{V_f}{V_i} \right) \]

\[ \frac{V_f}{V_i} \rightarrow \text{Latch Gain} = A_i \]

\[ \rightarrow t_n \approx \frac{C}{g_m} \ln A_i \]

\[ t_n (3\text{-stage amp}) = 18.2 \left( \frac{C}{g_m} \right) \]

Compared to a 3-stage open-loop cascade of amps for equal overall gain of 1000

\[ \rightarrow \text{Latch faster by about x3} \]
Latch-Only Comparator

• Faster compared to cascade of open-loop amplifiers

• Main problem associated with latch-only comparator topology:
  – High input-referred offset voltage (as high as 100mV!)
  
• Solution:
  – Use preamplifier to amplify the signal and reduce overall input-referred offset

Pre-Amplifier + Latch

Overall Input-Referred Offset

Latch offset attenuated by preamp gain when referred to preamp input. Assuming the two offset sources are uncorrelated:

\[
\sigma_{\text{Input-Ref. Offset}} = \sqrt{\sigma_{\text{Vos Preamp}}^2 + \frac{1}{A_{\text{Preamp}}} \sigma_{\text{Vos Latch}}^2}
\]

Example: \( \sigma_{\text{Vos Preamp}} = 4\, \text{mV} \) & \( \sigma_{\text{Vos Latch}} = 50\, \text{mV} \) & \( A_{\text{Preamp}} = 10 \)

\[
\sigma_{\text{Input-Ref. Offset}} = \sqrt{4^2 + \frac{1}{10^2} \times 50^2} = 6.4\, \text{mV}
\]
Pre-Amplifier Tradeoffs

• Example:
  - Latch offset 50 to 100mV
  - Preamp DC gain 10X
  - Preamp input-referred latch offset 5 to 10mV
  - Input-referred preamplifier offset 2 to 10mV
  - Overall input-referred offset 5.5 to 14mV

  → Addition of preamp reduces the latch input-referred offset reduced by ~7 to 9X → ~extra 3-bit resolution!

Comparator Preamplifier Gain-Speed Tradeoffs

• Amplifier maximum Gain-Bandwidth product \(f_u\) for a given technology, typically a function of maximum device \(f_t\)

\[
\begin{align*}
  f_u & \quad \text{unity gain frequency, } f_0 = -3\text{dB frequency} & \tau_0 & \quad \text{settlement time} \\
  f_0 & = \frac{f_u}{A_{\text{preamp}}} \\
  f_0 & = \frac{1\text{GHz}}{10} = 100\text{MHz} \\
  \tau_0 & = \frac{1}{2\pi f_0} = 1.6\text{sec}
\end{align*}
\]

→ Tradeoff:
  • To reduce the effect of latch offset → high preamp gain desirable
  • Fast comparator → low preamp gain
Latched Comparator

Important features:
- Maximum clock rate $f_s \Rightarrow$ settling time, slew rate, small signal bandwidth
- Resolution $\Rightarrow$ gain, offset
- Overdrive recovery
- Input capacitance (and linearity of input capacitance!)
- Power dissipation
- Input common-mode range and CMR
- Kickback noise
- ...

Comparators Overdrive Recovery

Linear model for a single-pole amplifier:

$U \to$ amplification after time $t_a$

During reset amplifier settles exponentially to its zero input condition with $\tau_0 = RC$

Assume $V_m \to$ maximum input normalized to $1/2$ LSB ($=1$)

Example: Worst case input/output waveforms

Previous input $\to$ max. possible e.g. VFS
Current input $\to$ min. input-referred signal (0.5 LSB)
Comparators Overdrive Recovery

Example: Worst case input/output waveforms

- If recovery time is not long enough to allow output to discharge (recover) from previous state, then it may not be able to resolve the small current input → error
- To minimize this effect:
  1. Passive clamp
  2. Active restore
  3. Low gain/stage

Comparators Overdrive Recovery

Limiting or Resetting Output

Clamp
- Adds parasitic capacitance

Active Restore
- After outputs are latched by following stage
  - Activate & equalize output nodes
CMOS Latched Comparator Delay Including Preamplifier

Latch delay found previously:
\[
\tau_D = \frac{C}{g_m} \ln \left( \frac{V_C}{V_{in}} \right)
\]

Assuming gain of $A_g$ for the preamplifier:

\[
\tau_D = \frac{C}{g_m} \ln \left( A_g \frac{V_C}{V_{in}} \right)
\]

---

Latched Comparator Including Preamplifier Example

Preamplifier gain:
\[
A_g = \frac{g_{m1}}{g_{m3}} = \frac{\left( V_{GS1} - V_{th1} \right)}{\left( V_{GS3} - V_{th1} \right)}
\]

Comparator delay:
\[
\tau_D = \frac{C}{g_m} \ln \left( A_g \frac{V_0}{V_{in}} \right)
\]
Comparator Dynamic Behavior

\[ \tau_{\text{Delay}} = \frac{C}{g_m} \ln \left( \frac{A_v V_0}{V_{\text{in}}} \right) \]

Comparator Resolution

\[ \Delta t = \left( \frac{g_m}{C} \right) \ln \left( \frac{V_{\text{out1}}}{V_{\text{out2}}} \right) \]
Comparator Voltage Transfer Function
Non-Idealities

\[ V_{\text{out}} \]

\[ V_{\text{in}} \]

\[ V_{\text{Offset}} \]

-0.5LSB

0.5LSB

\[ \varepsilon \]

\[ V_{\text{Offset}} \rightarrow \text{Comparator offset voltage} \]

\[ \varepsilon \rightarrow \text{Meta-Stable region (output ambiguous)} \]

---

CMOS Comparator Example

- Flash ADC: 8bits, +/-1/2LSB INL @ fs=15MHz (VDD=5V, Vref=3.8V, LSB~15mV)
- No offset cancellation

Comparator with Auto-Zero


Flash ADC
Comparator with Auto-Zero

Flash ADC
Comparator with Auto-Zero

\[ V_o = A_{ij} \cdot A_{ip} [(V_{in} - V_{ref}) - (V_{c} - V_{c}) - V_{offset}] \]

Substituting for \((V_{c} - V_{c})\) from previous cycle:

\[ V_o = A_{ij} \cdot A_{ip} [(V_{in} - V_{ref}) - (V_{p} - V_{s})] \]

Note: Offset is cancelled & difference between input & reference established


Auto-Zero Implementation

Comparator Example

- Variation on Yukawa latch used w/o preamp
- Good for low resolution ADCs (in this case 1.5bit/stage pipeline ADC + digital correction)
- Note: M1, M2, M11, M12 operate in triode mode
- M11 & M12 added to vary comparator threshold
- Conductance at node X is sum of $G_{M1}$ & $G_{M11}$


Comparator Example (continued)

- M1, M2, M11, M12 operate in triode mode with all having equal L
- Conductance of input devices:
  \[ G_1 = \frac{\mu_{ox}}{L} \left[ W_1 (V_{th1} - V_{th}) + W_1 (V_{R} + V_{th}) \right] \]
  \[ G_2 = \frac{\mu_{ox}}{L} \left[ W_2 (V_{th1} - V_{th}) + W_2 (V_{R} + V_{th}) \right] \]
  \[ \Delta G = \frac{\mu_{ox}}{L} \left[ W_1 (V_{th1} - V_{th2}) - W_2 (V_{R} + V_{th}) \right] \]
- To 1st order, for $W1= W2$ & $W11=W12$
  \[ V_{th} = \frac{W11}{W1} x V_R \]
  where $V_R = V_{R+} - V_{R-}$
- $V_R$ fixed $W11, J2$ varied $\Rightarrow$ Eliminates need for resistive divider

Comparator Example

- Used in a pipelined ADC with digital correction
  → no offset cancellation required
- Note: Differential reference
- M7, M8 operate in triode region
- Preamp gain ~10
- Input buffers suppress kick-back
- \( \Phi_1 \) high \( \rightarrow \) \( C_s \) charged to \( VR \) & \( \Phi_2 B \) is also high \( \rightarrow \) current diverted to latch \( \rightarrow \) comparator output in hold mode
- \( \Phi_2 \) high \( \rightarrow \) \( C_s \) connected to \( S/Hout \) & comparator input (VR-S/Hout), current sent to preamp \( \rightarrow \) comparator in amplify mode


Bipolar Comparator Example

- Used in 8bit 400Ms/s & 6bit 2Gb/s flash ADC
- Signal amplification during \( \Phi_1 \) high, latch operates when \( \Phi_1 \) low
- Input buffers suppress kick-back & input current
- Separate ground and supply buses for front-end preamp \( \rightarrow \) kick-back noise reduction