EE247
Lecture 26

• This lecture is taped on Wed. Nov. 28th due to conflict of regular class hours with a meeting

• Any questions regarding this lecture could be discussed during regular office hours or in class at the next lecture

• Please hand in your homework #8 solution to Yida Duan, otherwise bring it to H.K.’s office hour

• Regular office hours held today, Nov. 29th, 2:30 to 3:30pm, @ 563 Cory Hall

EE247
Lecture 26

• Oversampled ADCs 1st order $\Sigma \Delta$ modulator (continued)
  • In-band quantization noise analysis & dynamic range
  • Issue: DC input results in periodic tones $\rightarrow$ limit cycle oscillations

  – 2nd order $\Sigma \Delta$ modulator
    • Dynamic range
    • Practical implementation
      – Effect of various building block nonidealities on the $\Sigma \Delta$ performance
      – Example
Summary of Last Lecture

Oversampled ADCs:

– Reduction of baseband quantization noise power by combining oversampling with clever use of feedback around the quantizer

– Allows trading speed for resolution

– No stringent requirements imposed on analog building blocks (more today)

– Takes advantage of low cost, low power digital filtering available in fine-line CMOS technology

1st Order Sigma-Delta Modulators

Analog 1-Bit $\Sigma\Delta$ modulators convert a continuous time analog input $v_{in}$ into a 1-Bit digital sequence $D_{OUT}$
1\textsuperscript{st} Order \(\Sigma\Delta\) Modulator

1\textsuperscript{st} order modulator, simplest loop filter → an integrator

\[
H(z) = \frac{z^{-1}}{1 - z^{-1}}
\]

Note: Non-linear system with memory → difficult to analyze

1\textsuperscript{st} Order \(\Sigma\Delta\) Modulator

STF and NTF

Signal transfer function:

\[
\text{STF} = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} = z^{-1} \quad \Rightarrow \quad \text{Delay}
\]

Noise transfer function:

\[
\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1} \quad \Rightarrow \quad \text{Differentiator}
\]
Noise Transfer Function

\[
N_{TF} = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1} \quad \text{set} \quad z = e^{j\omega T}
\]

\[
N_{TF}(j\omega) = (1 - e^{-j\omega T}) = 2e^{-j\omega T/2} \left( \frac{e^{j\omega T/2} - e^{-j\omega T/2}}{2} \right)
\]

\[
= 2e^{-j\omega T/2} \sin(\omega T/2)
\]

\[
= 2e^{-j\omega T/2} e^{-j\pi/2} \left[ \sin(\omega T/2) \right]
\]

\[
= \left[ 2\sin(\omega T/2) \right] e^{-j(\omega T - \pi)/2}
\]

where \( T = 1/f_s \)

Thus:

\[
|N_{TF}(f)| = 2|\sin(\omega f/2)| = 2|\sin(\pi f/f_s)|
\]

\[
N_s(f) = |N_{TF}(f)|^2 N_c(f)
\]
Quantizer Error

• For quantizers with many bits

\[
\overline{e^2(kT)} = \frac{\Delta^2}{12}
\]

• Let’s use the same expression for the 1-Bit case

• Use simulation to verify validity

• Experience: Often sufficiently accurate to be useful, with enough exceptions to be careful

First Order ΣΔ Modulator
Simulated Noise Transfer Characteristic

- Confirms assumption of quantization noise being white at insertion point
- Linearized model seems to be accurate

\[
N_s(f) = 4\sin\left(\pi f / f_s\right)^2
\]
First Order ΣΔ Modulator
In-Band Quantization Noise

\[ NTF(z) = 1 - z^{-1} \]

\[ |NTF(f)|^2 = 4 \left| \sin(\pi f / f_s) \right|^2 \quad \text{for } M >> 1 \]

\[ S_y = \int_{-B}^{B} \left| S_Q(f) \right|^2 NTF(z)_{z=e^{j\pi f/T}} \, df \]

\[ \approx \int_{-\frac{f_s}{2M}}^{\frac{f_s}{2M}} \frac{1}{f_s} \frac{\Delta^2}{12} (2\sin\pi fT)^2 \, df \]

\[ \rightarrow S_Q = \frac{\pi^2}{3} \frac{1}{M^3} \frac{\Delta^2}{12} \]

Total in-band quantization noise

1st Order ΣΔ Dynamic Range

\[ DR = 10\log \left( \frac{\text{full-scale signal power}}{\text{inband noise power}} \right) = 10\log \left( \frac{S_X}{S_Q} \right) \]

\[ S_X = \frac{1}{2} \left( \frac{\Delta}{2} \right)^2 \]

sinusoidal input, \( STF = 1 \)

\[ S_Q = \frac{\pi^2}{3} \frac{1}{M^3} \frac{\Delta^2}{12} \]

\[ \frac{S_X}{S_Q} = \frac{9}{2\pi^2} M^3 \]

\[ DR = 10\log \left( \frac{9}{2\pi^2} M^3 \right) + 30\log M \]

\[ DR = -3.4\,\text{dB} + 30\log M \]

2X increase in \( M \rightarrow 9\,\text{dB (1.5-Bit) increase in dynamic range} \)
Oversampling and Noise Shaping

• $\Sigma\Delta$ modulators have interesting characteristics
  – Unity gain for input signal $V_{IN}$
  – Significant attenuation of in-band quantization noise injected at quantizer input
  – Performance significantly better than 1-Bit noise performance possible for frequencies $< f_s$

• Increase in oversampling ($M = f_s/f_N > 1$) improves SQNR considerably
  – 1st order $\Sigma\Delta$: DR increases 9dB for each doubling of $M$
  – To first order, SQNR independent of circuit complexity and accuracy

• Analysis assumes that the quantizer noise is "white"
  – Not entirely true in practice, especially for low-order modulators
  – Practical modulators suffer from other noise sources also (e.g. thermal noise)

1st Order $\Sigma\Delta$ Modulator Response to DC Input

• Matlab & Simulink model from Lecture 25 used
• Input $\rightarrow$ DC at 1/11 full-scale level
1st Order ΣΔ
Response to DC Input

- DC input A = 1/11
- Output spectrum shows DC component plus distinct tones!!
- Tones frequency shaped the same as quantization noise
  - More prominent at higher frequencies
  - Seems like periodic quantization “noise”

Limit Cycle Oscillation

DC input 1/11 → Periodic sequence:

<table>
<thead>
<tr>
<th>Time (t/T)</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.4</td>
</tr>
<tr>
<td>10</td>
<td>0.2</td>
</tr>
<tr>
<td>20</td>
<td>0.0</td>
</tr>
<tr>
<td>30</td>
<td>-0.2</td>
</tr>
<tr>
<td>40</td>
<td>-0.4</td>
</tr>
<tr>
<td>50</td>
<td>-0.4</td>
</tr>
</tbody>
</table>

- Average = 1/11
1st Order $\Sigma\Delta$ Limit Cycle Oscillation

- Problem: quantization noise becomes periodic in response to low level DC inputs & could fall within passband of interest!
- Solution:
  - Use dithering (inject noise-like signal at the input): randomizes quantization noise
  - If circuit thermal noise is large enough $\Rightarrow$ acts as dither
  - Second order loop

1st Order $\Sigma\Delta$ Modulator
Linearized Model Analysis

$$Y(z) = z^{-1} X(z) + \left(1 - z^{-1}\right) E(z)$$
2\textsuperscript{nd} Order $\Sigma\Delta$ Modulator

- Two integrators in series
- Single quantizer (typically 1-bit)
- Feedback from output to \textit{both} integrators
- Tones less prominent compared to 1st order

Linearized Model Analysis

Recursive derivation:

$$Y_n = X_{n-1} + (E_n - 2E_{n-1} + E_{n-2})$$

Using the delay operator $z^{-1}$:

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)^2 E(z)$$
2nd Order $\Sigma\Delta$ Modulator
In-Band Quantization Noise

$$NTF(z) = \left(1 - z^{-1}\right)^2$$

$$|NTF(f)|^2 =$$

$$= 2^4 \left| \sin\left(\pi f / f_s\right) \right|^4$$ for $M >> 1$

$$\bar{S}_Q = \int_{b-B}^{B} S_Q(f) \left| NTF(z) \right|^2_{z=e^{i\pi s f}} df$$

$$\equiv \int_{-f_s M}^{f_s M} \frac{\Delta^2}{12} \left(2 \sin \pi T f\right)^4 df$$

$$= \frac{\pi^4}{5} \frac{1}{M^2} \frac{\Delta^2}{12}$$
2\textsuperscript{nd} Order ΣΔ Modulator

Dynamic Range

\[ DR = 10 \log \left( \frac{\text{full-scale signal power}}{\text{inband noise power}} \right) = 10 \log \left( \frac{S_X}{S_Q} \right) \]

\[ S_X = \frac{1}{2} \left( \frac{\Delta}{2} \right)^2 \]

\[ S_Q = \frac{\pi^4}{5} \cdot \frac{1}{M^2} \cdot \\frac{\Delta^2}{12} \]

\[ S_X = \frac{15}{2\pi^4} \cdot M^5 \]

\[ DR = 10 \log \left( \frac{15}{2\pi^4} \cdot M^5 \right) = 10 \log \left( \frac{15}{2\pi^4} \right) + 50 \log M \]

\[ DR = -11.1 \text{dB} + 50 \log M \]

2X increase in \( M \rightarrow 15 \text{dB} \) (2.5-bit) increase in DR

---

2\textsuperscript{nd} Order vs 1\textsuperscript{st} Order ΣΔ Modulator

Dynamic Range

<table>
<thead>
<tr>
<th>( M )</th>
<th>( 2\textsuperscript{nd} \text{ Order D.R.} )</th>
<th>( 1\textsuperscript{st} \text{ Order D.R.} )</th>
<th>Resolution (2\textsuperscript{nd} order - 1\textsuperscript{st} order)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>49 dB (7.8bit)</td>
<td>33dB (5.2bit)</td>
<td>2.6 bit</td>
</tr>
<tr>
<td>32</td>
<td>64 dB (10.3bit)</td>
<td>42dB (6.7bit)</td>
<td>3.6 bit</td>
</tr>
<tr>
<td>256</td>
<td>109 dB (17.9bit)</td>
<td>68.8dB (11.1bit)</td>
<td>6.8 bit</td>
</tr>
<tr>
<td>1024</td>
<td>139 dB (22.8bit)</td>
<td>87dB (14.2bit)</td>
<td>8.6 bit</td>
</tr>
</tbody>
</table>

Note: For higher oversampling ratios resolution of 2\textsuperscript{nd} order modulator significantly higher compared to 1\textsuperscript{st} order
2nd Order $\Sigma\Delta$ Modulator Example

- Digital audio application
  - Signal bandwidth 20kHz
  - Desired resolution 16-bit

$16$-bit → $98$dB Dynamic Range

$DR_{2\text{nd order }\Sigma\Delta} = -11.1dB + 50\log M$

$M_{\text{min}} = 153$

$M \rightarrow 256 = 2^8$ to reasons:
1. Allow some margin so that thermal noise dominate & provides dithering
2. Choice of $M$ power of 2 → ease of digital filter implementation

→ Sampling rate $(2\times20kHz + 5kHz)M = 12MHz$ (quite reasonable!)

Limit Cycle Tones in 1st Order & 2nd Order $\Sigma\Delta$ Modulator

- Higher oversampling ratio → lower tones
- 2nd order tones much lower compared to 1st
- 2X increase in M decreases the tones by 6dB for 1st order loop and 12dB for 2nd order loop

ΣΔ Implementation
Practical Design Considerations

- Internal node scaling & clipping
- Effect of finite opamp gain & linearity
- KT/C noise
- Opamp noise
- Effect of comparator nonidealities
- Power dissipation considerations

Switched-Capacitor Implementation 2nd Order ΣΔ
Nodes Scaled for Maximum Dynamic Range

- Modification (gain of ½ in front of integrators) reduce & optimize required signal range at the integrator outputs ~ 1.7x input full-scale (Δ)
- Note: Non-idealities associated with 2nd integrator and quantizer when referred to the ΣΔ input is attenuated by 1st integrator high gain
  → The only building block requiring low-noise and high accuracy is the 1st integrator

2nd Order ΣΔ Modulator
Example: Switched-Capacitor Implementation

- Fully differential front-end
- Two bottom-plate integrators
- 1-bit DAC is made of switches and Vrefs

Switched-Capacitor Implementation 2nd Order ΣΔ
Phase 1

During phase 1:
- 1st integrator samples Vin on 1st stage C1
- 2nd integrator samples output of 1st integrator
- Comparator senses polarity of 2nd intg. output → result saved in output latch
- S3 opens prior to S1 → minimize effect of charge injection
Switched-Capacitor Implementation 2\textsuperscript{nd} Order

\[ \Sigma \Delta \]

\textbf{Phase 2}

- Input sampled during \( \phi_1 \) transferred to \( C_2 \) \( \rightarrow \) integration
- Note: \( S_2 \) connects integrator inputs to \( + \) or \( - \) \( V_{\text{ref}} \), polarity depends on whether \( D_{\text{out}} \) is \( 0 \) or \( 1 \)

2\textsuperscript{nd} Order \( \Sigma \Delta \) Modulator

Switched-Capacitor Implementation

- The \( \frac{1}{2} \) loss in front of each integrator implemented by choice of:
  \[ C_2 = 2C_1 \quad \Rightarrow f_{\text{intg}} = f_s / (4\pi) \]
Design Phase Simulations

- Design of oversampled ADCs requires simulation of extremely long data traces
- SPICE type simulators:
  - Normally used to test for gross circuit errors only
  - Too slow for detailed performance verification
- Typically, behavioral modeling is used in MATLAB-like environments
- Circuit non-idealities either computed or found by using SPICE at subcircuit level
- Non-idealities introduced in the behavioral model one-by-one first to fully understand the effect of each individually
- Next step is to add as many of the non-idealities simultaneously as possible to verify whether there are interaction among non-idealities

2nd Order ΣΔ

Effect of 1st Integrator Maximum Signal Handling Capability on SNR

Effect of 1st Integrator maximum signal handling capability on converter SNR
→ No SNR loss for max. sig. handling > 1.7Δ

Effect of 2nd Integrator Maximum Signal Handling Capability on SNR

- Effect of 2nd Integrator maximum signal handling capability on SNR
  \[ \rightarrow \text{No SNR loss for max. sig. handling} > 1.7 \Delta \]


Effect of Integrator Finite DC Gain

\[ H(z)_{\text{ideal}} = \frac{C_x}{C_I} \times \frac{z^{-1}}{1-z^{-1}} \]

\[ H(z)_{\text{Finite DC Gain}} = \frac{C_x}{C_I} \times \frac{\frac{a}{1+a+C_x/C_I}z^{-1}}{1-\frac{1+a}{1+a+C_x/C_I}z^{-1}} \]

\[ \rightarrow H(\text{DC}) = a \]
2nd Order $\Sigma\Delta$

Effect of Integrator Finite DC Gain

• Note: Quantization transfer function wrt output has integrator in the feedback path:

\[
\frac{D_{out}}{e_Q} = \frac{1}{1 + H(\omega)}
\]

→ @ DC for ideal integ: \( \frac{D_{out}}{e_Q} = 0 \)

→ @ DC for real integ: \( \frac{D_{out}}{e_Q} \sim \frac{1}{a} \)

2nd Order $\Sigma\Delta$

Effect of Integrator Finite DC Gain

• Low integrator DC gain → Increase in total in-band quantization noise

• Can be shown: If \( a > M \) (oversampling ratio) → Insignificant degradation in SNR

• Normally DC gain designed to be >> M in order to suppress nonlinearities
2nd Order $\Sigma\Delta$

Effect of Integrator Finite DC Gain

- Example: $a = 2M \rightarrow 0.4$dB degradation in SNR
- $a = M \rightarrow 1.4$dB degradation in SNR


2nd Order $\Sigma\Delta$

Effect of Comparator Non-Idealities on $\Sigma\Delta$ Performance

1-bit A/D $\rightarrow$ Single comparator
- Speed must be adequate for the operating sampling rate
- Input referred offset- feedback loop & high DC intg. Gain suppresses the effect
  $\rightarrow$ $\Sigma\Delta$ performance quite insensitive to comparator offset
- Input referred comparator noise- same as offset
- Hysteresis= Minimum overdrive required to change the output
$\text{2nd Order } \Sigma \Delta$

Comparator Hysteresis

Hysteresis = Minimum overdrive required to change the output

 Comparator hysteresis $\lt \frac{\Delta}{25}$ does not affect SNR
 E.g. $\Delta=1$V, comparator hysteresis up to 40mV tolerable

Key Point: One of the main advantages of $\Sigma \Delta$ ADCS $\rightarrow$ Highly tolerant of comparator and in general building-block non-idealities
2nd Order \(\Sigma \Delta\)

**Effect of Integrator Nonlinearities**

\[
\begin{align*}
\text{Ideal Integrator} & \\
u(kT) & \xrightarrow{\text{Delay}} \nu(kT) \\
v(kT+T) = u(kT) + v(kT)
\end{align*}
\]

With non-linearity added:

\[
v(kT+T) = u(kT) + \alpha_2[u(kT)]^2 + \alpha_3[u(kT)]^3 + \ldots + \beta_2[v(kT)]^2 + \beta_3[v(kT)]^3 + \ldots
\]


---

**2nd Order \(\Sigma \Delta\)**

**Effect of Integrator Nonlinearities (Single-Ended)**

- Simulation for single-ended topology
- Even order nonlinearities can be significantly attenuated by using differential circuit topologies

2nd Order $\Sigma\Delta$

Effect of Integrator Nonlinearities

- Simulation for single-ended topology
- Odd order nonlinearities (3rd in this case)


2nd Order $\Sigma\Delta$

Effect of Integrator Nonlinearities

- Odd order nonlinearities (usually 3rd) could cause significant loss of SNR for high resolution oversampled ADCs
- Two significant sources of non-linearities:
  - Non-linearities associated with opamp used to build integrators
    - Opamp open-loop non-linearities are suppressed by the loopgain since there is feedback around the opamp
    - Class A opamps tend to have lower open loop gain but more linear output versus input transfer characteristic
    - Class A/B opamps typically have higher open loop gain but non-linear transfer function. At times this type is preferred for $\Sigma\Delta$ AFE due to its superior slew rate compared to class A type
  - Integrator capacitor non-linearities
    - Poly-SiO2-Poly capacitors have in the order of 10ppm/V non-linearity
    - Metal-SiO2-Metal Cs ~ 1ppm/V