EE247 Lecture 28

• Administrative
  – Extra office hours next week @ 563 Cory:
    Wed. Dec. 12th, 2pm-4pm
    Thurs. Dec. 13th, 10am-12pm

  – Project submission:
    • Deadline extended: Thurs. Dec. 13th or Frid. Dec. 14th
    • If you have chosen to do the project, please make an appointment with the instructor for 15mins per each project report to present the results:
      Thurs. Dec. 13th after 1pm or
      Frid. Dec. 14th after 10am

• Higher order $\Sigma\Delta$ modulators
  – Cascaded $\Sigma\Delta$ modulators (MASH) (last lecture)
  – Forward path multi-order filter (continued)

• Bandpass $\Sigma\Delta$ modulators

• Testing of $\Sigma\Delta$ modulator front-end

• Acknowledgements

• Examples of systems utilizing analog-digital interface circuitry (not part of final exam)
Higher Order $\Sigma\Delta$ Modulators

(2) Multi-Order Filter

$Y(z) = \frac{H(z)}{1 + H(z)} X(z) + \frac{1}{1 + H(z)} E(z)$

$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}$

- Zeros of NTF (poles of H(z)) can be strategically positioned to suppress in-band noise spectrum
- Approach: Design NTF first and solve for H(z)

Example: Modulator Specification

- Example: Audio ADC
  - Dynamic range (DR) 18 Bits
  - Signal bandwidth (B) 20 kHz
  - Nyquist frequency ($f_N$) 44.1 kHz
  - Modulator order (L) 5
  - Oversampling ratio ($M = f_s/f_N$) 64
  - Sampling frequency ($f_s$) 2.822 MHz

- The order L and oversampling ratio M are chosen based on
  - SQNR > 120dB
Noise Transfer Function, NTF(z)

\[
\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}
\]

- Chebychev 2 filter chosen
- \( \rightarrow \) zeros in stop-band

```
% stop-band attenuation Rstop=80dB, L=5 ...
L=5;
Rstop = 80;
B=20000;
[b,a] = cheby2(L, Rstop, B, 'high');

% normalize
b = b/b(1);
NTF = filt(b, a, ...);
```

Loop-Filter Characteristics

\[ H(z) = \frac{1}{NFT} - 1 \]
Modulator Topology

Simulation Model

Internal Node Voltages

- Internal signal peak amplitudes are weak function of input level (except near overload)
- Maximum peak-to-peak voltage swing approach ±10V! Exceed supply voltage!
- Solutions:
  - Reduce $V_{ref}$ ??
  - Node scaling
Node Scaling Example:
3rd Integrator Output Voltage Scaled by $\alpha$

$K3 \cdot \alpha$, $b1/\alpha$, $a3/\alpha$, $K4/\alpha$, $b2 \cdot \alpha$

$V_{\text{new}} = V_{\text{old}} \cdot \alpha$

Node Voltage Scaling

$\alpha = \frac{1}{10}$
$k1 = \frac{1}{10}$; $k2 = 1$; $k3 = \frac{1}{4}$; $k4 = \frac{1}{4}$; $k5 = \frac{1}{8}$; $a1 = 1$; $a2 = \frac{1}{2}$; $a3 = \frac{1}{2}$; $a4 = \frac{1}{4}$; $a5 = \frac{1}{4}$; $b1 = \frac{1}{512}$; $b2 = \frac{1}{16} - \frac{1}{64}$; $g = 1$

- Integrator output range reasonable for new parameters
- But: maximum input signal limited to -5dB (-7dB with safety) – fix?
Input Range Scaling

Increasing the DAC levels by using higher value for $g$ reduces the analog to digital conversion gain:

$$\frac{D_{\text{OUT}}(z)}{V_{\text{IN}}(z)} = \frac{H(z)}{1 + gH(z)} \approx \frac{1}{g}$$

Increasing $V_{\text{IN}}$ and $g$ by the same factor leaves 1-Bit data unchanged.

Scaled Stage 1 Model

$g$ modified:
From 1 to 2.5;

→ Overload input level shifted up by 8dB

$+2\text{dB}$
Stability Analysis
(not included in final exam)

• Approach: linearize quantizer and use linear system theory!
• One way of performing stability analysis ➔ use RLocus in Matlab with H(z) as argument and Geff as variable
• Effective quantizer gain
  \[ G_{eff}^2 = \frac{y^2}{q^2} \]
• Can obtain \( G_{eff} \) from simulation


Stability Analysis

\[ STF = \frac{G \cdot H(z)}{1 + G \cdot H(z)} \]
\[ H(z) = \frac{N(z)}{D(z)} \]
\[ \rightarrow STF = \frac{G \cdot N(z)}{D(z) + G \cdot N(z)} \]

• Zeros of STF same as zeros of H(z)
• Poles of STF vary with G
• For G=0 (no feedback) poles of the STF same as poles of H(z)
• For G=large, poles of STF move towards zeros of H(z)
• Draw root-locus: for G values for which poles move to LHP (s-plane) or inside unit circle (z-plane) ➔ system is stable
Modulator z-Plane Root-Locus

- As $G_{eff}$ increases, poles of STF move from poles of $H(z)$ ($G_{eff} = 0$) to zeros of $H(z)$ ($G_{eff} = \infty$).
- Pole-locations inside unit-circle correspond to stable STF and NTF.
- Need $G_{eff} > 0.45$ for stability.

Effective Quantizer Gain, $G_{eff}$

- Large inputs $\Rightarrow$ comparator input grows.
- Output is fixed ($\pm 1$) $\Rightarrow$ $G_{eff}$ drops $\Rightarrow$ modulator unstable for large inputs.
- Solution:
  - Limit input amplitude
  - Detect instability (long sequence of $+1$ or $-1$) and reset integrators.
  - Be aware that signals grow slowly for nearly stable systems $\Rightarrow$ use long simulations.
5th Order Modulator
Final Parameter Values

Input range ~ ±1V

±2.5V

Stable input range with margin ~ ±1V

Summary

- Oversampled ADCs decouple SQNR from circuit complexity and accuracy
- If a 1-Bit DAC is used, the converter is to 1st order, inherently linear—indeed of component matching
- Typically, used for high resolution & low frequency applications – e.g. digital audio
- 2nd order $\Sigma\Delta$ used extensively due to lower levels of limit cycle related spurious tones compared to 1st order

- $\Sigma\Delta$ modulators of order greater than 2:
  - Cascaded (multi-stage) modulators
  - Single-loop, single-quantizer modulators with multi-order filtering in the forward path
Bandpass $\Delta\Sigma$ Modulator

- Replace the integrator in 1st order lowpass $\Sigma\Delta$ with a resonator
- $\Rightarrow$ 2nd order bandpass $\Sigma\Delta$

**Key Point:**

- NTF $\rightarrow$ notch type shape
- STF $\rightarrow$ bandpass shape

Ref:
Paolo Cusinato, et. al, “A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range”, IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001
Bandpass $\Sigma\Delta$ Characteristics

- Oversampling ratio defined as $f_s / 2B$ where $B$ = signal bandwidth

- Typically, sampling frequency is chosen to be $f_s = 4f_{\text{center}}$ where $f_{\text{center}}$ = bandpass filter center frequency

- STF has a bandpass shape while NTF has a notch shape

- To achieve same resolution as lowpass, need twice as many integrators

Bandpass $\Sigma\Delta$ Modulator Dynamic Range
As a Function of Modulator Order ($K$)

- Bandpass $\Sigma\Delta$ resolution for order $K$ is the same as lowpass $\Sigma\Delta$ resolution with order $L = K/2$
Example: Sixth-Order Bandpass $\Sigma\Delta$ Modulator


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**Example: Sixth-Order Bandpass $\Sigma\Delta$ Modulator**

**Features & Measured Performance**

- Analog input full-scale: 4.4V (differential)
- Sampling frequency ($f_s$): 42.8MHz
- Center frequency ($f_0$): 10.7MHz
- Signal bandwidth ($B$): 200kHz
- OSR: 107
- Dynamic range: 74dB (200kHz band)
  - 88dB (9kHz band)
- Peak SNDR: 61dB
- IMD (0-15dB): 71dBc
- Active die area: 1mm²
- Power supply: 3.3V
- Power consumption: 76mW (adaptive biasing)
  - 126mW (standard biasing)
- Technology: 0.35μm CMOS

Modulator Front-End Testing

• Should make provisions for testing the modulator (AFE) separate from the decimator (digital back-end)
• Data acquisition board used to collect 1-bit digital output at $f_s$ rate
• Analyze data in a PC environment or dedicated test equipment in manufacturing environments can be used
• Need to run DFT on the collected data and also make provisions to perform the function of digital decimation filter in software
• Typically, at this stage, parts of the design phase behavioral modeling effort can be utilized
• Good testing strategy vital for debugging/improving challenging designs

Summary
Oversampled ADCs

• Noise shaping utilized to reduce baseband quantization noise power
• Reduced precision requirement for analog building blocks compared to Nyquist rate converters
• Relaxed transition band requirements for analog anti-aliasing filters
• Utilizes low cost, low power digital filtering
• Speed is traded for resolution
• Typically used for lower frequency applications compared to Nyquist rate ADCs
Material Covered in EE247

• Filters
  – Continuous-time filters
    • Biquads & ladder type filters
    • Opamp-RC, Opamp-MOSFET-C, gm-C filters
  – Automatic frequency tuning
  – Switched capacitor (SC) filters

• Data Converters
  – D/A converter architectures
  – A/D converter
    • Nyquist rate ADC- Flash, Interpolating & Folding, Pipeline ADCs,…..
    • Self-calibration techniques
    • Oversampled converters

Acknowledgements

• The course notes for EE247 are based on numerous sources including:
  – Prof. P. Gray’s EE290 course
  – Prof. B. Boser’s EE247 course notes
  – Prof. B. Murmann’s Nyquist ADC notes
  – Fall 2004 & ‘05 & ‘06 EE247 class feedback
  – Last but not least, Fall 2007 EE247 class
    • The instructor would like to thank the class of 2007 for their enthusiastic & active participation!
Systems Including Analog-Digital Interface Circuitry
(Not Included in Final Exam)

- Wireline communications
  - Telephone related (DSL, ISDN, CODEC)
  - Television circuitry (Cable modems, TV tuners…)
  - Ethernet (10/1Gigabit, 10/100BaseT…)
- Wireless
  - Cellular telephone (CDMA, Analog, GSM….)
  - Wireless LAN (Blue tooth, 802.11a/b/g…..)
  - Radio (analog & digital), Television
- Disk drives
- Fiber-optic systems

E.E. Circuit Course
vs. Frequency Range

- RF Band
- IF Band
- Baseband

AM Radio 10.7MHz 80MHz 100MHz
FM Radio 100MHz
Cellular Phone

EE240, EE247

EE242
Data Transmission Over Existing Twisted-Pair Phone Lines

- Data transmitted over existing phone lines covering distances close to 3.5 miles
  - Voice-band MODEMs (up to 56Kb/s)
  - ISDN (160Kb/s)
  - HDSL, SDSL, .......
  - ADSL (up to 8Mb/s)
Data Transmission Over Twisted-Pair Phone Lines

ISDN (U-Interface) Transceiver

- Full duplex transmission (RX & TX signals sent simultaneously)
- 160kbit/sec baseband data (80kHz signal bandwidth)
- Standardized line code 2B1Q (4 level code 3:1:-1:-3)
- Max. desired loop coverage 18kft (~36dB signal attenuation)
- Final required BER (bit-error-rate) $10^{-7}$ \(\Rightarrow\) (min. SNDR=27dB)

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ISDN (U-Interface) Transceiver

Echo Problem

- Transformer coupling to line
  - For a perfectly matched system \(\Rightarrow\) no leakage of TX signal into RX path
  - Unfortunately, system has poor matching + complicating factor of bridged-taps

---
ISDN (U-Interface) Transceiver
Echo Problem

- System full duplex transmission $\rightarrow$ RX & TX signals sent simultaneous (& at the same frequency band)
  - Leakage of TX signal to RX path (echo)
  - Worst case $\rightarrow$ echo could be 30dB higher compared to the received signal!!

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ISDN (U-Interface) Transceiver
Echo Cancellation

- Echo cancellation performed in the digital domain
  - Typically echo cancellation performed by transversal adaptive digital filter
  - Any non-linearity incurred by the analog circuitry makes echo canceller significantly more complex
  - Desirable to have high linearity analog circuitry (75dB range)
Simplified Transceiver Block Diagram

CMA → Control, maintenance & access unit
DFE → Decision feedback equalizer
DEC → Decimation filter
REC → Reconstruction filter
LEC & NEC → Linear/non-linear echo-canceler


Analog Front-End

To avoid stringent requirements for non-linear echo canceler:
→ high linearity analog circuitry needed (~ 75dB)
Data Transmission Over Twisted-Pair Phone Lines

DSL (Digital Subscriber Loop)

- HDSL & SDSL more like ISDN @ higher frequencies
  - Full duplex transmission with RX & TX signals on the same frequency band

Data Transmission Over Twisted-Pair Phone Lines

ADSL (Asymmetric Digital Subscriber Loop)

- In USA mostly ADSL \( \rightarrow \) FDM (frequency division multiplex)
  - Signal from CO to customer on a different band compared to customer to CO
    - Echo cancellation can be performed by simple filtering
  - Data rates up to 8Mbps (much higher compared to ISDN)
ADSL Signal Characteristics

• Main difference compared to ISDN: TX & RX signals on different frequency bands
  – Downstream (fast, from CO to customer) 138kHz to 1.1MHz
  – Upstream (slow, from customer to CO) 30kHz to 138kHz
    • Echo cancellation much easier
• More severe signal attenuation at high frequencies (1MHz DSL v.s. 80kHz ISDN)

![Signal Characteristics Diagram]

Typical ADSL Analog Front-End

• ADC 16/14b with 14bit linearity, pipeline with auto. calibration @ 5Ms/s
• DAC 16/14b with 14bit linearity, with auto. calibration
• On-chip filters 3rd to 4th order LPF with $f_c$ 1.1MHz for downstream and 138kHz upstream (typically continuous-time type filters with on-chip frequency tuning)

Typical ADSL Analog Front-End

- Note: Band selection filters are off-chip due to stringent noise requirements (3nV/√Hz)
  - Discrete LC type

Wireless Communication Circuits
Wireless Circuits

- Differ from wired comm. circuits
  - Includes RF circuitry+IF circuitry+baseband circuits (three different frequency ranges)
  - Signal scenarios in wireless receivers more challenging
  - Requirement for received signal BER in the order of $10^{-3}$ for voice-only→(min. SNR~9dB)
Superheterodyne Receiver

- One or more intermediate frequency (IF)
- Periodic signal at a frequency equal to the desired RX signal + or – IF frequency is provided by a Local Oscillator
- RX signal is frequency shifted to a fixed frequency (IF filter center frequency)

RF Superheterodyne Receiver

Example: CDMA Receiver

- Received frequency is mixed down to a fixed IF frequency and then filtered with a bandpass filter
Why Image Reject Filter?

- Any signal at the image frequency of the RX signal with respect to Osc. frequency will fall on the desired RX signal and cause impairment.

Why Image Reject Filter?

- Image reject filter attenuates signals out of the RX band.
- Typically, image reject filters are ceramic or LC type filters.
Quadrature Downconversion

- In systems with phase or freq. modulation, since signal is not symmetric around $f_{IF}$, directly converting down to baseband corrupts the sidebands.
  - Quadrature downconversion overcomes this problem.

Effect of Adjacent Channels

- Adjacent channels can be as much as 60dB higher compared to the desired RX signal!
- Linearity of stages prior and including channel selection filters extremely important.
Effect of Adjacent Channels

- Due to existence of large unwanted signals & limited dynamic range for the front-end circuitry:
  - Can not amplify the signal up front due to linearity issues
  - Need to allocate amplification/filtering numbers to RX blocks carefully
  - Can only amplify when unwanted signals are filtered adequately
  - System design critical with respect to tradeoffs affecting:
    - Gain
    - Linearity
    - Power dissipation
    - Chip area

Homodyne (Direct to Baseband) Receivers

- No intermediate frequency, signal mixed directly down to baseband
- Almost all of the filtering performed at baseband
  - Higher levels of integration possible
  - Issue to be aware of:
    - Requirements for the baseband filters more stringent
    - Since the local oscillator frequency is exactly at the same freq. as the RX signal freq. → can cause major DC offsets & drive the receiver front-end into non-linear region
Example: Wireless LAN 802.11b & Bluetooth


Digital IF Receiver
(IF sampling)

* IF signal is converted to digital → most of signal processing performed in the digital domain
* Performance requirement for ADC more demanding in terms of noise, linearity, and dynamic range!
* With advancements of ADCs could be the architecture of choice in the future
Typical Wireless Transmitter

- Transmit signal shipped from DSP to the analog front-end in the form of I& Q signals
- Signal converted to analog form by D/A
- Lowpass filter provides signal shaping
- In-phase & Quad. Components combined and then mixed up to RF
- Power amplifier amplifies and provides the low-impedance output

Analog Filters in Super-Heterodyne Wireless Transceivers

<table>
<thead>
<tr>
<th>Filters</th>
<th>Function</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Filter</td>
<td>Image Rejection</td>
<td>Ceramic or LC</td>
</tr>
<tr>
<td>IF Filter</td>
<td>Channel selection</td>
<td>SAW</td>
</tr>
<tr>
<td>Base-band Filters</td>
<td>Channel Selection &amp; Anti-aliasing for ADC</td>
<td>Integrated Cont.-Time or S.C.</td>
</tr>
</tbody>
</table>
Example: Dual Mode CDMA (IS95) & Analog Cellular Phone

- Baseband analog circuitry includes:
  - CDMA
    - 4bit flash type ADC clock rate 10MHz
    - 8bit segmented TX DAC clock rate 10MHz (shared with FM)
    - 7th order elliptic RX lowpass filter corner freq. 650kHz
    - 3rd order chebyshev TX lowpass filter corner freq. 650kHz
  - FM (analog)
    - 8bit successive approximation ADCs clock rate 360kHz
    - 5th order chebyshev RX lowpass filter corner frequency 14kHz
    - 3rd order butterworth TX lowpass filter corner frequency 27kHz
Summary

• Examples of systems utilizing challenging analog to digital interface circuitry- in the area of wireline & wireless systems discussed

• Analog circuits still remain the interface → connecting the digital world to the real world!