

EE247 Reader Nyquist Rate Data Converters

Books

R. v. d. Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, 2nd ed., Kluwer, 2003

B. Razavi, *Data Conversion System Design*, IEEE Press, 1995.

Publications

1. W. R. Bennett, "Spectra of quantized signals," *Bell Syst. Tech. J.*, vol. 27, pp. 446-72, July 1988.
2. B. Widrow, "A study of rough amplitude quantization by means of Nyquist sampling theory," *IRE Trans. Circuit Theory*, vol. CT-3, pp. 266-76, 1956.
3. "Understanding Data Converters," Texas Instruments Application Report SLAA013, Mixed-Signal Products, 1995.
4. M. V. Bossche, J. Schoukens, and J. Renneboog, "Dynamic Testing and Diagnostics of A/D Converters," *IEEE Transactions on Circuits and Systems*, vol. CAS-33, no. 8, Aug. 1986.
5. B. Ginetti and P. Jespers, "Reliability of Code Density Test for High Resolution ADCs," *Electron. Lett.*, vol. 27, pp. 2231-3, Nov. 1991.
6. Analog Devices Application Note 586: "LVDS Data Outputs for High Speed ADCs"
7. W. Yang et al., "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. of Solid-State Circuits*, Dec. 2001
8. M. Pelgrom, "A 10-b 50-MHz CMOS D/A Converter with 75-W Buffer," *JSSC*, Dec. 1990, pp. 1347.
9. C. Conroy et al, "Statistical Design Techniques for D/A Converters," *JSSC* Aug. 1989, pp. 1118-28.
10. Kuboki, S.; Kato, K.; Miyakawa, N.; Matsubara, K. Nonlinearity analysis of resistor string A/D converters. *IEEE Transactions on Circuits and Systems*, vol.CAS-29, (no.6), June 1982. p.383-9.
11. D. W. J. Groeneveld, H. J. Schouwenaars, H. A. H. Termeer, and C. A. A. Bastiaansen, "A self-calibration technique for monolithic high-resolution D/A

converters," IEEE Journal of Solid-State Circuits, vol. 24, pp. 1517 - 1522, December 1989.

12. R. J. Van De Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters," IEEE Journal of Solid-State Circuits, vol. 11, pp. 795 - 800, December 1976.

13. D.A. Johns, K. Martin "Analog Integrated Circuits" Wiley, 1997, p.606

14. A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

15. M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Techn. Papers, pp. 314.

16. L. A. BIENSTMAN et al, " An Eight-Channel 8 13it Microprocessor Compatible NMOS D/A Converter with Programmable Scaling", IEEE JSSC, VOL. SC-15, NO. 6, DECEMBER 1980

17. S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

18. I. E. Opris, "Bootstrapped pad protection structure," IEEE J.Solid-State Circuits, pp. 300, Feb. 1998

19. A. Wang, "Recent developments in ESD protection for RF IC," *Proc. DAC Conference*, Jan. 2003

20. W. Yang, *et al.* "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR at Nyquist Input," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001, pp. 1931

21. K. Vleugels et al, "A 2.5-V Sigma-Delta Modulator for Broadband Communications Applications "IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001, pp. 1887

22. R. Yen, *et al.* "A MOS Switched-Capacitor Instrumentation Amplifier," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-17, NO. 6,, DECEMBER 1982 1008

23. H. Ohara, et al., "A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE Journal of Solid-State Circuits*, vol. 22, pp. 930 - 938, December 1987.

24. J.T. Wu, et al., "A 100-MHz pipelined CMOS comparator " IEEE Journal of Solid-State Circuits, vol. 23, pp. 1379 - 1385, December 1988.

25. R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier," *IEEE Journal of Solid-State Circuits*, vol. 13, pp. 499 - 503, August 1978.
26. A. Yukawa, "A CMOS 8-Bit High-Speed A/D Converter IC," *JSSC* June 1985, pp. 775-9.
27. I. Mehr and L. Singer, "A 500-Msample/s, 6-Bit Nyquist-Rate ADC for Disk-Drive Read-Channel Applications," *JSSC* July 1999, pp. 912-20.
28. T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 166 - 172, March 1995.
29. C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," *JSSC* February 1990, pp. 997-1002.
30. C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," *JSSC* August 1996, pp. 1132-40.
31. I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," *JSSC* March 2000, pp. 318-25.
32. T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 166 - 172, March 1995.
33. Y. Akazawa, et al., "A 400MSPS 8b flash AD conversion LSI," *IEEE International Solid-State Circuits Conference*, vol. XXX, pp. 98 - 99, February 1987.
34. T. Wakimoto, et al, "Si bipolar 2GS/s 6b flash A/D conversion LSI," *IEEE International Solid-State Circuits Conference*, vol. XXXI, pp. 232 - 233, February 1988
35. C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," *JSSC* February 1990, pp. 997-1002.
36. C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," *JSSC* August 1996, pp. 1132-40.
37. H. Kimura et al, "A 10-b 300-MHz Interpolated-Parallel A/D Converter," *JSSC* April 1993, pp. 438-446.
38. B. Nauta and G. Venes, *JSSC* Dec 1985, pp. 1302-8
39. Opris et. al., *JSSC* 12/1998
40. Lewis et. al., *JSSC* 3/1992
41. A. N. Karanicolas et al. "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE J. Of Solid-State Circuits*, pp. 1207-15, Dec. 1993

42. B. Razavi and B. A. Wooley, "A 12-b 5-Msample/s two-step CMOS A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 27, pp. 1667 - 1678, December 1992.
43. E. G. Soenen et al., "An architecture and an algorithm for fully digital correction of monolithic pipelined ADCs," *TCAS II*, pp. 143-153, March 1995
44. L. Singer et al., "A 12 b 65 MSample/s CMOS ADC with 82 dB SFDR at 120 MHz," *ISSCC 2000, Digest of Techn. Papers.*, pp. 38-39
45. B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," *ISSCC Dig. Techn. Papers*, pp. 328-329, 2003.
46. A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999
47. D. W. Cline, P.R Gray "A power optimized 13-b 5 MSamples/s pipelined analog-to-digital converter in 1.2um CMOS," *JSSC 3/1996*
48. R.H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Selected Areas Comm.*, April 1999
49. Schreier, "ADCs and DACs: Marching Towards the Antenna," GIRAFE workshop, ISSCC 2003