• Administrative issues
  ▪ Midterm exam postponed to **Tues. Oct. 28th**
    o You can *only* bring one 8x11 paper with your own written notes (please do not photocopy)
    o No books, class or any other kind of handouts/notes, calculators, computers, PDA, cell phones....
    o Midterm includes material covered to end of lecture 14

• D/A converters
  – Static performance of D/As (continued)
    • Systematic & random errors
  – Practical aspects of current-switched DACs
  – Segmented current-switched DACs
  – DAC dynamic non-idealities
  – DAC design considerations
  – Self calibration techniques
    • Current copiers
    • Dynamic element matching
  – DAC reconstruction filter
Summary Last Lecture

D/A converter architectures:
- Resistor string DAC
- Serial charge redistribution DAC
- Parallel charge scaling DAC
- Combination of resistor string (MSB) & binary weighted charge scaling (LSB)
- Current source DAC
  - Unit element
  - Binary weighted

- Static performance
  - Component matching-systematic & random errors
    - Component random variations \( \rightarrow \) Gaussian pdf
    - INL for both unit-element DAC: \( \sigma_{\text{INL}} = \sigma_e \times 2^{(B/2)-1} \)
    - DNL for unit-element: \( \sigma_{\text{DNL}} = \sigma_e \)

DAC INL

\[
\sigma_{\text{INL}}^2 = n \left(1 - \frac{n}{N}\right) \times \sigma_e^2
\]

To find max. variance:
\[
\frac{d\sigma_{\text{INL}}^2}{dn} = 0
\]

\( \rightarrow n = N/2 \rightarrow \sigma_{\text{INL}}^2 = \frac{N}{4} \times \sigma_e^2 \)

- Error is maximum at mid-scale \((N/2)\):
  \[
  \sigma_{\text{INL}} = \frac{1}{2} \sqrt{2^B - 1} \sigma_e
  \]
  with \( N = 2^B - 1 \)

- INL depends on both DAC resolution & element matching \( \sigma_e \)
- While \( \sigma_{\text{DNL}} = \sigma_e \) is to first order independent of DAC resolution and is only a function of element matching

Ref: Kuboki et al., TCAS, 6/1982
Simulation Example

12 Bit converter DNL and INL

\[ \sigma_e = 1\% \]
\[ B = 12 \]

Random # generator used in MatLab

Computed INL:
\[ \sigma_{\text{INL}}^{\text{max}} = 0.32 \text{ LSB (midscale)} \]

Why is the results not as expected per our derivation?

INL & DNL for Binary Weighted DAC

- INL same as for unit element DAC
- DNL depends on transition
  - Example:
    0 to 1 \( \Rightarrow \sigma_{\text{DNL}}^2 = \sigma_{(dV/dI)}^2 \)
    1 to 2 \( \Rightarrow \sigma_{\text{DNL}}^2 = 3\sigma_{(dV/dI)}^2 \)

- Consider MSB transition:
  0111 \( \ldots \) 1000 \( \ldots \)
Example: 4-bit DAC

Digital Input

Analog Output

\[ \begin{align*}
8 & \quad 7 \\
6 & \quad 5 \\
4 & \quad 3 \\
2 & \quad 1 \\
0 & \\
\end{align*} \]

DAC Output [LSB]

Binary Weighted DAC DNL

\[ \begin{align*}
\sigma_{DNL}^2 &= \sigma_{(d \text{ref}/\text{ref})}^2 \\
\sigma_{INL} &= \frac{\sigma_{DNL}}{2} \\
\sigma_{DNL_{\text{max}}} &= 2^{B-1} \sigma_e \\
\sigma_{INL_{\text{max}}} &= \frac{1}{2} \sqrt{2^{B-1} - 1} \sigma_e \\
\end{align*} \]

\[ \begin{align*}
\sigma_e &= 1% \\
\Rightarrow \sigma_{DNL} &= 0.64 \text{ LSB} \\
\sigma_{INL} &= 0.32 \text{ LSB} \\
\end{align*} \]
MOS Current Source Variations
Due to Device Matching Effects

\[ I_d = \frac{I_{d1} + I_{d2}}{2} \]
\[ \frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d} \]
\[ \frac{dI_d}{I_d} = \frac{dW/L}{W/L} + 2dV_{th} \frac{V_{GS} - V_{th}}{V_{th}} \]

- Current matching depends on:
  - Device \( W/L \) ratio matching
    \( \Rightarrow \) Larger device area less mismatch effect
  - Current mismatch due to threshold voltage variations:
    \( \Rightarrow \) Larger gate-overdrive less threshold voltage mismatch effect

Current-Switched DACs in CMOS

\[ \frac{dI_d}{I_d} = \frac{dW}{W} + 2dV_{th} \frac{V_{GS} - V_{th}}{V_{th}} \]

- Advantages:
  Can be very fast
  Reasonable area for resolution < 9-10 bits

- Disadvantages:
  Accuracy depends on device \( W/L \) & \( V_{th} \) matching
Unit Element versus Binary Weighted DAC

Unit Element DAC

\[ \sigma_{DNL} = \sigma_\epsilon \]
\[ \sigma_{INL} \approx \frac{B}{2} - 1 \sigma_\epsilon \]

Binary Weighted DAC

\[ \sigma_{DNL} \approx \frac{2^B}{2} \sigma_\epsilon = 2 \sigma_{INL} \]
\[ \sigma_{INL} \approx \frac{B}{2} - 1 \sigma_\epsilon \]

Number of switched elements:

\[ S = 2^B \]
\[ S = B \]

Key point: Significant difference in performance and complexity!

“Another” Random Run …

DNL and INL of 12 Bit converter

Now (by chance) worst DNL is mid-scale.

Close to statistical result!
10Bit DAC DNL/INL Comparison
Plots: 100 Simulation Runs Overlaid

Ref: C. Lin and K. Bult, "A 10-b, 500-
MSample/s CMOS DAC
in 0.6
mm2," IEEE
Journal of
Solid-State
Circuits, vol.
33, pp. 1948
- 1958,
December 1998.

Note: $\sigma_e=2\%$

10Bit DAC DNL/INL Comparison
Plots: RMS for 100 Simulation Runs

Ref: C. Lin and K. Bult, "A 10-b, 500-
MSample/s CMOS DAC
in 0.6
mm2," IEEE
Journal of
Solid-State
Circuits, vol.
33, pp. 1948
- 1958,
December 1998.

Note: $\sigma_e=2\%$
DAC INL/DNL Summary

- DAC choice of architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
- Results assume uncorrelated random element variations
- Systematic errors and correlations are usually also important and may affect final DAC performance


Unit Element versus Binary Weighted DAC
Example: B=10

<table>
<thead>
<tr>
<th>Unit Element DAC</th>
<th>Binary Weighted DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sigma_{DNL} = \sigma_\varepsilon$</td>
<td>$\sigma_{DNL} \equiv 2^{\frac{B}{2}} \sigma_\varepsilon = 32\sigma_\varepsilon$</td>
</tr>
<tr>
<td>$\sigma_{INL} \equiv 2^{\frac{B}{2}-1} \sigma_\varepsilon = 16\sigma_\varepsilon$</td>
<td>$\sigma_{INL} \equiv 2^{\frac{B}{2}-1} \sigma_\varepsilon = 16\sigma_\varepsilon$</td>
</tr>
</tbody>
</table>

Number of switched elements:

$S = 2^B = 1024$

$S = B = 10$

Significant difference in performance and complexity!
Segmented DAC
Combination of Unit-Element & Binary-Weighted

- **Objective:**
  Compromise between unit-element and binary-weighted DAC

- **Approach:**
  \[ B_1 \text{ MSB bits} \rightarrow \text{unit elements} \]
  \[ B_2 \text{ LSB bits} \rightarrow \text{binary weighted} \]
  \[ B_{\text{Total}} = B_1 + B_2 \]

- **INL:** unaffected same as either architecture
- **DNL:** Worst case occurs when LSB DAC turns off and one more MSB DAC element turns on → Same as binary weighted DAC with \( (B_2+1) \) # of bits
- **Number of switched elements:** \( (2^{B_1}-1) + B_2 \)

#### Comparison

**Example:**
\[ B = 12, \quad B_1 = 5, \quad B_2 = 7 \]
\[ B_1 = 6, \quad B_2 = 6 \]
Assuming: \( \sigma_\varepsilon = 1\% \)

<table>
<thead>
<tr>
<th>DAC Architecture (B1+B2)</th>
<th>( \sigma_{\text{INL}[\text{LSB}]} )</th>
<th>( \sigma_{\text{DNL}[\text{LSB}]} )</th>
<th># of switched elements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit element (12+0)</td>
<td>0.32</td>
<td>0.01</td>
<td>4095</td>
</tr>
<tr>
<td>Segmented (6+6)</td>
<td>0.32</td>
<td>0.113</td>
<td>63+6=69</td>
</tr>
<tr>
<td>Segmented (5+7)</td>
<td>0.32</td>
<td>0.16</td>
<td>31+7=38</td>
</tr>
<tr>
<td>Binary weighted(0+12)</td>
<td>0.32</td>
<td>0.64</td>
<td>12</td>
</tr>
</tbody>
</table>
Practical Aspects
Current-Switched DACs

- Unit element DACs ensure monotonicity by turning on equal-weighted current sources in succession
- Typically current switching performed by differential pairs
- For each diff pair, only one of the devices are on→ switch device mismatch not an issue
- Issue: While binary weighted DAC can use the incoming binary digital word directly, unit element requires a decoder

\[ \rightarrow \text{N to } (2^N-1) \text{ decoder} \]

<table>
<thead>
<tr>
<th>Binary</th>
<th>Thermometer</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>00000000</td>
</tr>
<tr>
<td>001</td>
<td>00000001</td>
</tr>
<tr>
<td>010</td>
<td>00000011</td>
</tr>
<tr>
<td>011</td>
<td>00001111</td>
</tr>
<tr>
<td>100</td>
<td>00111111</td>
</tr>
<tr>
<td>101</td>
<td>01111111</td>
</tr>
<tr>
<td>110</td>
<td>11111111</td>
</tr>
<tr>
<td>111</td>
<td>11111111</td>
</tr>
</tbody>
</table>

Segmented Current-Switched DAC
Example: 8bit→4MSB+4LSB

- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register
Segmented Current-Switched DAC
Cont’d

• 4-bit MSB Unit element DAC + 4-bit binary weighted DAC

• Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder

• Digital code for both DACs stored in a register

Segmented Current-Switched DAC
Cont’d

• MSB Decoder
  ➔ Domino logic
  ➔ Example: D4,5,6,7=1 OUT=1

• Register
  ➔ Latched NAND gate:
  ➔ CTRL=1 OUT=INB
Segmented Current-Switched DAC Reference Current Considerations

- $I_{\text{ref}}$ is referenced to $V_{\text{DD}}$

  → Problem: Reference current varies with supply voltage

\[ I_{\text{ref}} = \frac{(V_{\text{DD}} - V_{\text{ref}})}{R} \]

Segmented Current-Switched DAC Reference Current Considerations

- $I_{\text{ref}}$ is referenced to $V_{\text{SS}} \rightarrow \text{GND}$

\[ I_{\text{ref}} = \frac{(V_{\text{ref}} - V_{\text{SS}})}{R} \]
Segmented Current-Switched DAC Considerations

- Example:
  - 2-bit MSB Unit element DAC & 3-bit binary weighted DAC

- To ensure monotonicity at the MSB→LSB transition: First OFF MSB current source is routed to LSB current generator

DAC Dynamic Non-Idealities

- Finite settling time
  - Linear settling issues: (e.g. RC time constants)
  - Slew limited settling

- Spurious signal coupling
  - Coupling of clock/control signals to the output via switches

- Timing error related glitches
  - Control signal timing skew
Dynamic DAC Error: Timing Glitch

- Consider binary weighted DAC transition 011 → 100
- DAC output depends on timing
- Plot shows situation where the control signals for LSB & MSB
  - LSB/MSBs on time
  - LSB early, MSB late
  - LSB late, MSB early

Glitch Energy

- Glitch energy (worst case) proportional to: \( dt \times 2^{B-1} \)
- \( dt \) → error in timing & \( 2^{B-1} \) associated with half of the switches changing state
- LSB energy proportional to: \( T = 1/f_s \)
- Need \( dt \times 2^{B-1} \ll T \) or \( dt \ll 2^{B-1} T \)

- Examples:

<table>
<thead>
<tr>
<th>( f_s ) [MHz]</th>
<th>B</th>
<th>( dt ) [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12</td>
<td>&lt;&lt; 488</td>
</tr>
<tr>
<td>20</td>
<td>16</td>
<td>&lt;&lt; 1.5</td>
</tr>
<tr>
<td>1000</td>
<td>10</td>
<td>&lt;&lt; 2</td>
</tr>
</tbody>
</table>

→ Timing accuracy for data converters much more critical compared to digital circuitry
DAC Dynamic Errors

- To suppress effect of non-idealities:
  - Retiming of current source control signals
    - Each current source has its own clocked latch incorporated in the current cell
    - Minimization of latch clock skew by careful layout ensuring simultaneous change of bits
  - To minimize control and clock feed through to the output via G-D & G-S of the switches
    - Use of low-swing digital circuitry

DAC Implementation Examples

- Untrimmed segmented

- Current copiers:

- Dynamic element matching:
Two sources of systematic error:
- Finite current source output resistance
- Voltage drop due to finite ground bus resistance
Current-Switched DACs in CMOS

Assumptions:
- $R_x$ small compared to transistor gate-overdrive
- To simplify analysis: Initially, all device currents assumed to be equal to $I$

$V_{GS_{M1}} = V_{GS_{M1}} - 4RI$
$V_{GS_{M2}} = V_{GS_{M2}} - 7RI$
$V_{GS_{M3}} = V_{GS_{M3}} - 9RI$
$V_{GS_{M4}} = V_{GS_{M4}} - 10RI$
$I_2 = k(V_{GS_{M2}} - V_{th})^2$
$I_2 = I_1 \left(1 - \frac{4RI}{V_{GS_{M2}} - V_{th}} \right)^2$

Example: 5 unit element current sources

$\rightarrow$ Desirable to have $g_m$ small
Current-Switched DACs in CMOS
Example: INL of 3-Bit unit element DAC

<table>
<thead>
<tr>
<th>Input</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>INL [LSB]</td>
<td>-0.1</td>
<td>0.1</td>
<td>0.2</td>
<td>0.3</td>
<td>-0.1</td>
<td>0.1</td>
<td>0.2</td>
<td>0.3</td>
</tr>
</tbody>
</table>

 Sequential current source switching
 Symmetrical current source switching

Example: 7 unit element current source DAC- assume \( g_mR = 1/100 \)

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7) \( \rightarrow INL = +0.25\text{LSB} \)
- If switching of current sources symmetrical (4-3-5-2-6-1-7) \( \rightarrow INL = +0.09, -0.058\text{LSB} \) \( \rightarrow INL \) reduced by a factor of 2.6

Current-Switched DACs in CMOS
Example: DNL of 7 unit element DAC

<table>
<thead>
<tr>
<th>Input</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>DNL [LSB]</td>
<td>-0.2</td>
<td>-0.1</td>
<td>0</td>
<td>0.1</td>
<td>0.2</td>
<td>-0.2</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

 Sequential current source switching
 Symmetrical current source switching

Example: 7 unit element current source DAC- assume \( g_mR = 1/100 \)

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7) \( \rightarrow DNL_{\text{max}} = +0.15\text{LSB} \)
- If switching of current sources symmetrical (4-3-5-2-6-1-7) \( \rightarrow DNL_{\text{max}} = +0.15\text{LSB} \) \( \rightarrow DNL \) unchanged
More recent published DAC using symmetrical switching built in 0.35\textmu{}V analog/1.9V digital, area x10 smaller compared to previous example

- Layout of Current sources - each current source made of 4 devices in parallel each located in one of the 4 quadrants
- Thermometer decoder used to convert incoming binary digital control for the 5 MSB bits
- Dummy decoder used on the LSB side to match the latency due to the MSB decoder
• Current source layout
  – MSB current sources layout in the mid sections of the four quad
  – LSB current sources on the periphery
  – Two rows of dummy current sources added at the periphery to create identical environment for devices in the center versus the ones on the outer sections

• Note that each current cell has its clocked latch and clock signal laid out to be close to its switch to ensure simultaneous switching of current sources
• Special attention paid to the final latch to have the cross point of the complementary switch control signal such that the two switches are not both turned off during transition
A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, Student Member, IEEE, Marc A. F. Borremans, Student Member, IEEE, Michel S. J. Steyaert, Senior Member, IEEE, and Willy Sansen, Fellow, IEEE

- Measured DNL/INL with current associated with the current cells as variable

A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. Wouter J. Groeneveld, Hans J. Schouwenaars, Senior Member, IEEE, Henk A. H. ter Meer, and Cornelis A. A. Bastiaanssen

Fig. 2. Calibration principle. (a) Calibration. (b) Operation.
16-bit DAC (6+10)- MSB DAC uses calibrated current sources

---

**Integral Linearity (LSB)**

![Graph showing integral linearity](image)

- $f_n = 1 \text{ kHz}$
- $f_c = 44 \text{ kHz}$
- $B = 20 \text{ kHz}$

---

EECS 247- Lecture 15  Data Converters: DAC Design (continued)  © 2008 H.K.  Page 43
Current Divider Accuracy

\[ I_d = \frac{I_{d1} + I_{d2}}{2} \]
\[ dI_d = \frac{I_{d1} - I_{d2}}{I_d} \]
\[ dI_d = 2 \frac{dI_{d1}}{V_{GS} - V_{th}} + dV_{th} \]

Ideal Current Divider
Real Current Divider
M1 & M2 mismatched

Problem: Device mismatch could severely limit DAC accuracy
Dynamic Element Matching

During $\Phi_1$

\[
I_1^{(1)} = \frac{1}{2} I_o (1 + \Delta I) \\
I_2^{(1)} = \frac{1}{2} I_o (1 - \Delta I)
\]

During $\Phi_2$

\[
I_1^{(2)} = \frac{1}{2} I_o (1 - \Delta I) \\
I_2^{(2)} = \frac{1}{2} I_o (1 + \Delta I)
\]

\[
\langle I_2 \rangle = \frac{I_1^{(1)} + I_2^{(2)}}{2} = \frac{I_o (1 - \Delta I) + (1 + \Delta I)}{2} = \frac{I_o}{2}
\]

Fig. 4. (a) Binary weighted current network with equal switching frequencies. (b) Error analysis results.
Dynamic Element Matching

During $\Phi_1$

$\Delta_{11} = \Delta_{12}$
$\Delta_{21} = \Delta_{22}$
$
\Delta_{11} = \frac{1}{2} I_f(l+\Delta_i) \\
\Delta_{21} = \frac{1}{2} I_f(l-\Delta_i) \\
\Delta_{12} = \frac{1}{2} I_f(l+\Delta_i)(l+\Delta_i) \\
\Delta_{22} = \frac{1}{2} I_f(l-\Delta_i)(l-\Delta_i)$

During $\Phi_2$

$\Delta_{11} = \Delta_{12}$
$\Delta_{21} = \Delta_{22}$
$
\Delta_{11} = \frac{1}{2} I_f(l+\Delta_i) \\
\Delta_{21} = \frac{1}{2} I_f(l-\Delta_i) \\
\Delta_{12} = \frac{1}{2} I_f(l+\Delta_i)(l+\Delta_i) \\
\Delta_{22} = \frac{1}{2} I_f(l-\Delta_i)(l-\Delta_i)$

$\langle I_f \rangle = \frac{I_{11} + I_{12}}{2}$
$\langle I_f \rangle = \frac{I_{21} + I_{22}}{2}$
$\langle I_f \rangle = \frac{I_f (l+\Delta_i)(l+\Delta_i) + I_f (l-\Delta_i)(l-\Delta_i)}{2}$
$\langle I_f \rangle = \frac{I_f (l+\Delta_i\Delta_i)}{4}$

E.g. $\Delta_1 = \Delta_2 = 1\% \rightarrow$ matching error is $(1\%)^2 = 0.01\%$

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 6, DECEMBER 1976

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASCHER

- Bipolar 12-bit DAC using dynamic element matching built in 1976
- Element matching clock frequency 100kHz
- INL <0.25LSB!
Example: State-of-the-Art current steering DAC

<table>
<thead>
<tr>
<th></th>
<th>Max Sample Frequency</th>
<th>GSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>14</td>
<td>Bit</td>
</tr>
<tr>
<td>DNL</td>
<td>+/- 0.8</td>
<td>LSB</td>
</tr>
<tr>
<td>INL</td>
<td>+/- 2.1</td>
<td>LSB</td>
</tr>
<tr>
<td>SFDR @ 1.0 GSPS</td>
<td>&gt; 60</td>
<td>dB</td>
</tr>
<tr>
<td>IMD @ 1.0 GSPS</td>
<td>&gt; 64</td>
<td>dBc</td>
</tr>
<tr>
<td>NSD @ f_{out} = 400MHz</td>
<td>-155</td>
<td>dBm/Hz</td>
</tr>
<tr>
<td>Power (Core) @ 1.4GSPS</td>
<td>200</td>
<td>mW</td>
</tr>
<tr>
<td>Power (Total) @ 1.4GSPS</td>
<td>400</td>
<td>mW</td>
</tr>
<tr>
<td>Area (Core)</td>
<td>0.8</td>
<td>mm²</td>
</tr>
<tr>
<td>Area (Chip)</td>
<td>6.25</td>
<td>mm²</td>
</tr>
</tbody>
</table>

Layout Tree Structures
DAC In the Big Picture

- Learned to build DACs
  - Convert the incoming digital signal to analog
- DAC output → staircase form
- Some applications require filtering (smoothing) of DAC output → reconstruction filter

DAC Reconstruction Filter

- Need for and requirements depend on application
- Tasks:
  - Correct for sinc droop
  - Remove “aliases” (stair-case approximation)
Reconstruction Filter Options

- Digital and SC filter possible only in combination with oversampling (signal bandwidth $B << f_s/2$)
- Digital filter
  - Band limits the input signal to prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band sinc amplitude droop associated with the inherent DAC S/H function

DAC Reconstruction Filter

Example: Voice-Band CODEC Receive Path

Note: $f_{\text{DAC}}^{\text{max}} = 3.4kHz$

$\sin(\pi f_{\text{DAC}}^{\text{max}} x T_s)/(\pi f_{\text{DAC}}^{\text{max}} x T_s)$

$\Rightarrow -2.75 \text{ dB droop due to DAC sinc shape}$

Summary
D/A Converter

• D/A architecture
  – Unit element – complexity proportional to $2^B$, excellent DNL
  – Binary weighted – complexity proportional to B, poor DNL
  – Segmented – unit element MSB($B_1$)+ binary weighted LSB($B_2$)
    → Complexity proportional ($(2^{B_1}-1) + B_2$) -DNL compromise between the two

• Static performance
  – Component matching

• Dynamic performance
  – Time constants, Glitches

• DAC improvement techniques
  – Symmetrical switching rather than sequential switching
  – Current source self calibration
  – Dynamic element matching

• Depending on the application, reconstruction filter may be needed

What Next?

• ADC Converters:
  – Need to build circuits that "sample"
  – Need to build circuits for amplitude quantization

Analog Input

Anti-Aliasing
Filter

Sampling
+Quantization

"Bits to Staircase"

Reconstruction
Filter

Analog Output
Analog-to-Digital Converters

• Two categories:
  – Nyquist rate ADCs $\Rightarrow f_{\text{sig\ max}} \sim 0.5 f_{\text{sampling}}$
    • Maximum achievable signal bandwidth higher compared to oversampled type
    • Resolution limited to max. 12-14 bits
  – Oversampled ADCs $\Rightarrow f_{\text{sig\ max}} \ll 0.5 f_{\text{sampling}}$
    • Maximum achievable signal bandwidth significantly lower compared to nyquist
    • Maximum achievable resolution high (18 to 20 bits!)