ADC Converters

Comparator design

- Single-stage open-loop amplifier
- Cascade of open-loop amplifiers
- Problem associated with DC offset
  - Cascaded output series cancellation
  - Input series cancellation
  - Offset cancellation through additional input pair plus offset storage capacitors
- Latched comparators
- Comparator examples

Voltage Comparators

Electrical schematic

Play an important role in majority of ADCs
Function: Compare the instantaneous value of two analog signals & generate a digital output voltage based on the sign of the difference:

\[
\begin{align*}
\text{If } V_{i+} - V_{i-} > 0 & \Rightarrow V_{\text{out}} = \text{“1”} \\
\text{If } V_{i+} - V_{i-} < 0 & \Rightarrow V_{\text{out}} = \text{“0”}
\end{align*}
\]
Voltage Comparator Architectures

Comparator architectures:

• High gain amplifier with differential analog input & single-ended large swing output
  – Output swing has to be compatible with driving digital logic circuits
  – Open-loop amplification → no frequency compensation required
  – Precise gain not required

• Latched comparators; in response to a strobe (clock edge), input stage disabled & digital output stored in a latch till next strobe
  – Two options for implementation:
    • Latch-only comparator
    • Low-gain preamplifier + high-sensitivity latch

• Sampled-data comparators
  – T/H input
  – Offset cancellation

Comparator Built with High-Gain Amplifier

Amplify $V_{in\text{ min}}$ to $V_{DD}$
$\Rightarrow V_{in\text{ min}}$ determined by ADC resolution

Example: 12-bit ADC with:
- $V_{FS}=1.5V \Rightarrow 1\text{LSB}=0.36mV$
- $V_{DD}=1.8V$

$\Rightarrow$ For 1.8V output & 0.5LSB precision:

$$A_{\text{gain}} = \frac{1.8V}{0.18mV} = 10,000$$
Comparators
1-Single-Stage Amplification

• Amplifier maximum Gain-Bandwidth product \( f_u \) for a given technology, typically a function of maximum device \( f_t \).

\[ f_u = \text{unity-gain frequency}, \quad f_u = -3 \text{dB frequency} \quad f_u = \frac{f_u}{A_v} \]

Example: \( f_u = 10 \text{GHz} \) & \( A_v = 10,000 \)

\[ f_o = \frac{10 \text{GHz}}{10,000} = 1 \text{MHz} \]

\[ \tau_{\text{settling}} = \frac{1}{2\pi f_o} = 0.16 \mu \text{sec} \]

Allow a few \( \tau \) for output to settle

\[ f_{\text{Clock}} \rightarrow \frac{1}{5\tau_{\text{settling}}} = 1.26 \text{MHz} \]

\[ \tau_{\text{settling}} = \pi \tau_{\text{settling}} = \approx \]

\[ f_u = 0.1-10 \text{GHz} \]

Too slow for majority of applications!

→ Try cascade of lower gain stages to broaden frequency of operation

Comparators
2- Cascade of Open Loop Amplifiers

The stages identical \( \rightarrow \) small-signal model for the cascades:

One stage:

\[ |A_v(0)| = g_m R_L \]

\[ \omega_b = -3 \text{dB frequency} = \frac{1}{R_L C_T} \]

\[ \omega_u = -\text{unity gain frequency} = G \times \text{BW} = \frac{g_m}{C_T} \]

\[ \therefore \omega_u = \frac{\omega_u}{|A_v(0)|} \]
Open Loop Cascade of Amplifiers

For an N-stage cascade:

\[ A_T(\omega) = (A_T(\omega))_N = \frac{(A_T(\omega))_N}{1 + \frac{1}{\omega_0}} \]

Define

\[ \omega_{\text{in}} = -3\text{dB frequency of the N-stage cascade} \]

Then

\[ |A_T(\omega_{\text{in}})| = \frac{|A_T(\omega)|_N}{2} \]

and

\[ \omega_{\text{in}} = \sqrt{\frac{2}{N-1}} \cdot \frac{\omega_0}{|A_T(\omega)|_N} \]

Thus,

\[ \frac{\omega_{\text{in}}}{\omega_0} = \left( \frac{\omega_0}{|A_T(\omega)|_N} \right)^{1/N} \cdot \frac{1}{\sqrt{2^{1/N} - 1}} \]

Example: N=4, A_T=10000 \( \Rightarrow \omega_{\text{in}} = 430 \omega_0 \)

Open Loop Cascade of Amplifiers

Example:

| N | \omega_{\text{in}}/\omega_0 | |A_T(\omega)| |
|---|-----------------|----------------|
| 1 | 10,000          | 10,000         |
| 2 | 64              | 100            |
| 3 | 236             | 21.5           |
| 4 | 435             | 10             |
| 5 | 611             | 6.3            |
| 10| 1067            | 2.5            |
| 20| 1185            | 1.6            |

For \(|A_T(\omega)|=10,000\)

Example:

\[ N=3, \quad f_u = 10\text{GHz} \quad \& \quad |A_T(0)| = 10000 \]

\[ f_0N = \frac{10\text{GHz}}{(10,000)^{1/3}} = 237\text{MHz} \]

\[ \tau_{\text{setting}} = \frac{1}{2\pi f_0} = 0.7\text{ns} \]

Allow a few \(\tau\) for output to settle

\[ f_{\text{Max, Clock}} \rightarrow \frac{1}{5\tau_{\text{setting}}} = 290\text{MHz} \]

\(f_{\text{Max}}\) improved from 1.26MHz to 290MHz \(\Rightarrow X236\)
Open Loop Cascade of Amplifiers
Offset Voltage

- From offset point of view: high gain/stage is preferred

- Choice of # of stage → bandwidth vs offset tradeoff

\[ A_T = A_1 \cdot A_2 \cdot A_3 \]

Input-referred offset → \[ V_{os} = V_{os1} + \frac{V_{os2}}{A_1} + \frac{V_{os3}}{A_1 \cdot A_2} \]

Open Loop Cascade of Amplifiers
Step Response

- Assuming linear behavior (not slew limited)

\[ v_{o1} = \frac{1}{C} \int_0^t g_m v_{in} dt = \frac{g_m}{C} v_{in} t \]

\[ v_{o2} = \frac{1}{C} \int_0^t g_m v_{o1} dt = \frac{g_m}{C} \int_0^t g_m v_{in} dt = \frac{1}{2} \left( \frac{g_m}{C} \right)^2 v_{in} t^2 \]

\[ v_{o3} = \frac{1}{C} \int_0^t g_m v_{o2} dt = \frac{g_m}{C} \int_0^t \left( \frac{1}{2} \left( \frac{g_m}{C} \right)^2 v_{in} t^2 \right) dt \]

\[ = \frac{1}{3} \left( \frac{1}{2} \left( \frac{g_m}{C} \right)^3 \right) v_{in} t^3 \]
Open Loop Cascade of Amplifiers

Step Response

- Assuming linear behavior

\[ \text{Delay} = \frac{C}{g_m} \left( N! \left( \frac{V_{out}}{V_{in}} \right)^{1/N} \right) \]

For the output to reach a specified \( V_{out} \) (i.e., \( V_{oh} = V_{out} \)) the delay is

\[ \tau_D = \frac{C}{g_m} \left( N! \left( \frac{V_{out}}{V_{in}} \right)^{1/N} \right) \]

### Delay/(C/gm)

<table>
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<th>10K</th>
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<td>13.2</td>
</tr>
</tbody>
</table>

### Out/Min

- Minimum total delay broad function of \( N \)
- Relationship between # of stages resulting in minimize delay \( (N_{op}) \) and gain \( (V_{out}/V_{in}) \) approximately:

\[ N_{opt} = 1 + \log_2 A_T \quad \text{for} \quad A < 1000 \]

\[ N_{opt} = 1.2 \ln A_T \quad \text{for} \quad A \geq 1000 \]

Offset Cancellation

• In sampled-data cascade of amplifiers Vos can be cancelled
  → Store on ac-coupling caps in series with amp stages

• Offset associated with a specific amp can be cancelled by
  storing it in series with either the input or the output of that
  stage

• Offset can be cancelled by adding a pair of auxiliary inputs
  to the amplifier and storing the offset on capacitors
  connected to the aux. inputs during offset cancellation
  phase


Offset Cancellation
Output Series Cancellation

• Amp modeled as ideal
  + Vos (input referred)

1- Store offset:
  • S1, S4 → open
  • S2, S3 → closed
  → VC = AxVos

Offset Cancellation
Output Series Cancellation

2- Amplify:
- S2, S3 → open
- S1, S4 → closed
  → V_C = A \times V_{OS}

Circuit requirements:
- Amp not saturate during offset storage
- High-impedance (C) load → C_c not discharged
- C_c >> C_{switch} to avoid attenuation
- C_c >> C_L to avoid excessive offset due to charge injection

Offset Cancellation
Cascaded Output Series Cancellation

Note: Offset storage capacitors in series with the amplifier outputs
Offset Cancellation
Cascaded Output Series Cancellation

1- S1 open, S2,3,4,5 closed

\[ V_{C1} = A_1 x V_{os1} \]
\[ V_{C2} = A_2 x V_{os2} \]
\[ V_{C3} = A_1 x V_{os3} \]

2- S3 open first
- Feedthrough from S3 offset on X
- Switch offset, \( \epsilon_3 \) induced on node X
- Since S4 remains closed, offset associated with \( \epsilon_3 \) stored on C2

\[ V_x = \epsilon_3 \]
\[ V_{C1} = A_1 x V_{os1} - \epsilon_3 \]
\[ V_{C2} = A_2 x (V_{os2} + \epsilon_3) \]
3- $S_4 \rightarrow$ open
- Feedthrough from $S_4$ → offset on $Y$
- Switch offset, $\varepsilon_4$ induces error on node $Y$
- Since $S_5$ remains closed, offset associated with $\varepsilon_4$ → stored on $C_3$

$$V_Y = \varepsilon_4$$
$$V_{C2} = A_2x(V_{os2} + \varepsilon_3) - \varepsilon_4$$
$$V_{C3} = A_3x(V_{os3} + \varepsilon_4)$$

4- $S_2 \rightarrow$ open, $S_5 \rightarrow$ open, $S_1 \rightarrow$ closed
- $S_2$ open & $S_1$ closed → since input connected to low impedance source charge injection not of major concern
- Switch offset, $\varepsilon_5$ introduced due to $S_5$ opening

$$V_X = A_1x(V_{in}+V_{os1}) - V_{C1}$$
$$= A_1x(V_{in}+V_{os1}) - (A_1\cdot V_{os1} - \varepsilon_3)$$
$$= A_1\cdot V_{in} + \varepsilon_3$$
Offset Cancellation
Cascaded Output Series Cancellation

\[ V_y = A_2(x_{V} + V_{os2}) - V_{c2} \]
\[ = A_2(x(A_1V_{in} + \varepsilon_3 + V_{os2})) - [A_2(V_{os2} + \varepsilon_3) - \varepsilon_4] \]
\[ = A_1A_2.V_{in} + \varepsilon_4 \]

\[ V_{out} = A_3(x_{V} + V_{os3}) - V_{c3} \]
\[ = A_3(A_2xA_1V_{in} + \varepsilon_4 + V_{os3}) - [A_3(V_{os3} + \varepsilon_4) - \varepsilon_5] \]
\[ = A_1A_2A_3.V_{in} + \varepsilon_5 \]

Example:
3-stage open-loop differential amplifier with series offset cancellation + output amplifier (see Ref.)

\[ A_{Total}(DC) = 2 \times 10^6 = 126\text{dB} \]
\[ \text{Input-referred offset} < 5\mu V \]

Offset Cancellation
Output Series Cancellation

• Advantages:
  – Almost complete cancellation
  – Closed-loop stability not required

• Disadvantages:
  – Gain per stage must be small
  – Offset storage C in the signal path → could slow down overall performance

Offset Cancellation
Input Series Cancellation

1- Store offset

\[ S1 = 0 \text{ (off)} \]
\[ S2, S3 = 1 \text{ (conducting)} \]

\[ V_C = -A(V_C - V_{os}) = \left( \frac{A}{A + 1} \right) V_{os} \]

Note: Mandates closed-loop stability


Offset Cancellation
Input Series Cancellation

2- Amplify

\[ S2, S3 \rightarrow \text{open} \]
\[ S1 \rightarrow \text{closed} \]

\[ V_{out} = -A(V_{in} + V_C - V_{os}) = -A[V_{in} + V_{os}(\frac{A}{A + 1} - 1)] \]

\[ V_{out} = -A(V_{in} - \frac{V_{os}}{A + 1}) \]

Example: A=4
\[ \rightarrow \text{Input-referred offset} = V_{os}/5 \]

Input-Refereed Offset = \[ \frac{V_{os}}{A + 1} \]
Offset Cancellation
Cascaded Input Series Cancellation

\[ V_{\text{out}} = A_1 A_2 \left[ V_{\text{in}} + \frac{V_{\text{off2}}}{A_1 (A_2 + 1) A_3} \right] \]

Input-Reflected Offset = \[ \frac{V_{\text{off2}}}{A_1 (A_2 + 1) A_3} \]

\[ \varepsilon_2 \rightarrow \text{charge injection associated with opening of S4} \]

• Advantages:
  – In applications such as C-array successive approximation ADCs can use C-array to store offset

• Disadvantages:
  – Cancellation not complete
  – Requires closed loop stability
  – Offset storage C in the signal path- could slow down overall performance
CMOS Comparators
Cascade of Gain Stages

Fully differential gain stages → 1st order cancellation of switch feedthrough offset

1- Output series offset cancellation

2- Input series offset cancellation

3- Combined input & output series offset cancellation

$V_{0x1}$ & $V_{0x2}$ are both stored on a single pair of coupling capacitors
Offset Cancellation

- Cancel offset by additional pair of inputs + offset storage Cs + an extra clock phase for offset storage (Lecture 18 slide 46-48)

Latched Comparators

Compares two input voltages at time $t_x$ & generates a digital output:

- If $V_{i+} - V_{i-} > 0 \Rightarrow V_{out} = "1"$
- If $V_{i+} - V_{i-} < 0 \Rightarrow V_{out} = "0"$
CMOS Latched Comparators

Comparator amplification need not be linear
→ can use a latch → regeneration

Latch → Amplification + positive feedback

Simplest Form of CMOS Latch
CMOS Latched Comparators
Small Signal Model

Latch can be modeled as a:
→ Single-pole amp + positive feedback

Small signal ac half circuit

Latched Comparator Latch Delay

\[ g_a V = \frac{V}{R_L} + C \frac{dV}{dt} \]
\[ g_a \left( 1 - \frac{1}{g_m R_L} \right) V = \frac{dV}{dt} \]
\[ g_a \left( 1 - \frac{1}{g_m R_L} \right) dt = \frac{dV}{V} \]

Integrating both sides:
\[ \frac{g_a}{C} \left( 1 - \frac{1}{g_m R_L} \right) \int_{t_i}^{t} dt = \int_{V_i}^{V} \frac{1}{V} dV \]
\[ \left( \int_{x_i}^{x} \frac{1}{x} dx = \ln x \right) \Rightarrow \ln a - \ln b = \ln \frac{a}{b} \]

Latch Delay:
\[ t_b = t_i - t_i = \frac{C}{g_a} \left( \frac{1}{g_m R_L} \right) \ln \left( \frac{V_o}{V_i} \right) \]

For \( g_m R_L \gg 1 \)

\[ t_b = \frac{C}{g_a} \ln \left( \frac{V_o}{V_i} \right) \]
CMOS Latched Comparators

\[
\tau_D = \frac{C}{g_m} \ln \left( \frac{V_T}{V_i} \right)
\]

\[
\frac{V_T}{V_i} \rightarrow \text{Latch Gain} = A_L
\]

\[
\Rightarrow \tau_D = \frac{C}{g_m} \ln A_L
\]

\[\tau_D(\text{3-stage amp}) = 18.2 \frac{C}{g_m}\]

Normalized Latch Delay

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<th>AL</th>
<th>(\frac{\tau_D}{C/g_m})</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>2.3</td>
</tr>
<tr>
<td>100</td>
<td>4.6</td>
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<td>1000</td>
<td>6.9</td>
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<td>10K</td>
<td>9.2</td>
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</table>

Compared to a 3-stage open-loop cascade of amps for equal overall gain of 1000
\(\Rightarrow\) Latch faster by about \(x3\)

Latch-Only Comparator

- Much faster compared to cascade of open-loop amplifiers
- Main problem associated with latch-only comparator topology:
  - High input-referred offset voltage (as high as 100mV!)
- Solution:
  - Use preamplifier to amplify the signal and reduce overall input-referred offset
Pre-Amplifier + Latch
Overall Input-Referred Offset

Latch offset attenuated by preamp gain when referred to preamp input.
Assuming the two offset sources are uncorrelated:

\[ \sigma_{\text{Input-Referred Offsets}} = \sqrt{\sigma_{\text{Vos Preamp}}^2 + \frac{1}{A_{\text{Preamp}}} \sigma_{\text{Vos Latch}}^2} \]

Example:
\[ \sigma_{\text{Vos Preamp}} = 4mV \] & \[ \sigma_{\text{Vos Latch}} = 50mV \] & \[ A_{\text{Preamp}} = 10 \]

\[ \sigma_{\text{Input-Referred Offsets}} = \sqrt{4^2 + \frac{1}{10} 50^2} = 6.4mV \]

Pre-Amplifier Tradeoffs

- Example:
  - Latch offset: 50 to 100mV
  - Preamp DC gain: 10X
  - Preamp input-referred latch offset: 50 to 100mV
  - Input-referred preamplifier offset: 2 to 10mV
  - Overall input-referred offset: 5.5 to 14mV

⇒ Addition of preamp reduces the latch input-referred offset reduced by ~7 to 9X ⇒ allows extra 3-bit resolution for ADC!
Comparator Preamplifier Gain-Speed Tradeoffs

- Amplifier maximum Gain-Bandwidth product ($f_u$) for a given technology, typically a function of maximum device $f_t$

\[ f_u = \text{unity gain frequency}, \quad f_0 = -3 \text{dB frequency} \quad \text{&} \quad \tau_0 = \text{settling time} \]

\[ f_0 = \frac{f_u}{A_{\text{preamp}}} \]

For example assuming preamp has a gain of 10:

\[ f_0 = \frac{1 \text{GHz}}{10} = 100 \text{MHz} \]

\[ \tau_0 = \frac{1}{2\pi f_0} = \frac{A_{\text{preamp}}}{2\pi f_u} = 1.6\pi \text{sec} \]

- Tradeoff:
  - To reduce the effect of latch offset $\rightarrow$ high preamp gain desirable
  - Fast comparator $\rightarrow$ low preamp gain
  - Choice of preamp gain: compromise speed v.s. input-referred latch offset

Latched Comparator

Important features:
- Maximum clock rate $f_s$ settling time, slew rate, small signal bandwidth
- Resolution $\rightarrow$ gain, offset
- Overdrive recovery
- Input capacitance (and linearity of input capacitance)
- Power dissipation
- Input common-mode range and CMR
- Kickback noise
- ...
Comparator Overdrive Recovery

Linear model for a single-pole amplifier:

During reset amplifier settles exponentially to its zero input condition with $t_0 = RC$

Assume $V_m$ → maximum input normalized to $1/2\text{LSB}$ (=1)

Example: Worst case input/output waveforms

Previous input $\rightarrow$ max. possible e.g. VFS
Current input $\rightarrow$ min. input-referred signal (0.5LSB)

Comparators Overdrive Recovery

- If recovery time is not long enough to allow output to discharge (recover) from previous state- then it may not be able to resolve the current input $\rightarrow$ error
- To minimize this effect:
  1. Passive clamp
  2. Active restore
  3. Low gain/stage
Comparators Overdrive Recovery
Limiting Output Voltage

Clamp
Adds parasitic capacitance

Active Restore
After outputs are latched by following stage
→ Activate $\phi_R$ & equalize output nodes

CMOS Preamplifier + Latched Comparator
Delay in Response

Latch delay previously found:

$$\tau_D = \frac{C}{g_m} \ln \left( \frac{V_2}{V_1} \right)$$

Assuming gain of $A_i$ for the preamplifier then : $V_i = A_i \times V_{in}$

$$\tau_D = \frac{C}{g_m} \ln \left( \frac{V_0}{A_i V_{in}} \right)$$
Latched Comparator Including Preamplifier Example

Preamplifier gain:

\[ A_p = \frac{g_{m1}}{g_{m2}} = \left( \frac{V_{G5}^{M3} - V_{G5}^{M1}}{V_{G5}^{M2} - V_{G5}^{M1}} \right) \]

Comparator delay:

(for simplicity, preamp delay ignored)

\[ \tau_0 = C \ln \left( \frac{V_0}{A F_{in}} \right) \]

Comparator Dynamic Behavior

\( V_{OUT} \)

\( CLK \)

Comparator Reset

Comparator Decision

\( T_{CLK} \)

\( \tau_{delay} \)
Comparator Resolution

\[ \Delta t = \left(\frac{g_m}{C}\right) \ln\left(\frac{V_{in1}}{V_{in2}}\right) \]

Comparator Voltage Transfer Function

Non-Idealities

- Comparator offset voltage
- Meta-Stable region (output ambiguous)

\[ V_{offset} \rightarrow \text{Comparator offset voltage} \]
\[ \epsilon \rightarrow \text{Meta-Stable region (output ambiguous)} \]
CMOS Comparator Example

- Flash ADC: 8 bits, ±1/2 LSB INL @ fs=15 MHz (Vref=3.8 V, LSB=15 mV)
- No offset cancellation


Comparator with Auto-Zero

Note:
Reference & input both differential

Flash ADC Comparator with Auto-Zero

\[ V_{C_1} - V_{C_2} = (V_{ref_1} - V_{ref_2}) - V_{offset} \]


Substituting for \( V_{C_1} - V_{C_2} \) from previous cycle:

\[ V = A_{h1} \cdot A_{h2} [(V_{in_1} - V_{in_2}) - (V_{ref_1} - V_{ref_2}) - V_{offset}] \]

Note: Offset is cancelled & difference between input & reference established

Flash ADC
Using Comparator with Auto-Zero


Auto-Zero Implementation

Comparator Example

- Variation on Yukawa latch used w/o preamp
- Good for low resolution ADCs (in this case 1.5bit/stage for a pipeline)
- Note: M1, M2, M11, M12 operate in triode mode
- M11 & M12 added to vary comparator threshold
- Conductance at node X is sum of $G_{M1}$ & $G_{M11}$


Comparator Example (continued)

- M1, M2, M11, M12 operate in triode mode with all having equal $L$
- Conductance of input devices:

\[
\begin{align*}
G_1 & = \frac{\mu_{Cox}}{L} \left[ W_2 (V_{T1} - V_{Th}) + W_1 (V_R - V_{Th}) \right] \\
G_2 & = \frac{\mu_{Cox}}{L} \left[ W_2 (V_{T2} - V_{Th}) + W_2 (V_R - V_{Th}) \right] \\
\Delta G & = \frac{\mu_{Cox} W_2}{L} \left( V_{Th} - V_{R} - V_{R} \right)
\end{align*}
\]

- To 1st order, for $W_1 = W_2$ & $W_11 = W_12$

\[
V_{Th} = \frac{W_11}{W_1} \times V_x
\]

where $V_x = V_{Th} - V_{Th}$.

\[ V_x \text{ fixed, } W11, W12 \text{ varied from comparator to comparator} \iff \text{Eliminates need for resistive divider} \]

Comparator Example

- Used in a pipelined ADC with digital correction
- Differential reference & input
- M7, M8 operate in triode region
- Preamp gain ~10
- Input buffers suppress kick-back
  - $\phi_1$ high $\rightarrow$ C_n charged to VR & $\phi_2$ is also high $\rightarrow$ current diverted to latch $\rightarrow$ comparator output in hold mode
  - $\phi_2$ high $\rightarrow$ C_n connected to S/Hout & comparator input (VR-S/Hout), current sent to preamp $\rightarrow$ comparator in amplify mode


Bipolar Comparator Example

- Used in 8bit 400Ms/s & 6bit 2Gb/s flash ADC
- Signal amplification during $\phi_1$ high, latch operates when $\phi_1$ low
- Input buffers suppress kick-back & input current
- Separate ground and supply buses for front-end preamp $\rightarrow$ kick-back noise reduction