EE247
Lecture 4

• Active ladder type filters
  – For simplicity, will start with all pole ladder type filters
    • Convert to integrator based form- example shown
  – Then will attend to high order ladder type filters incorporating zeros
    • Implement the same 7th order elliptic filter in the form of ladder RLC with zeros
      – Find level of sensitivity to component mismatch
      – Compare with cascade of biquads
    • Convert to integrator based form utilizing SFG techniques
  – Effect of integrator non-Idealities on filter frequency characteristics

RLC Ladder Filters
Example: 5th Order Lowpass Filter

• Made of resistors, inductors, and capacitors
• Doubly terminated or singly terminated (with or w/o \( R_L \))

Doubly terminated LC ladder filters \(\rightarrow\) Lowest sensitivity to component mismatch
LC Ladder Filters

• First step in the design process is to find values for Ls and Cs based on specifications:
  – Filter graphs & tables found in:
  – CAD tools
    • Matlab
    • Spice

LC Ladder Filter Design Example

Design a LPF with maximally flat passband:

- $f_{-3dB} = 10$MHz, $f_{stop} = 20$MHz
- $R_s > 27$dB @ $f_{stop}$

• Maximally flat passband $\rightarrow$ Butterworth

  • Find minimum filter order
  • Here standard graphs from filter books are used

  $f_{stop} / f_{-3dB} = 2$

  $R_s > 27$dB

Minimum Filter Order $\Rightarrow$ 5th order Butterworth

From: Williams and Taylor, p. 2-37
## LC Ladder Filter Design Example

### Find values for L & C from Table:

- Normalized values:
  - $C_1_{\text{Norm}} = C_5_{\text{Norm}} = 0.618$
  - $C_3_{\text{Norm}} = 2.0$
  - $L_2_{\text{Norm}} = L_4_{\text{Norm}} = 1.618$

### Denormalization:

- Since $\omega_{-3dB} = 2\pi \times 10 \text{MHz}$
  - $L_r = R/\omega_{-3dB}$
  - $C_r = 1/(RX\omega_{-3dB})$

**R** is the value of the source and termination resistor (choose both 1Ω for now)

Then: $L = L_r \times L_{\text{Norm}}$

$C = C_r \times C_{\text{Norm}}$

From: Williams and Taylor, p. 11.3

Last Lecture:
Example: 5th Order Butterworth Filter

Specifications:
\( f_{-3dB} = 10\text{MHz} \),
\( f_{\text{stop}} = 20\text{MHz} \),
\( R_s > 27\text{dB} \)

Used filter tables to obtain \( L_s \) & \( C_s \)

SPICE simulation Results

Low-Pass RLC Ladder Filter
Conversion to Integrator Based Active Filter

- To convert RLC ladder prototype to integrator based filer:
  - Use Signal Flowgraph technique
    - Name currents and voltages for all components
    - Use KCL & KVL to derive equations
    - Make sure reactive elements expressed as \( 1/s \) term
    - \( V(C) = f(I) \) & \( I(L) = f(V) \)
    - Use state-space description to derive the SFG
    - Modify & simply the SFG for implementation with integrators e.g. convert all current nodes to voltage
Conversion to Integrator Based Active Filter

\[
\begin{align*}
V_1 &= V_{in} - V_2, & V_2 &= \frac{I_2}{sC_1}, & V_3 &= V_2 - V_4, \\
V_4 &= \frac{I_4}{sC_3}, & V_5 &= V_4 - V_6, & V_6 &= \frac{I_6}{sC_5}, & V_o &= V_6, \\
I_1 &= \frac{V_1}{R_s}, & I_3 &= I_1 - I_3, & I_3 &= \frac{I_3}{sL_2}, \\
I_4 &= I_3 - I_5, & I_5 &= \frac{I_5}{sL_4}, & I_6 &= I_5 - I_7, & I_7 &= \frac{V_6}{R_L}.
\end{align*}
\]
Low-Pass RLC Ladder Filter

Signal Flowgraph

SFG

Low-Pass RLC Ladder Filter

Normalize
Low-Pass RLC Ladder Filter

Synthesize

\[
\begin{align*}
V_{in} & \quad V_1 \quad -1 \quad V_2 \quad 1 \quad V_3 \quad -1 \quad V_4 \quad 1 \quad V_5 \quad -1 \quad V_6 \quad 1 \quad V_o \\
\frac{R^*}{R_s} \quad \frac{1}{sC_1R} \quad \frac{R^*}{sL_2} \quad \frac{1}{sC_3R} \quad \frac{R^*}{sL_4} \quad \frac{1}{sC_5R} \quad R^* \quad R_L
\end{align*}
\]

\[
\begin{align*}
V_{in} &= \frac{R^*}{R_s} \\
V_1 &\quad V_2 \quad V_3 \quad V_4 \quad V_5 \quad V_6 \quad V_o
\end{align*}
\]

\[
\begin{align*}
\tau_1 &= \frac{C_1R^*}{} \\
\tau_2 &= \frac{L_2}{R^*} = \frac{C_2R^*}{} \\
\tau_3 &= \frac{C_3R^*}{} \\
\tau_4 &= \frac{L_4}{R^*} = \frac{C_4R^*}{} \\
\tau_5 &= \frac{C_5R^*}{}
\end{align*}
\]

Main building block: Integrator
Let us start to build the filter with RC& Opamp type integrator

Integrator Based Implementation
Opamp-RC Integrator

### Single-Ended

\[ V_o = -V_{i1} \times \frac{1}{sR_1C_1} - V_{i2} \times \frac{1}{sR_2C_1} \]

### Differential

\[ V_{o+} - V_{o-} = (V_{i1+} - V_{i1-}) \times \frac{1}{sR_1C_1} \\
+ (V_{i2+} - V_{i2-}) \times \frac{1}{sR_2C_1} \]

Note: Implementation with single-ended integrator requires extra circuitry for sign inversion whereas in differential case both signal polarities are available.

---

Differential Integrator Based LP Ladder Filter

**Synthesize**

- First iteration:
  - All resistors are chosen = 1Ω
  - Values for \( \tau = R \times C \) found from RLC analysis
  - Capacitors: \( C1 = 9.836nF \), \( C2 = 25.45nF \), \( C3 = 31.83nF \)
Simulated Magnitude Response

Scale Node Voltages

To maximize dynamic range
scale node voltages

Scale $V_o$ by factor “s”
Differential Integrator Based LP Ladder Filter

Node Scaling

• Second iteration:
  - Nodes scaled, note output node x2
  - Resistor values scaled according to scaling of nodes
  - Capacitors the same: $C_1 = C_5 = 9.836\, \text{nF}$, $C_2 = C_4 = 25.45\, \text{nF}$, $C_3 = 31.83\, \text{nF}$

Maximizing Signal Handling by Node Voltage Scaling

Before Node Scaling

After Node Scaling

Scale $V_o$ by factor “s”
Filter Noise

Total noise @ the output:
1.4 \mu \text{V rms}
(noiseless opamps)

That's excellent, but:
• Capacitors too large
  for integration
  \rightarrow large Si area
  • Resistors too small
  \rightarrow high power
dissipation

Typical applications allow
higher noise, assuming
tolerable noise in the
order of 140 \mu \text{V rms} \ldots

Scale to Meet Noise Target

Scale capacitors and resistors
to meet noise objective

\[ s = 10^{-4} \rightarrow (V_{n1}/V_{n2})^2 \]

Noise after scaling: 141 \mu \text{V rms} (noiseless opamps)
Differential Integrator Based LP Ladder Filter
Final Design

• Final iteration:
  • Based on scaled nodes and noise considerations
  • Capacitors: $C_1=C_5=0.9836\,\text{pF}$, $C_2=C_4=2.545\,\text{pF}$, $C_3=3.183\,\text{pF}$
  • Resistors: $R_1=11.77\,\text{K}$, $R_2=9.677\,\text{K}$, $R_3=10\,\text{K}$, $R_4=12.82\,\text{K}$, $R_5=8.493\,\text{K}$, $R_6=11.93\,\text{K}$, $R_7=7.8\,\text{K}$, $R_8=10.75\,\text{K}$, $R_9=8.381\,\text{K}$, $R_{11}=10\,\text{K}$, $R_{11}=9.306\,\text{K}$

RLC Ladder Filters
Including Transmission Zeros

• All poles
• Poles & Zeros
RLC Ladder Filter Design Example

• Design a baseband filter for CDMA IS95 cellular phone receive path with the following specs.
  – Filter frequency mask shown on the next page
  – Allow enough margin for manufacturing variations
    • Assume overall tolerable pass-band magnitude variation of 1.8dB
    • Assume the -3dB frequency can vary by +/-8% due to manufacturing tolerances & circuit inaccuracies
  – Assume any phase impairment can be compensated in the digital domain

* Note this is the same example as for cascade of biquad while the specifications are given closer to a real product case

RLC Ladder Filter Design Example
CDMA IS95 Receive Filter Frequency Mask
RLC Ladder Filter Design
Example: CDMA IS95 Receive Filter

- Since phase impairment can be corrected for, use filter type with max. roll-off slope/pole
  → Filter type → Elliptic
- Design filter freq. response to fall well within the freq. mask
  - Allow margin for component variations & mismatches
- For the passband ripple, allow enough margin for ripple change due to component & temperature variations
  → Design nominal passband ripple of 0.2dB
- For stopband rejection add a few dB margin 44+5=49dB
- Final design specifications:
  - \( f_{\text{pass}} = 650 \text{ kHz} \) \( R_{\text{pass}} = 0.2 \text{ dB} \)
  - \( f_{\text{stop}} = 750 \text{ kHz} \) \( R_{\text{stop}} = 49 \text{ dB} \)
- Use Matlab or filter tables to decide the min. order for the filter (same as cascaded biquad example)
  - 7th Order Elliptic

RLC Low-Pass Ladder Filter Design
Example: CDMA IS95 Receive Filter

- Use filter tables & charts to determine LC values
RLC Ladder Filter Design
Example: CDMA IS95 Receive Filter

• Specifications
  – $f_{\text{pass}} = 650$ kHz  $R_{\text{pass}} = 0.2$ dB
  – $f_{\text{stop}} = 750$ kHz  $R_{\text{stop}} = 49$ dB
• Use filter tables to determine LC values
  – Elliptic filters tabulated wrt “reflection coefficient $\rho$”

$$R_{\text{pass}} = 10 \times \log \left(1 - \rho^2\right)$$

  – Since $R_{\text{pass}} = 0.2$ dB $\Rightarrow \rho = 20\%$
  – Use table accordingly

• Table from Zverev book page #281 & 282:
  • Since our spec. is $A_{\text{min}} = 44$ dB
    add 5dB margin & design for $A_{\text{min}} = 49$ dB
Table from Zverev page #281 & 282:

- Normalized component values:
  
  - C1 = 1.17677
  - C2 = 0.19393
  - L2 = 1.19467
  - C3 = 1.51134
  - C4 = 1.01098
  - L4 = 0.72398
  - C5 = 1.27776
  - C6 = 0.71211
  - L6 = 0.80165
  - C7 = 0.83597

RLC Filter Frequency Response

- Component values denormalized
- Frequency response simulated
- Frequency mask superimposed
- Frequency response well within spec.
**Frequency Response Passband Detail**

- Passband well within spec.
- Make sure enough margin is allowed for variations due to process & temperature

**RLC Ladder Filter Sensitivity**

- The design has the same specifications as the previous example implemented with cascaded biquads

- To compare the sensitivity of RLC ladder versus cascaded-biquads:
  - Changed all Ls &Cs one by one by 2% in order to change the pole/zeros by 1% (similar test as for cascaded biquad)
  - Found frequency response most sensitive to L4 variations
  - Note that by varying L4 both poles & zeros are varied
Component mismatch in RLC filter:
- Increase L4 from its nominal value by 2%
- Decrease L4 by 2%
Sensitivity of Cascade of Biquads

Component mismatch in Biquad 4 (highest Q pole):
- Increase $\omega_{p4}$ by 1%
- Decrease $\omega_{z4}$ by 1%

High Q poles $\Rightarrow$ High sensitivity in Biquad realizations

Sensitivity Comparison for Cascaded-Biquads versus RLC Ladder

- 7th Order elliptic filter
  - 1% change in pole & zero pair

<table>
<thead>
<tr>
<th></th>
<th>Cascaded Biquad</th>
<th>RLC Ladder</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passband deviation</td>
<td>2.2dB (29%)</td>
<td>0.2dB (2%)</td>
</tr>
<tr>
<td>Stopband deviation</td>
<td>3dB (40%)</td>
<td>1.7dB (21%)</td>
</tr>
</tbody>
</table>

Doubly terminated LC ladder filters $\Rightarrow$ Significantly lower sensitivity compared to cascaded-biquads particularly within the passband
RLC Ladder Filter Design
Example: CDMA IS95 Receive Filter

- Previously learned to design integrator based ladder filters without transmission zeros
  - Question:
    - How do we implement the transmission zeros in the integrator-based version?
    - Preferred method → no extra power dissipation → no extra active elements

Integrator Based Ladder Filters
How Do to Implement Transmission zeros?

- Use KCL & KVL to derive:
  \[ I_2 = I_1 - I_3 - I_{C_a}, \quad I_{C_a} = (V_2 - V_4)sC_a, \quad V_2 = \frac{I_2}{sC_1}, \quad V_2 = \frac{I_1 - I_3 - I_{C_a}}{sC_1} \]

Substituting for \( I_{C_a} \) and rearranging:

\[
V_2 = \frac{I_1 - I_3}{s(C_1 + C_a)} + V_4 \times \frac{C_a}{C_1 + C_a}
\]
Integrator Based Ladder Filters
How Do to Implement Transmission zeros?

- Use KCL & KVL to derive:
  \[ V_2 = \frac{I_1 - I_3}{s(C_1 + C_a)} + V_4 \times \frac{C_a}{C_1 + C_a} \]
  - Frequency independent constants
  - Can be substituted by:
    Voltage-Controlled Voltage Source

\[ V_4 = \frac{I_3 - I_5}{s(C_3 + C_a)} + V_2 \times \frac{C_a}{C_3 + C_a} \]

- Replace shunt capacitors with voltage controlled voltage sources:

\[
\begin{align*}
V_2 &= \frac{I_1 - I_3}{s(C_1 + C_a)} + V_4 \times \frac{C_a}{C_1 + C_a} \\
V_4 &= \frac{I_3 - I_5}{s(C_3 + C_a)} + V_2 \times \frac{C_a}{C_3 + C_a}
\end{align*}
\]

Exact same expressions as with \( C_a \) present
3rd Order Lowpass Filter
All Poles & No Zeros

\[ V_{in} \quad I_1 \quad V_1 \quad -I_2 \quad V_2 \quad +V_3 \quad -I_3 \quad V_3 \quad -I_4 \quad V_4 \quad I_5 \quad V_o \]

\[ \frac{1}{Rs} \quad \frac{1}{sC_1} \quad \frac{1}{sL_2} \quad \frac{1}{sC_3} \quad \frac{1}{RL} \]

Implementation of Zeros in Active Ladder Filters
Without Use of Active Elements

\[ V_{in} \quad I_1 \quad V_1 \quad -I_2 \quad V_2 \quad +V_3 \quad -I_3 \quad V_3 \quad -I_4 \quad V_4 \quad I_5 \quad V_o \]

\[ \frac{1}{Rs} \quad \frac{1}{s(C_1+C_a)} \quad \frac{1}{sC_1} \quad \frac{1}{sL_2} \quad \frac{1}{s(C_3+C_a)} \quad \frac{1}{RL} \]
Integrator Based Ladder Filters

Higher Order Transmission zeros

Convert zero generating Cs in C loops to voltage-controlled voltage sources
Example:

**5th Order Chebyshev II Filter**

- 5th order Chebyshev II
- Table from: Williams & Taylor book, p. 11.112
- 50dB stopband attenuation
- \( f_{-3dB} = 10MHz \)

**Transmission Zero Generation Opamp-RC Integrator**

\[
V_o = -\frac{I}{s(C+C_x)} \left[ \frac{V_{in1}}{R_1} + \frac{V_{in2}}{R_2} + \frac{V_o}{R_f} \right]
\]

\[V_{in3} \times \frac{C_x}{C+C_x}\]
Differential Integrator Based LP Ladder Filter
Final Design 5th Order All-Pole
Differential 5th Order Chebychev Lowpass Filter

- All resistors 1Ω
- Capacitors: $C_1=36.11\text{nF}$, $C_2=14.05\text{nF}$, $C_3=12.15\text{nF}$, $C_4=5.344\text{nF}$, $C_5=2.439\text{nF}$
- Coupling capacitors: $C_a=1.36\text{nF}$, $C_b=1.36\text{nF}$, $C_c=1.31\text{nF}$, $C_d=1.31\text{nF}$

5th Order Chebyshev II Filter

Simulated Frequency Response
7th Order Differential Lowpass Filter
Including Transmission Zeros

Transmission zeros implemented with pair of coupling capacitors

Effect of Integrator Non-Idealities on Filter Frequency Characteristics

• In the passive filter design (RLC filters) section:
  – Reactive element (L & C) non-idealities $\rightarrow$ expressed in the form of Quality Factor (Q)
  – Filter impairments due to component non-idealities explained in terms of component Q

• In the context of active filter design (integrator-based filters)
  – Integrator non-idealities $\rightarrow$ Translates to the form of Quality Factor (Q)
  – Filter impairments due to integrator non-idealities explained in terms of integrator Q
Effect of Integrator Non-Idealities on Filter Performance

- Ideal integrator characteristics

- Real integrator characteristics:
  - Effect of opamp finite DC gain
  - Effect of integrator non-dominant poles

**Ideal Integrator**

\[ V_{in} \rightarrow \text{Ideal Intg.} \rightarrow V_o \]

*Ideal Integrator:*

- DC gain = \( \infty \)
- Single pole @ DC
- \( \rightarrow \) no non-dominant poles

\[ H(s) = \frac{-\omega_b}{s} \]

\( \omega_b = 1 / RC \)
Ideal Integrator Quality Factor

Ideal intg. transfer function:

$$H(s) = \frac{-\omega_0}{s} \frac{-\omega_0}{j\omega} = -\frac{1}{j\omega}$$

Since component Q is defined as:

$$H(j\omega) = \frac{1}{R(\omega) + jX(\omega)}$$

$$Q = \frac{X(\omega)}{R(\omega)}$$

Then:

$$Q_{\text{ideal}} = \infty$$

Real Integrator Non-Idealities

$$H(s) = \frac{-a}{s}$$

$$H(s) = \frac{-a}{(1 + \frac{s}{a})(1 + \frac{s}{p_2})(1 + \frac{s}{p_3})...}$$
Effect of Integrator Finite DC Gain on Q

Example: $a=100 \rightarrow P1/\omega_0 = 1/100$

\[ \text{Phase error } \approx 0.5 \text{ degree} \]

Effect of Integrator Finite DC Gain on Q

Example: Lowpass Filter

- Finite opamp DC gain
- Phase lead @ $\omega_0$
- Droop in the passband
Effect of Integrator Non-Dominant Poles

Example: $\omega_0/\omega_p = 1/100$

$\Rightarrow$ phase error $\equiv -0.5^\circ$

Effect of Integrator Non-Dominant Poles

Example: Lowpass Filter

- Additional poles due to opamp poles:
  - Phase lag @ $\omega_0$
  - Peaking in the passband
- In extreme cases could result in oscillation!
Effect of Integrator Non-Dominant Poles & Finite DC Gain on Q

Note that the two terms have different signs
→ Can cancel each other’s effect!

Integrator Quality Factor

Real intg. transfer function: 

\[
H(s) = \frac{-a}{(1 + s \frac{a}{a_0})(1 + \frac{s}{p_2})(1 + \frac{s}{p_3})\ldots}
\]

Based on the definition of Q and assuming that:

\[
\frac{a_0}{p_{2,3,\ldots}} << 1 \quad \text{&} \quad a >> 1
\]

It can be shown that in the vicinity of unity-gain-frequency:
Example:
Effect of Integrator Finite Q on Bandpass Filter Behavior

Integrator DC gain = 100

Example:
Effect of Integrator Q on Filter Behavior

Integrator DC gain = 100 & P2 @ 100. ω_o
Summary
Effect of Integrator Non-Idealities on Q

$Q_{\text{ideal}}^\text{intg} = \infty$

$Q_{\text{real}}^\text{intg} = \frac{1}{\frac{1}{a} - \omega_2 \sum_{n=2}^{\infty} \frac{1}{p_n}}$

- Amplifier finite DC gain reduces the overall Q in the same manner as series/parallel resistance associated with passive elements.
- Amplifier poles located above integrator unity-gain frequency enhance the Q!
  - If non-dominant poles close to unity-gain freq. $\rightarrow$ Oscillation
- Depending on the location of unity-gain-frequency, the two terms can cancel each other out!