EE247
Lecture 10

• Switched-capacitor filters
  – Effect of non-idealities (continued)
  – Switched-capacitor filters utilizing double sampling technique

• Data converters
  – Areas of application
  – Data converter transfer characteristics
  – Sampling, aliasing, reconstruction
  – Amplitude quantization

Effect of Opamp Nonidealities on Switched Capacitor Filter Behaviour

• Opamp finite gain
• Opamp finite bandwidth
• Sources of distortion
  – Finite slew rate of the opamp
  – Non-linearity associated with opamp output/input characteristics
  – Capacitor non-linearity- usually insignificant, similar to cont. time filters
  – Charge injection & clock feedthrough (will be covered in the oversampling data converter section)
Effect of Opamp Non-Idealities

Finite DC Gain

\[ H(s) = - f_s \frac{C_s}{C_I} \frac{1}{s + f_s \frac{C_s}{C_I} \frac{L}{a}} \]

\[ H(s) = \frac{-a b}{s + a b \times \frac{1}{a}} \]

\[ \Rightarrow Q_{ntg} = a \]

- Finite DC gain same effect in S.C. filters as for C.T. filters
- If DC gain not high enough → lowing of overall Q & droop in passband

Effect of Opamp Non-Idealities

Finite Opamp Bandwidth

\[ H_{\text{actual}}(Z) = H_{\text{ideal}}(Z) \left[ 1 - e^{-k} + e^{-k} \frac{C_1}{C_1 + C_s} z^{-1} \right] \]

where \( k = \pi \times \frac{C_1}{C_1 + C_s} \frac{f_t}{f_s} \)

\( f_t \rightarrow \text{Opamp unity-gain-frequency} \), \( f_s \rightarrow \text{Clock frequency} \)


Opamp Bandwidth Requirements for Switched-Capacitor Filters Compared to Continuous-Time Filters

- Finite opamp bandwidth causes phase lag at the unity-gain frequency of the integrator for both type filters
  - \( \rightarrow \) Results in negative intg. Q & thus increases overall Q and gain @ results in peaking in the passband of interest

- For given filter requirements, opamp bandwidth requirements much less stringent for S.C. filters compared to cont. time filters
  - \( \rightarrow \) Lower power dissipation for S.C. filters (at low freq.s only due to other effects)

- Finite opamp bandwidth causes down shifting of critical frequencies in both type filters
  - Since cont. time filters are usually tuned \( \rightarrow \) tuning accounts for frequency deviation
  - S.C. filters are untuned and thus frequency shift could cause problems specially for narrow-band filters
Effect of Opamp Nonidealities on Switched Capacitor Filter Behaviour

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What is Slewing?

Assumption:
Integrator opamp is a simple class A transconductance type differential pair with fixed tail current, \( I_{ss}=\text{const} \).
What is Slewing?

$|V_{Cs}| > V_{max}$ → Output current constant $I_o = \text{Iss}/2$ or $-\text{Iss}/2$
→ Constant current charging/discharging $C_I$: $V_o$ ramps down/up → Slewing

After $V_{Cs}$ is discharged enough to have:

$|V_{Cs}| < V_{max}$ → $I_o = g_m V_{Cs}$ → Output → Exponential or over-shoot settling

Distortion Induced by Opamp Finite Slew Rate

Vo

Output Voltage

Slewing

Settling

Settling (multi-pole)

Time

Multiple pole settling

One pole settling
Ideal Switched-Capacitor Output Waveform

\[ \Phi_1, \Phi_2 \]
\[ \text{Vin, Vo, Vcs, Clock} \]
\[ \text{Charge transferred from Cs to C1} \]

Slew Limited Switched-Capacitor Integrator

Output Slewing & Settling

\[ \Phi_1, \Phi_2 \]
\[ \text{Vo-ideal, Vo-real} \]
\[ \text{Slewing, Linear Settling} \]
Distortion Induced by Finite Slew Rate of the Opamp

- Error due to exponential settling changes linearly with signal amplitude.
- Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error).

For high-linearity need to have either high slew rate or non-slewing opamp.

\[ HD_k = \frac{V_o}{S_f T_s} \frac{8(\sin \frac{a_0 T_s}{2})^2}{\pi k (k^2 - 4)} \]

\[ HD_3 = HD_k f_0 >> f_s \approx \frac{8a V_o f_s^2}{75 S f_s} \]

Distortion Induced by Opamp Finite Slew Rate

Example:
Slew Related Harmonic Distortion

\[ HD_3 = \frac{V_o}{S_r T_s} \left( \frac{sin \left( \frac{\omega T_s}{2} \right)}{15 \pi} \right)^8 \]

\[ HD_3 = \frac{8\pi V_o}{15 S_r} \left( \frac{f_s}{f} \right)^2 \]

Switched-capacitor filter with 4kHz bandwidth, \( f_s = 128kHz \), \( S_r = 1V/\mu sec \), \( V_o = 3V \)


Distortion Induced by Opamp Finite Slew Rate

Example
Distortion Induced by Finite Slew Rate of the Opamp

• Note that for a high order switched capacitor filter → only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  → Can reduce slew limited non-linearities by using an amplifier with a higher slew rate only for the last stage
  → Can reduce slew limited non-linearities by using class A/B amplifiers
    • Even though the output/input characteristics is non-linear as long as the DC open-loop gain is high, the significantly higher slew rate compared to class A amplifiers helps improve slew rate induced distortion in S.C. filters

• In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) → no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time

More Realistic Switched-Capacitor Circuit Slew Scenario

At the instant $C_i$ connects to input of opamp ($t=0^+$)
→ Opamp not yet active at $t=0^+$ due to finite opamp bandwidth → delay
→ Feedforward path from input to output generates a voltage spike at the output with polarity opposite to final $V_o$ step- spike magnitude function of $C_p$, $C_L$, $C_s$
→ Spike increases slewing period
→ Eventually, opamp becomes active - starts slewing followed by subsequent settling
Switched-Capacitor Circuit

Opamp not Active @ \( t=0^+ \)

\[ \text{Charge sharing: } C_I V_{CI}^{0^+} = V_{CI}^{0^+} (C_i + C_{eq}) \]
\[ \text{where } C_{eq} = \frac{C_I C_L}{C_I + C_L} \]

\[ \Delta V_{out}^{0^+} = V_{CI}^{0^+} \frac{C_I}{C_i + C_L} \approx V_{CI}^{0^-} \frac{C_i}{C_i + C_{eq}} \times \frac{C_I}{C_I + C_L} \]

Assuming \( C_L << C_i << C_I \) → \( C_{eq} = C_L \) → \( C_I V_{CI}^{0^+} = V_{CI}^{0^+} (C_i + C_L) \) → \( V_{CI}^{0^+} = V_{CI}^{0^+} \)
→ \( \Delta V_{out}^{0^+} = V_{CI}^{0^+} \frac{C_I}{C_i + C_L} \times \frac{C_i}{C_i + C_L} = V_{CI}^{0^+} \)

Note that \( \Delta V_{final}^{0^+} = \frac{C_I V_{CI}^{0^+}}{C_I} = \frac{C_i V_{CI}^{0^+}}{C_i} \)

More Realistic Switched-Capacitor Circuit Slew Scenario

Notice that if \( C_i \) is large → some of the charge stored on \( C_s \) is lost prior to opamp becoming effective → operation loses accuracy

\[ \text{Charge sharing: } C_s V_{Cs}^{0^+} = V_{Cs}^{0^+} (C_s + C_{eq}) \]
\[ \text{where } C_{eq} = \frac{C_I C_L}{C_I + C_L} \]

\[ V_{Cs}^{0^+} = V_{Cs}^{0^-} \frac{C_s}{C_s + C_{eq}} = V_{Cs}^{0^-} \frac{C_s C_I C_L}{C_s + C_{eq} C_I + C_L} \]

→ Partly responsible for S.C. filters only good for low-frequency applications
More Realistic S.C. Slew Scenario

Vo_ideal

Vo_real

Slewing Linear Settling Slewing Linear Settling

Vo_real Including t=0+ spike

Slewing Linear Settling

Spike generated at t=0+


Sources of Noise in Switched-Capacitor Filters

• Opamp Noise
  – Thermal noise
  – 1/f (flicker) noise

• Thermal noise associated with the switching process (kT/C)
  – Same as continuous-time filters

• Precaution regarding aliasing of noise required
Extending the Maximum Achievable Critical Frequency of Switched-Capacitor Filters

Consider a switched-capacitor resonator:

Regular sampling:
Each opamp is busy settling only during one of the two clock phases
\[ \rightarrow \text{Idle during the other clock phase} \]

Note: During $\phi_1$ both opamps are idle

Switched-Capacitor Resonator Using Double-Sampling

Double-sampling:
• 2nd set of switches & sampling caps added to all integrators

• While one set of switches/caps sampling the other set transfers charge into the intg. cap

• Opamps busy during both clock phases

• Effective sampling freq. twice the clock freq. while opamp bandwidth requirement remains the same
Double-Sampling Issues

Issues to be aware of:
- Jitter in the clock
- Unequal clock phases
- Mismatch in sampling caps.

$\rightarrow$ Results in parasitic passbands


Double-Sampled Fully Differential S.C. 6th Order All-Pole Bandpass Filter

Sixth Order Bandpass Filter Signal Flowgraph

Double-Sampled Fully Differential 6th Order S.C. All-Pole Bandpass Filter

- Cont. time termination (Q) implementation
- Folded-Cascode opamp with $f_c = 100$MHz used
- Center freq. 3.1MHz (Measured error >1%), filter $Q=55$
- Clock freq. 12.83MHz $\Rightarrow$ effective oversampling ratio 8.27
- Measured dynamic range 46dB ($IM3=1\%$)

Switched-Capacitor Filter Application
Example: Voice-Band CODEC (Coder-Decoder) Chip


CODEC Transmit Path
Lowpass Filter Frequency Response

Note: $f_s=128$kHz
Note: $f_s=8$ kHz

Low Q bandpass (Q<1) filter shape → Implemented with lowpass followed by highpass
CODEC Transmit Path
Clocking Scheme

First filter (1st order RC type) performs anti-aliasing for the next S.C. biquad

The first 2 stage filters form 3rd order elliptic with corner frequency @ 32kHz → Anti-aliasing for the next S.C. lowpass filter with 3.4kHz corner freq.

The stages prior to the high-pass perform anti-aliasing for high-pass

Notice gradual lowering of clock frequency → Ease of anti-aliasing

SC Filter Summary

✓ Pole and zero frequencies proportional to
  – Sampling frequency \( f_s \)
  – Capacitor ratios
  ➢ High accuracy and stability in response
  ➢ Long time constants realizable without large R, C

✓ Compatible with transconductance amplifiers
  – Reduced circuit complexity, power dissipation

✓ Amplifier bandwidth requirements less stringent compared to CT filters (low frequencies only)

ệm Issue: Sampled-data filters → require anti-aliasing prefiltering
Switched-Capacitor Filters versus Continuous-Time Filter Limitations

Considering overall effects:
- Opamp finite unity-gain-bandwidth
- Opamp settling issues
- Opamp finite slew rate
- Clock feedthru & switch charge injection
- Switch+ sampling cap. finite time-constant

→ Limited switched-capacitor filter performance frequency range

Summary
Filter Performance versus Filter Topology

<table>
<thead>
<tr>
<th></th>
<th>Max. Usable Bandwidth</th>
<th>SNDR</th>
<th>Freq. Tolerance w/o Tuning</th>
<th>Freq. Tolerance + Tuning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Opamp-RC</td>
<td>~10MHz</td>
<td>60-90dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Opamp-MOSFET-C</td>
<td>~5MHz</td>
<td>40-60dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Opamp-MOSFET-RC</td>
<td>~5MHz</td>
<td>50-90dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Gm-C</td>
<td>~100MHz</td>
<td>40-70dB</td>
<td>+40-60%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Switched Capacitor</td>
<td>~10MHz</td>
<td>40-90dB</td>
<td>&lt;1%</td>
<td>–</td>
</tr>
</tbody>
</table>
Frequency Warping

- Frequency response
  - Continuous time (s-plane): imaginary axis
  - Sampled time (z-plane): unit circle
- Continuous to sampled time transformation
  - Should map imaginary axis onto unit circle
  - How do S.C. integrators map frequencies?

\[
H_{SC}(z) = \frac{C_s}{C_{int}} \frac{z^{-\frac{1}{2}}}{1 - z^{-1}} = -\frac{C_s}{C_{int}} \frac{1}{2j \sin \pi f T_{int}}
\]

CT – SC Integrator Comparison

<table>
<thead>
<tr>
<th>CT Integrator</th>
<th>SC Integrator</th>
</tr>
</thead>
<tbody>
<tr>
<td>[H_{RC}(s) = -\frac{1}{s\tau} = \frac{1}{2\pi f RC \tau}]</td>
<td>[H_{SC}(z) = \frac{C_s}{C_{int}} \frac{z^{-\frac{1}{2}}}{1 - z^{-1}} = -\frac{C_s}{C_{int}} \frac{1}{2j \sin \pi f_{SC} T_{int}}]</td>
</tr>
</tbody>
</table>

Identical time constants:
\[\tau = RC = \frac{C_{int}}{f_s C_s}\]

Set: \[H_{RC}(f_{RC}) = H_{SC}(f_{SC}) \rightarrow f_{RC} = \frac{L}{\pi} \sin \left(\frac{\pi f_{SC}}{f_s}\right)\]
LDI Integration

\[ f_{\text{RC}} = \frac{f_s}{\pi} \sin \left( \frac{\pi f_{\text{SC}}}{f_s} \right) \]

- "RC" frequencies up to \( f_s / \pi \) map to physical (real) "SC" frequencies
- Frequencies above \( f_s / \pi \) do not map to physical frequencies
- Mapping is symmetric about \( f_s / 2 \) (aliasing)
- "Accurate" only for \( f_{\text{RC}} << f_s \)

Material Covered in EE247

Where are We?

✓ Filters
  - Continuous-time filters
    • Biquads & ladder type filters
    • Opamp-RC, Opamp-MOSFET-C, \( gm \)-C filters
    • Automatic frequency tuning
  - Switched capacitor (SC) filters

- Data Converters
  - D/A converter architectures
  - A/D converter
    • Nyquist rate ADC - Flash, Pipeline ADCs, …
    • Oversampled converters
    • Self-calibration techniques
- Systems utilizing analog/digital interfaces
Data Converters

• Data converters
  – Areas of application
  – Data converter transfer characteristics
  – Sampling, aliasing, reconstruction
  – Amplitude quantization
  – Static converter error sources
    • Offset
    • Full-scale error
    • Differential non-linearity (DNL)
    • Integral non-linearity (INL)

Data Converter Applications
Data Converter Basics

- DSPs benefited from device scaling

- However, real world signals are still analog:
  - Continuous time
  - Continuous amplitude

- DSP can only process:
  - Discrete time
  - Discrete amplitude

→ Need for data conversion from analog to digital and digital to analog

A/D & D/A Conversion

A/D Conversion

- Analog Input
- Anti-alias Filtering
- Sampling
- Quantization
- Digital Filter
- Digital Coding
- Digital Out

D/A Conversion

- Digital In
- Digital Decoding
- DAC
- Analog Hold
- Reconstruction Filtering
- Analog Out
Data Converters

- Stand alone data converters
  - Used in variety of systems
  - Example: Analog Devices AD9235 12bit/ 65Ms/s
  ADC- Applications:
    - Ultrasound equipment
    - IF sampling in wireless receivers
    - Various hand-held measurement equipment
    - Low cost digital oscilloscopes

Data Converters

- Embedded data converters
  - Integration of data conversion interfaces along with DSPs and/or RF circuits → Cost, reliability, and performance
  - Main issues
    - Feasibility of integrating sensitive analog functions in a technology typically optimized for digital performance
    - Down scaling of supply voltage as a result of downscaling of feature sizes
    - Interference & spurious signal pick-up from on-chip digital circuitry and/or high frequency RF circuits
    - Portable applications dictate low power consumption
Embedded Converters
Example: Typical Cell Phone

Contains in integrated form:
- 4 Rx filters
- 4 Tx filters
- 4 Rx ADCs
- 4 Tx DACs
- 3 Auxiliary ADCs
- 8 Auxiliary DACs

Total: Filters → 8
ADCs → 7
DACs → 12

D/A Converter Transfer Characteristics

- An ideal digital-to-analog converter:
  - Accepts digital inputs $b_1-b_n$
  - Produces either an analog output voltage or current
  - Assumption (will be revisited)
    - Uniform, binary digital encoding
    - Unipolar output ranging from 0 to $V_{FS}$

Nomenclature:
$N = \# \text{ of bits}$
$V_{FS} = \text{full scale output}$
$\Delta = \text{min. step size} \rightarrow \text{LSB}$
$\Delta = \frac{V_{FS}}{2^N}$
or $N = \log_2 \frac{V_{FS}}{\Delta} \rightarrow \text{resolution}$
D/A Converter Transfer Characteristics

\[ N = \text{# of bits} \]

\[ V_{FS} = \text{full scale output} \]

\[ \Delta = \text{min. step size} \rightarrow \text{LSB} \]

\[ \Delta = \frac{V_{FS}}{2^N} \]

\[ V_o = V_{FS} \sum_{i=0}^{N} b_i \times 2^{-i} \]

\[ = \Delta \times \sum_{i=0}^{N} b_i \times 2^{N-i}, \quad b_i = 0 \text{ or } 1 \]

Note: D(b_i = 1, all i)

\[ \rightarrow V_{o_{\text{max}}} = V_{FS} - \Delta \]

\[ \rightarrow V_{o_{\text{max}}} = V_{FS} \left(1 - \frac{1}{2^N}\right) \]

D/A Converter Example: D/A with 3-bit Resolution

Example: for \( N = 3 \) and \( V_{FS} = 0.8V \)

input code \( \Rightarrow 101 \)

Find the output value \( V_o \)

\[ V_o = \Delta \left( b_1 \times 2^2 + b_2 \times 2^1 + b_3 \times 2^0 \right) \]

Then: \( \Delta = V_{FS} / 2^3 = 0.4V \)

\[ \rightarrow V_o = 0.4V \left( 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 \right) = \]

\[ \rightarrow V_o = 0.5V \]

Note: MSB \( \rightarrow V_{FS} / 2 \) & LSB \( \rightarrow V_{FS} / 2^N \)
Ideal 3-Bit D/A Transfer Characteristic

- Ideal DAC introduces no error!
- One-to-one mapping from input to output

Ideal Response

Digital Input Code

Analog Output

Step Height (VLSB $\Delta$)

A/D Converter Transfer Characteristics

- An ideal analog-to-digital converter:
  - Accepts analog input in the form of either voltage or current
  - Produces digital output either in serial or parallel form
  - Assumption (will be revisited)
    - Unipolar input ranging from 0 to $V_{FS}$
    - Uniform, binary digital encoding

\[
N = \# \text{ of bits} \\
V_{FS} = \text{full scale output} \\
\Delta = \min. \text{ resolvable input} \rightarrow 1 \text{ LSB} \\
\Delta = \frac{V_{FS}}{2^N} \\
\text{or } N = \log_2 \frac{V_{FS}}{\Delta} \rightarrow \text{resolution}
\]
Ideal A/D Transfer Characteristic
Example: 3Bit A/D Converter

- Ideal ADC introduces error with max peak-to-peak: 
  \[ \pm \frac{1}{2^{N}} \Delta \]
  \[ \Delta = \frac{V_{FS}}{2^{N}} \]
  \( N = \# \text{ of bits} \)

- This error is called "quantization error"

- For a given VFS as N increases, quantization error decreases \( \Rightarrow \) resolution increases

Non-Linear Data Converters

- So far data converter characteristics studied are with uniform, binary digital encoding

- For some applications to maximize dynamic range, non-linear coding is used e.g. Voice-band telephony,
  - Small signals \( \Rightarrow \) larger \# of codes
  - Large signals \( \Rightarrow \) smaller \# of codes
Example: Non-Linear A/D Converter For Voice-Band Telephony Applications

Non-linear ADC and DAC used in voice-band CODECs

- To maximize dynamic range without need for large # of bits
- Non-linear Coding scheme called A-law & μ-law is used
- Also called companding


Data Converter Performance Metrics

- Data Converters are typically characterized by static, time-domain, & frequency domain performance metrics:
  - Static
    - Offset
    - Full-scale error
    - Differential nonlinearity (DNL)
    - Integral nonlinearity (INL)
    - Monotonicity
  - Dynamic
    - Delay & settling time
    - Aperture uncertainty
    - Distortion-harmonic content
    - Signal-to-noise ratio (SNR), Signal-to-(noise+distortion) ratio (SNDR)
    - Idle channel noise
    - Dynamic range & spurious-free dynamic range (SFDR)
Typical Sampling Process

C.T. ⇒ S.D. ⇒ D.T.

Continuous Time

Sampled Data (e.g. T/H signal)

Clock

Discrete Time

Physical Signals

"Memory Content"

Discrete Time Signals

- A sequence of numbers (or vector) with discrete index time instants

- Intermediate signal values not defined (not the same as equal to zero!)

- Mathematically convenient, non-physical

- We will use the term "sampled data" for related signals that occur in real, physical interface circuits
Uniform Sampling

- Samples spaced T seconds in time
- Sampling Period T ⇔ Sampling Frequency $f_s = 1/T$
- Problem: Multiple continuous time signals can yield exactly the same discrete time signal (aliasing)

Data Converters

- ADC/DACs need to sample/reconstruct to convert from continuous-time to discrete-time signals and back
- Purely mathematical discrete-time signals are different from "sampled-data signals" that carry information in actual circuits
- Question: How do we ensure that sampling/reconstruction fully preserve information?
**Aliasing**

- The frequencies $f_x$ and $nf_x \pm f_x$, $n$ integer, are indistinguishable in the discrete time domain.

- Undesired frequency interaction and translation due to sampling is called aliasing.

- If aliasing occurs, no signal processing operation downstream of the sampling process can recover the original continuous time signal!

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**Frequency Domain Interpretation**

- **Signal scenario before sampling**

- **Signal scenario after sampling** → DT

  > Signals @ $nf_x \pm f_{\text{max signal}}$ fold back into band of interest → Aliasing
Brick Wall Anti-Aliasing Filter

Sampling at Nyquist rate ($f_s = 2f_{signal}$) → required brick-wall anti-aliasing filters

Practical Anti-Aliasing Filter

- Practical filter: Nonzero "transition band"
- In order to make this work, we need to sample faster than 2x the signal bandwidth
- "Oversampling"
Data Converter Classification

• $f_s > 2f_{max}$ Nyquist Sampling
  - "Nyquist Converters"
  - Actually always slightly oversampled (e.g. CODEC $f_{sig}^{max} = 3.4kHz$ &
    ADC sampling $8kHz \rightarrow f_s/f_{max} = 2.35$)
  - Requires anti-aliasing filtering prior to A-to-D conversion

• $f_s >> 2f_{max}$ Oversampling
  - "Oversampled Converters"
  - Anti-alias filtering is often trivial
  - Oversampling is also used to reduce quantization noise, see later
    in the course...

• $f_s < 2f_{max}$ Undersampling (sub-sampling)

Sub-Sampling

- Sub-sampling → sampling at a rate less than Nyquist rate → aliasing
- For signals centered @ an intermediate frequency → Not destructive!
- Sub-sampling can be exploited to mix a narrowband RF or IF signal down
to lower frequencies
Nyquist Data Converter Topics

- Basic operation of data converters
  - Uniform sampling and reconstruction
  - Uniform amplitude quantization
- Characterization and testing
- Common ADC/DAC architectures
- Selected topics in converter design
  - Practical implementations
  - Compensation & calibration for analog circuit non-idealities
- Figures of merit and performance trends

Where Are We Now?

- We now know how to preserve signal information in CT → DT transition
- How do we go back from DT → CT?
Ideal Reconstruction

\[ x(k) \Rightarrow x(t) \]

- The DSP books tell us:

\[ x(t) = \sum_{k=-\infty}^{\infty} x(k) \cdot g(t-kT) \quad g(t) = \frac{\sin(2\pi B t)}{2\pi B t} \]

- Unfortunately not all that practical...

---

Zero-Order Hold Reconstruction

- How about just creating a staircase, i.e. hold each discrete time value until new information becomes available?

- What does this do to the frequency content of the signal?

- Let's analyze this in two steps...
DT → CT: Infinite Zero Padding

**Time Domain**

- DT sequence: \[ \cdots \uparrow \uparrow \uparrow \cdots \]

**Frequency Domain**

- Infinite Zero padded
- Interpolation: CT Signal

\[ \cdots \uparrow \uparrow \uparrow \cdots \]\n
Next step: pass the samples through a sample & hold stage (ZOH)

\[
|H(f)| = \left| \frac{\sin(\pi f T_s)}{\pi f T_s} \right|
\]

**Hold Pulse** $T_p = T_s$ Transfer Function

```
abs(H(f))
```

\[
T_p = T_s
\]
ZOH Spectral Shaping

Continuous Time Pulse Train Spectrum

ZOH Transfer Function ("Sinc Shaping")

ZOH output, Spectrum of Staircase Approximation

Smoothing Filter

- Order of the filter required is a function of oversampling ratio
- High oversampling helps reduce filter order requirement

Filter out the high frequency content associated with staircase shape of the signal
Summary

- Sampling theorem, $f_s > 2f_{\text{max}}$, usually dictates anti-aliasing filter
- If theorem is met, CT signal can be recovered from DT without loss of information
- ZOH and smoothing filter reconstruct CT signal from DT vector
- Oversampling helps reduce order & complexity of anti-aliasing & smoothing filters