EE247 Lecture 14

• Administrative issues
  ▪ Midterm exam postponed to **Thurs. Nov. 5th**
    o You can *only* bring one 8x11 paper with your own written notes (please do not photocopy)
    o No books, class or any other kind of handouts/notes, calculators, computers, PDA, cell phones....
    o Midterm includes material covered to end of lecture 14

EE247 Lecture 14

• D/A converters
  – D/A converters: Various Architectures (continued)
    • Charge scaling DACs (continued)
    • R-2R type DACs
    • Current based DACs
  – Static performance of D/As
    • Component matching
    • Systematic & random errors
  – Practical aspects of current-switched DACs
  – Segmented current-switched DACs
  – DAC dynamic non-idealities
  – DAC design considerations
Summary of Last Lecture

• Data Converters
  – Data converter testing (continued)
    • Dynamic tests (continued)
      – Relationship between: DNL & SNR, INL & SFDR
      – Effective number of bits (ENOB)
  – D/A converters: Various Architectures
    • Resistor string DACs
    • Serial charge redistribution DACs
    • Charge scaling DACs
    • R-2R type DACs
    • Current based DACs

Charge Scaling DAC Utilizing Split Array

- Split array → reduce the total area of the capacitors required for high resolution DACs
  - E.g. 10bit regular binary array requires 1024 unit Cs while split array (5&5) needs 64 unit Cs
  - Issue: Sensitive to parasitic capacitor
Charge Scaling DAC

- **Advantages:**
  - Low power dissipation → capacitor array does not dissipate DC power
  - Output is sample and held → no need for additional S/H
  - INL function of capacitor ratio
  - Possible to trim or calibrate for improved INL
  - Offset cancellation almost for free

- **Disadvantages:**
  - Process needs to include good capacitive material → not compatible with standard digital process
  - Requires large capacitor ratios
  - Not inherently monotonic (more later)

Segmented DAC

Resistor Ladder (MSB) & Binary Weighted Charge Scaling (LSB)

- Example: 12bit DAC
  - 6-bit MSB DAC → R-string
  - 6-bit LSB DAC → binary weighted charge scaling

- Component count much lower compared to full R-string
  - Full R string → 4096 resistors
  - Segmented → 64 R + 7 Cs (64 unit caps)

6-bit binary weighted charge redistribution DAC
Current Based DACs

R-2R Ladder Type

- R-2R DAC basics:
  - Simple R network divides both voltage & current by 2

Increase # of bits by replicating circuit

R-2R Ladder DAC

Emitter-follower added to convert to high output impedance current sources
R-2R Ladder DAC
How Does it Work?

Consider a simple 3bit R-2R DAC:

Simple 3bit DAC:
1- Consolidate first two stages:
R-2R Ladder DAC
How Does it Work?

Consider a simple 3bit R-2R DAC:

\[ I_3 = I_2 + I_1 + I_T \]
\[ I_3 = \frac{I_{\text{Total}}}{2}, \quad I_2 = \frac{I_{\text{Total}}}{4}, \quad I_1 = \frac{I_{\text{Total}}}{8} \]

In most cases need to convert output current to voltage

R-2R Ladder DAC

Trans-resistance amplifier added to:
- Convert current to voltage
- Generate virtual ground @ current summing node so that output impedance of current sources do not cause error
- Issue: error due to opamp offset

\[
V_{\text{out}} = \frac{I}{R_{\text{Total}}} + V_{\text{os}}\left(1 + \frac{R}{R_{\text{Total}}}\right)
\]

If \(R_{\text{Total}}\) large,
\[V_{\text{out}} = V_{\text{os}}\]

If \(R_{\text{Total}}\) not large
\[V_{\text{out}} = V_{\text{os}} \left(1 + \frac{R}{R_{\text{Total}}}\right)\]

Problem:
Since \(R_{\text{Total}}\) is code dependant
\[V_{\text{out}}\] would be code dependant

\[\rightarrow \text{Gives rise to INL & DNL}\]
R-2R Ladder Summary

• Advantages:
  – Resistor ratios only x2
  – Does not require precision capacitors

• Disadvantages:
  – Total device emitter area \( \Rightarrow A_{E\,\text{unit}} \times 2^B \)
  \( \Rightarrow \) Not practical for high resolution DACs
  – INL/DNL error due to amplifier offset

Current based DAC
Unit Element Current Source DAC

• “Unit elements” or thermometer
• \( 2^{B-1} \) current sources & switches
• Suited for both MOS and BJT technologies
• Monotonicity does not depend on element matching and is guaranteed
• Output resistance of current source \( \Rightarrow \) gain error
  – Cascode type current sources higher output resistance \( \Rightarrow \) less gain error
Current Source DAC
Unit Element

- Output resistance of current source → gain error problem
  → Use transresistance amplifier
    - Current source output held @ virtual ground
    - Error due to current source output resistance eliminated
    - New issues: offset & speed of the amplifier

Current Source DAC
Binary Weighted

- “Binary weighted”
- B current sources & switches ($2^B-1$ unit current sources but less # of switches)
- Monotonicity depends on element matching → not guaranteed
Static DAC Errors - INL / DNL

Static DAC errors mainly due to component mismatch

– Systematic errors
  • Contact resistance
  • Edge effects in capacitor arrays
  • Process gradients
  • Finite current source output resistance

– Random variations
  • Lithography etc…
  • Often Gaussian distribution (central limit theorem)


Current Source DAC

DNL/INL Due to Element Mismatch

• Simplified example:
  – 3-bit DAC
  – Assume only two of the current sources mismatched (# 4 & #5)
Current Source DAC
DNL/INL Due to Element Mismatch

\[ DNL[m] = \frac{\text{segment}[m] - V[\text{LSB}]}{V[\text{LSB}]} \]
\[ DNL[4] = \frac{\text{segment}[4] - V[\text{LSB}]}{V[\text{LSB}]} = \frac{(1-\Delta)R - IR}{IR} \]
\[ DNL[5] = \frac{\text{segment}[5] - V[\text{LSB}]}{V[\text{LSB}]} = \frac{(1+\Delta)R - IR}{IR} \]
\[ \rightarrow \text{INL}_{\text{max}} = -\Delta / I \text{[LSB]} \]

Component Mismatch
Probability Distribution Function

- Component parameters \( \rightarrow \) Random variables
- Each component is the product of many fabrication steps
- Most fabrication steps includes random variations
  \( \rightarrow \) Overall component variations product of several random variables
- Assuming each of these variables have a uniform pdf distribution:
  \( \rightarrow \) Joint pdf of a random variable affected by two uniformly distributed variables \( \rightarrow \) convolution of the two uniform pdfs…….

\[ \text{pdf}[f(x_1)] \star \text{pdf}[f(x_2)] \rightarrow \text{pdf}[f(x_1,x_2)] \]
\[ \star \rightarrow \text{pdf}[f(x_1,x_2)] \star \text{pdf}[f(x_3,x_4)] \star \cdots \star \text{pdf}[f(x_m,x_n)] \rightarrow \text{Gaussian pdf} \]
Gaussian Distribution

The probability density function for a Gaussian distribution is given by:

\[ p(x) = \frac{1}{\sqrt{2\pi\sigma}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \]

where:
- \( \mu \) is the expected value
- \( \sigma \) is the standard deviation
- \( \sigma^2 \) is the variance

Yield

In most cases, we are interested in finding the percentage of components (e.g., R) falling within certain bounds:

\[ P(-X \leq x \leq +X) = \]

\[ = \frac{1}{\sqrt{2\pi}} \int_{-X}^{+X} e^{-\frac{y^2}{2}} \, dy \]

\[ = \text{erf}\left( \frac{X}{\sqrt{2}} \right) \]

Integral has no analytical solution \( \rightarrow \) found by numerical methods.
Yield

<table>
<thead>
<tr>
<th>$X/\sigma$</th>
<th>$P(-X \leq x \leq X)$ [%]</th>
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<th>$P(-X \leq x \leq X)$ [%]</th>
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<td>0.2000</td>
<td>15.8519</td>
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<td>97.2193</td>
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<td>0.4000</td>
<td>31.0843</td>
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<td>2.6000</td>
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<td>83.8487</td>
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<td>89.0401</td>
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<td>92.8139</td>
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<tr>
<td>2.0000</td>
<td>95.4500</td>
<td>4.0000</td>
<td>99.9937</td>
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Example

- Measurements show that the offset voltage of a batch of operational amplifiers follows a Gaussian distribution with $\sigma = 2mV$ and $\mu = 0$.

- Find the fraction of opamps with $|V_{os}| < 6mV$:
  - $X/\sigma = 3 \Rightarrow 99.73\%$ yield

- Fraction of opamps with $|V_{os}| < 400\mu V$:
  - $X/\sigma = 0.2 \Rightarrow 15.85\%$ yield
Component Mismatch

Example: Resistors layouted out side-by-side

After fabrication large # of devices measured & graphed → typically if sample size large shape is Gaussian

E.g. Let us assume in this example 1000 Rs measured & 68.5% fall within ±4Ω, or ±0.4% of average
→ 1σ for resistors → 0.4%

Example: Two resistors layouted out side-by-side

For typical technologies & geometries
1σ for resistors → 0.02 to 5%

In the case of resistors σ is a function of area
DNL Unit Element DAC

E.g. Resistor string DAC:
Assumption: No systematic error - only random error

\[ \Delta = R_{\text{median}} I_{\text{ref}} \]
\[ \Delta_i = R_i I_{\text{ref}} \]

\[ DNL_i = \frac{\Delta_i - \Delta_{\text{median}}}{\Delta_{\text{median}}} \]
\[ = \frac{R_i - R_{\text{median}}}{R_{\text{median}}} = \frac{dR}{R_{\text{median}}} \]

\[ \sigma_{DNL} = \sigma_{dR_i} \]

To first order \( \Rightarrow \) DNL of unit element DAC is independent of resolution!

Note: Similar results for other unit-element based DACs

Example:
If \( \sigma_{dR/R} = 0.4\% \), what DNL spec goes into the DAC datasheet so that 99.9\% of all converters meet the spec?
### Yield

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#### DNL Unit Element DAC

**Example:**
If $\sigma_{dR/R} = 0.4\%$, what DNL spec goes into the datasheet so that 99.9% of all converters meet the spec?

**Answer:**
From table: for 99.9%

$X/\sigma = 3.3$

$\sigma_{DNL} = \sigma_{dR/R} = 0.4\%$

$3.3 \sigma_{DNL} = 3.3 \times 0.4\% = 1.3\%$

$\rightarrow$ DNL = +/- 0.013 LSB
### DAC INL Analysis

#### Ideal Variance

<table>
<thead>
<tr>
<th></th>
<th>$A=n+E$</th>
<th>$n$</th>
<th>$n\cdot \sigma_e^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$B=N-n-E$</td>
<td>$N-n$</td>
<td>$(N-n)\cdot \sigma_e^2$</td>
<td></td>
</tr>
</tbody>
</table>

\[ E = A-n \quad r = n/N \quad N = A+B \]

\[ = A-r(A+B) \]

\[ = (1-r) \cdot A - r \cdot B \]

\[ \rightarrow \text{Variance of } E: \]

\[ \sigma_e^2 = (1-r)^2 \cdot \sigma_A^2 + r^2 \cdot \sigma_B^2 \]

\[ = N \cdot r \cdot (1-r) \cdot \sigma_e^2 = n \cdot (1 - n/N) \cdot \sigma_e^2 \]

---

**DAC INL**

\[ \sigma_e^2 = n \left(1 - \frac{n}{N}\right) \cdot \sigma_e^2 \]

*To find max. variance:*

\[ \frac{d\sigma_e^2}{dn} = 0 \]

\[ \rightarrow n = N/2 \rightarrow \sigma_e^2 = \frac{N}{4} \cdot \sigma_e^2 \]

- Error is maximum at mid-scale ($N/2$):

\[ \sigma_{\text{INL}} = \frac{1}{2} \sqrt{2^B - 1} \cdot \sigma_e \]

*with* $N = 2^B - 1$

- INL depends on both DAC resolution & element matching $\sigma_e$

- While $\sigma_{\text{INL}} = \sigma_e$ is to first order independent of DAC resolution and is only a function of element matching

Ref: Kuboki et al., TCAS, 6/1982
Untrimmed DAC INL

Example:
Assume the following requirement for a DAC:

\[ \sigma_{\text{INL}} = 0.1 \text{ LSB} \]

Find maximum resolution for:

\[ B \equiv 2 + 2 \log_2 \left( \frac{\sigma_{\text{INL}}}{\epsilon} \right) \]

\[ \sigma_\epsilon = 1\% \Rightarrow B_{\text{max}} = 8.6 \text{bits} \]
\[ \sigma_\epsilon = 0.5\% \Rightarrow B_{\text{max}} = 10.6 \text{bits} \]
\[ \sigma_\epsilon = 0.2\% \Rightarrow B_{\text{max}} = 13.3 \text{bits} \]
\[ \sigma_\epsilon = 0.1\% \Rightarrow B_{\text{max}} = 15.3 \text{bits} \]

Note: In most cases, a number of systematic errors prevents achievement of above results

Simulation Example

\[ \sigma_{\epsilon} = 1\% \]
\[ B = 12 \]

Random # generator used in MatLab

Computed INL:
\[ \sigma_{\text{INL, max}} = 0.32 \text{ LSB (midscale)} \]

Why is the results not as expected per our derivation?
INL & DNL for Binary Weighted DAC

- INL same as for unit element DAC

- DNL depends on transition
  - Example:
    0 to 1 \( \rightarrow \sigma_{DNL}^2 = \sigma_{(dI/dV)}^2 \)
    1 to 2 \( \rightarrow \sigma_{DNL}^2 = 3\sigma_{(dI/dV)}^2 \)

- Consider MSB transition:
  0111 ... \( \rightarrow \) 1000 ...

DAC DNL

Example: 4bit DAC

- DNL depends on transition
  - Example:
    0 to 1 \( \rightarrow \sigma_{DNL}^2 = \sigma_{(dI_{ref}/dV)}^2 \)
    1 to 2 \( \rightarrow \sigma_{DNL}^2 = 3\sigma_{(dI_{ref}/dV)}^2 \)
**Binary Weighted DAC DNL**

- Worst-case transition occurs at mid-scale:

\[
\sigma_{DNL}^2 = \frac{\left(2^B - 1\right)\sigma_I^2 + \left(2^B - 2\right)\sigma_I^2}{1000...} = 2\sigma_I^2
\]

\[
\sigma_{INL\text{max}} = \frac{1}{2}\sqrt{2^B - 1}\sigma_I = \frac{1}{2}\sigma_{DNL\text{max}}
\]

- Example: 
  \(B = 12, \quad \sigma_I = 1\%\)
  \(\sigma_{DNL} = 0.64\ \text{LSB}\)
  \(\sigma_{INL} = 0.32\ \text{LSB}\)

**MOS Current Source Variations**

Due to Device Matching Effects

\[
I_d = \frac{I_{d1} + I_{d2}}{2}
\]

\[
dI_d = \frac{I_{d1} - I_{d2}}{I_d} \quad I_d
\]

\[
dI_d = \frac{dW/L}{W/L} \quad V_{GS} - V_{th}
\]

- Current matching depends on:
  - Device \(W/L\) ratio matching
    \(\Rightarrow\) Larger device area less mismatch effect
  - Current mismatch due to threshold voltage variations:
    \(\Rightarrow\) Larger gate-overdrive less threshold voltage mismatch effect
Current-Switched DACs in CMOS

\[
\frac{dI_d}{I_d} = \frac{dW}{W/L} + \frac{2dV_{th}}{V_{GS} - V_{th}}
\]

- Advantages:
  - Can be very fast
  - Reasonable area for resolution < 9-10 bits

- Disadvantages:
  - Accuracy depends on device $W/L$ & $V_{th}$ matching

Example: 8bit Binary Weighted

Unit Element versus Binary Weighted DAC

**Unit Element DAC**
\[
\sigma_{DNL} = \sigma_{\epsilon}
\]
\[
\sigma_{INL} \approx \frac{B}{2} - 1 \sigma_{\epsilon}
\]

**Binary Weighted DAC**
\[
\sigma_{DNL} \approx \frac{B}{2} \sigma_{\epsilon} = 2 \sigma_{INL}
\]
\[
\sigma_{INL} \approx \frac{B}{2} - 1 \sigma_{\epsilon}
\]

Number of switched elements:
\[
S = 2^B
\]
\[
S = B
\]

*Key point: Significant difference in performance and complexity!*
### Unit Element versus Binary Weighted DAC

Example: $B=10$

<table>
<thead>
<tr>
<th>Unit Element DAC</th>
<th>Binary Weighted DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sigma_{DNL} = \sigma_\varepsilon$</td>
<td>$\sigma_{DNL} \approx 2^{B/2} \sigma_\varepsilon = 32 \sigma_\varepsilon$</td>
</tr>
<tr>
<td>$\sigma_{INL} \approx 2^{B/2-1} \sigma_\varepsilon = 16 \sigma_\varepsilon$</td>
<td>$\sigma_{INL} \approx 2^{B/2-1} \sigma_\varepsilon = 16 \sigma_\varepsilon$</td>
</tr>
</tbody>
</table>

Number of switched elements:

$$S = 2^B = 1024$$  
$$S = B = 10$$

*Significant difference in performance and complexity!*

---

### “Another” Random Run …

DNL and INL of 12 Bit converter

Now (by chance) worst DNL is mid-scale.

Close to statistical result!
10Bit DAC DNL/INL Comparison
Plots: 100 Simulation Runs Overlaid


Note: $\sigma_e = 2\%$

10Bit DAC DNL/INL Comparison
Plots: RMS for 100 Simulation Runs


Note: $\sigma_e = 2\%$
DAC INL/DNL Summary

- DAC choice of architecture has significant impact on DNL.
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision.
- Results assume uncorrelated random element variations.
- Systematic errors and correlations are usually also important and may affect final DAC performance.


Segmented DAC
Combination of Unit-Element & Binary-Weighted

- Objective: Compromise between unit-element and binary-weighted DAC.
- Approach: 
  - $B_1$ MSB bits → unit elements
  - $B_2$ LSB bits → binary weighted
  - $B_{Total} = B_1 + B_2$

- INL: unaffected same as either architecture.
- DNL: Worst case occurs when LSB DAC turns off and one more MSB DAC element turns on → Same as binary weighted DAC with $(B_2 + 1)$ # of bits.
- Number of switched elements: $(2^{B_1-1}) + B_2$.

**Diagram:**

- A diagram illustrating the combination of unit-element and binary-weighted DACs.
Comparison

Example:

\[
B = 12, \quad B_1 = 5, \quad B_2 = 7 \\
B_1 = 6, \quad B_2 = 6 \\
\]

Assuming: \( \sigma_e = 1\% \)

\[
\sigma_{DNL} \equiv 2^{(B_2-1)} \sigma_e = 2\sigma_{INL} \\
\sigma_{INL} \equiv 2^{(B_1-1)} \sigma_e \\
S = 2^{B_1} - 1 + B_2 \\
\]

Unit element (12+0)

Segmented (6+6)

Segmented (5+7)

Binary weighted(0+12)

<table>
<thead>
<tr>
<th>DAC Architecture (B1+B2)</th>
<th>( \sigma_{INL}[\text{LSB}] )</th>
<th>( \sigma_{DNL}[\text{LSB}] )</th>
<th># of switched elements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit element (12+0)</td>
<td>0.32</td>
<td>0.01</td>
<td>4095</td>
</tr>
<tr>
<td>Segmented (6+6)</td>
<td>0.32</td>
<td>0.13</td>
<td>63+6=69</td>
</tr>
<tr>
<td>Segmented (5+7)</td>
<td>0.32</td>
<td>0.16</td>
<td>31+7=38</td>
</tr>
<tr>
<td>Binary weighted(0+12)</td>
<td>0.32</td>
<td>0.64</td>
<td>12</td>
</tr>
</tbody>
</table>

Practical Aspects

Current-Switched DACs

- Unit element DACs ensure monotonicity by turning on equal-weighted current sources in succession
- Typically current switching performed by differential pairs
- For each diff pair, only one of the devices are on \( \Rightarrow \) switch device mismatch not an issue
- Issue: While binary weighted DAC can use the incoming binary digital word directly, unit element requires a decoder

<table>
<thead>
<tr>
<th>Binary</th>
<th>Thermometer</th>
</tr>
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<tr>
<td>000</td>
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<tr>
<td>001</td>
<td>0000001</td>
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<tr>
<td>010</td>
<td>0000011</td>
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<td>011</td>
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<td>0011111</td>
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<td>110</td>
<td>0111111</td>
</tr>
<tr>
<td>111</td>
<td>1111111</td>
</tr>
</tbody>
</table>

\( \rightarrow \) \( N \) to \( (2^N-1) \) decoder
Segmented Current-Switched DAC

Example: 8bit → 4MSB + 4LSB

- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register

Segmented Current-Switched DAC
Cont'd

- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register
Segmented Current-Switched DAC  
Cont’d

• MSB Decoder
  → Domino logic
  → Example: D4,5,6,7=1 OUT=1

• Register
  → Latched NAND gate:
  → CTRL=1 OUT=INB

Segmented Current-Switched DAC
Reference Current Considerations

• \( I_{ref} \) is referenced to \( V_{DD} \)
  → Problem: Reference current varies with supply voltage

\[ I_{ref} = \left( \frac{V_{DD} \cdot V_{ref}}{R} \right) \]
Segmented Current-Switched DAC

Reference Current Considerations

- $I_{\text{ref}}$ is referenced to $V_{\text{ss}} \rightarrow \text{GND}$

$$I_{\text{ref}} = \frac{(V_{\text{ref}} - V_{\text{ss}})}{R}$$

**Example:**
- 2bit MSB Unit element DAC & 3bit binary weighted DAC

- To ensure monotonicity at the MSB $\rightarrow$ LSB transition: First OFF MSB current source is routed to LSB current generator
DAC Dynamic Non-Idealities

- Finite settling time
  - Linear settling issues: (e.g. RC time constants)
  - Slew limited settling

- Spurious signal coupling
  - Coupling of clock/control signals to the output via switches

- Timing error related glitches
  - Control signal timing skew

Dynamic DAC Error: Timing Glitch

- Consider binary weighted DAC transition 011 → 100
- DAC output depends on timing
- Plot shows situation where the control signals for LSB & MSB
  - LSB/MSBs on time
  - LSB early, MSB late
  - LSB late, MSB early
Glitch Energy

- Glitch energy (worst case) proportional to: $dt \times 2^{B-1}$
- $dt \rightarrow$ error in timing & $2^{B-1}$ associated with half of the switches changing state
- LSB energy proportional to: $T=1/f_s$
- Need $dt \times 2^{B-1} \ll T$ or $dt \ll 2^{-B+1}T$

Examples:

<table>
<thead>
<tr>
<th>$f_s$ [MHz]</th>
<th>B</th>
<th>$dt$ [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12</td>
<td>&lt;&lt; 488</td>
</tr>
<tr>
<td>20</td>
<td>16</td>
<td>&lt;&lt; 1.5</td>
</tr>
<tr>
<td>1000</td>
<td>12</td>
<td>&lt;&lt; 0.5</td>
</tr>
</tbody>
</table>

Timing accuracy for data converters much more critical compared to digital circuitry

DAC Dynamic Errors

- To suppress effect of non-idealities:
  - Retiming of current source control signals
    - Each current source has its own clocked latch incorporated in the current cell
    - Minimization of latch clock skew by careful layout ensuring simultaneous change of bits
  - To minimize control and clock feed through to the output via G-D & G-S of the switches
    - Use of low-swing digital circuitry
DAC Implementation Examples

- Untrimmed segmented

- Current copiers:

- Dynamic element matching:
Two sources of systematic error:
- Finite current source output resistance
- Voltage drop due to finite ground bus resistance

Current-Switched DACs in CMOS

Assumptions:
- $R\times I$ small compared to transistor gate-overdrive

To simplify analysis: Initially, all device currents assumed to be equal to $I$

\[
\begin{align*}
V_{GS_{M1}} &= V_{GS_{M1}} - 4RI \\
V_{GS_{M2}} &= V_{GS_{M1}} - 7RI \\
V_{GS_{M3}} &= V_{GS_{M1}} - 9RI \\
V_{GS_{M4}} &= V_{GS_{M1}} - 10RI \\
I_2 &= k(V_{GS_{M2}} - V_{th})^2 \\
I_2 &= I_1 \left(1 - \frac{4RI}{V_{GS_{M1}} - V_{th}}\right)^2
\end{align*}
\]

Example: 5 unit element current sources
Current-Switched DACs in CMOS

\[ I_2 = k \left( \frac{V_{GS_{th}} - V_{th}}{V_{GS_{th}} - V_{th}} \right)^2 = I_1 \left( 1 - \frac{4RI}{V_{GS_{th}} - V_{th}} \right)^2 \]

\[ g_{m1} = \frac{2I_1}{V_{GS_{th}} - V_{th}} \]

\[ \rightarrow I_2 = I_1 \left( 1 - \frac{4Rg_{m1}}{2} \right)^2 \approx I_1 \left( 1 - 4Rg_{m1} \right) \]

\[ \rightarrow I_3 = I_1 \left( 1 - \frac{7Rg_{m1}}{2} \right)^2 \approx I_1 \left( 1 - 7Rg_{m1} \right) \]

\[ \rightarrow I_4 = I_1 \left( 1 - \frac{9Rg_{m1}}{2} \right)^2 \approx I_1 \left( 1 - 9Rg_{m1} \right) \]

\[ \rightarrow I_5 = I_1 \left( 1 - \frac{10Rg_{m1}}{2} \right)^2 \approx I_1 \left( 1 - 10Rg_{m1} \right) \]

\[ \Rightarrow \text{Desirable to have } g_{m1} \text{ small} \]

Example: 5 unit element current sources

Example: INL of 3-Bit unit element DAC

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7):
  \[ \text{INL} = +0.25 \text{LSB} \]
- If switching of current sources symmetrical (4-3-5-2-6-1-7):
  \[ \text{INL} = +0.09, -0.058 \text{LSB} \]

\[ \Rightarrow \text{INL reduced by a factor of 2.6} \]
Current-Switched DACs in CMOS

Example: DNL of 7 unit element DAC

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  \[ DNL_{max} = +0.15 \text{LSB} \]

- If switching of current sources symmetrical (4-3-5-2-6-1-7)
  \[ DNL_{max} = +0.15 \text{LSB} \]

Two sources of systematic error:
- Finite current source output resistance
- Voltage drop due to finite ground bus resistance

\[ G_m \cdot R = \frac{I_{in}}{V_{gs}} \]

Fig. 9. Symmetrical switching.