# EE247
# Lecture 18

## ADC Converters

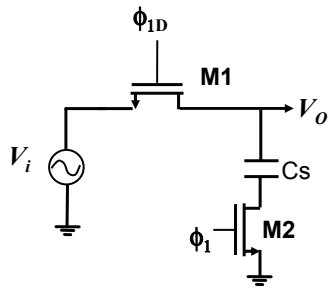
- Sampling (continued)
  - Bottom-plate switching
- Track & hold
  - T/H circuits
  - T/H combined with summing/difference function
  - T/H circuit incorporating gain & offset cancellation
  - T/H aperture uncertainty
- ADC architectures and design
  - Serial- slope type
  - Successive approximation
  - Flash ADC and its sources of error: comparator offset, sparkle code & meta-stability

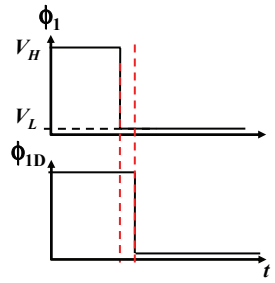


# EE247
# Lecture 18

- Administrative issues
  - Midterm exam on **Thurs. Nov. 5th**
    - You can *only* bring one 8x11 paper with your own written notes (please do not photocopy)
    - No books, class or any other kind of handouts/notes, calculators, computers, PDA, cell phones....
    - Midterm includes material covered to **end of lecture 14**

# Avoiding Switch Charge Injection
# Bottom Plate Sampling

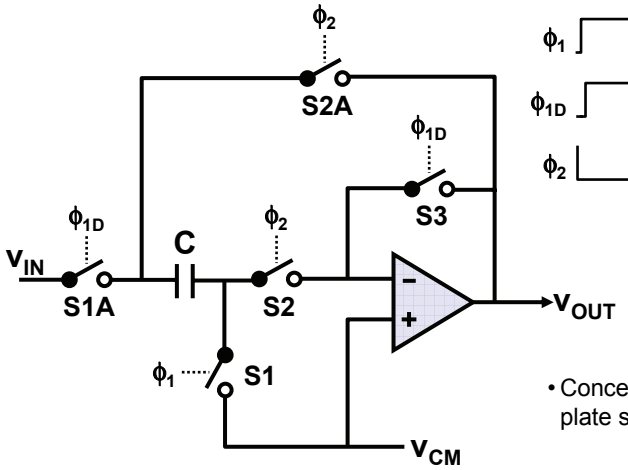


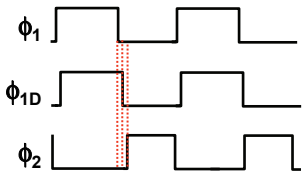




- Switches M2 opened slightly earlier compared to M1
  → Injected charge due to turning off M2 is constant since its GS voltage is constant & eliminated when used differentially
- Since $C_s$ bottom plate is already open when M1 is switched off:
  → No signal dependant charge injected on $C_s$



# Flip-Around Track & Hold

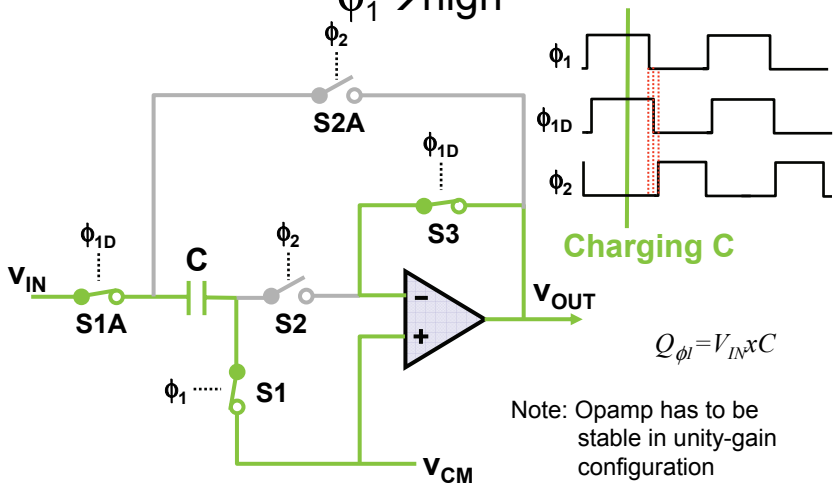



- Concept based on bottom-plate sampling

# Flip-Around T/H-Basic Operation

$\phi_1 \rightarrow$ high







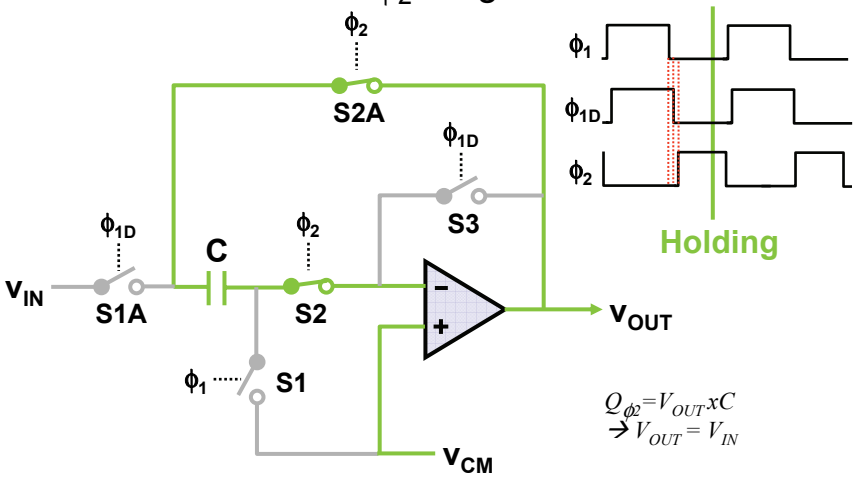
$Q_{\phi 1} = V_{IN} x C$

Note: Opamp has to be stable in unity-gain configuration



# Flip-Around T/H-Basic Operation

$\phi_2 \rightarrow$ high

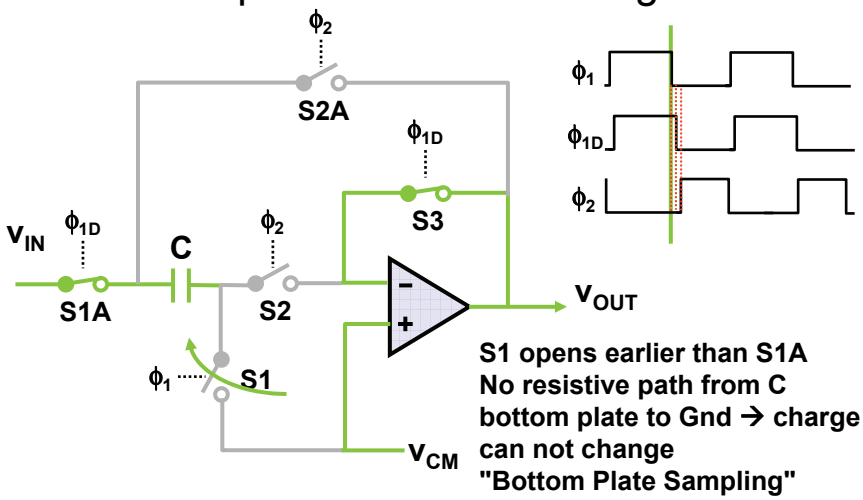






$Q_{\phi 2} = V_{OUT} x C$
$\rightarrow V_{OUT} = V_{IN}$

# Flip-Around T/H - Timing



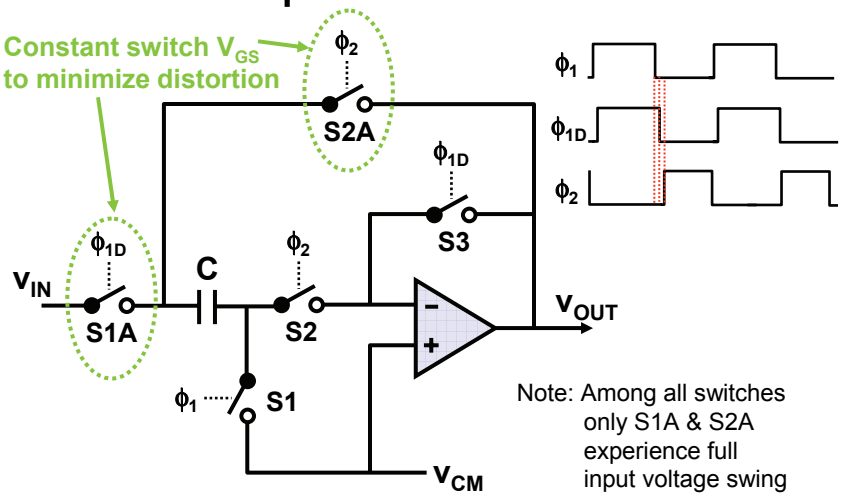

**S1 opens earlier than S1A**
**No resistive path from C bottom plate to Gnd → charge can not change**
**"Bottom Plate Sampling"**



# Charge Injection

- At the instant of transitioning from track to hold mode, some of the charge stored in sampling switch S1 is dumped onto C
- With "Bottom Plate Sampling", only charge injection component due to opening of S1 and is to first-order independent of $v_{IN}$
  - Only a dc offset is added. This dc offset can be removed with a differential architecture

# Flip-Around T/H



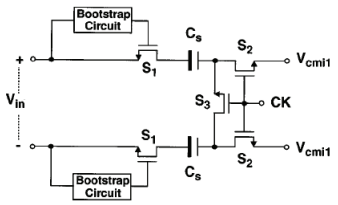

Note: Among all switches only S1A & S2A experience full input voltage swing



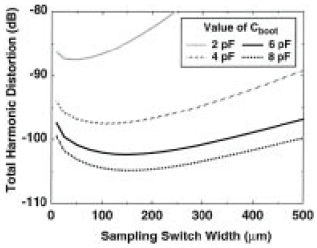
# Flip-Around T/H

- S1 is chosen to be an n-channel MOSFET
- Since it always switches the same voltage, it's on-resistance, $R_{S1}$, is signal-independent (to first order)
- Choosing $R_{S1} >> R_{S1A}$ minimizes the non-linear component of $R = R_{S1A} + R_{S1}$
  - Typically, S1A is a wide (much lower resistance than S1) & constant $V_{GS}$ switch
  - In practice size of S1A is limited by the (nonlinear) S/D capacitance that also adds distortion
  - If S1A's resistance is negligible → delay depends only on S1 resistance
  - S1 resistance is independent of $V_{IN}$ → error due to finite time-constant → independent of $V_{IN}$

# Differential Flip-Around T/H
# Choice of Sampling Switch Size




$C_s$=7pF

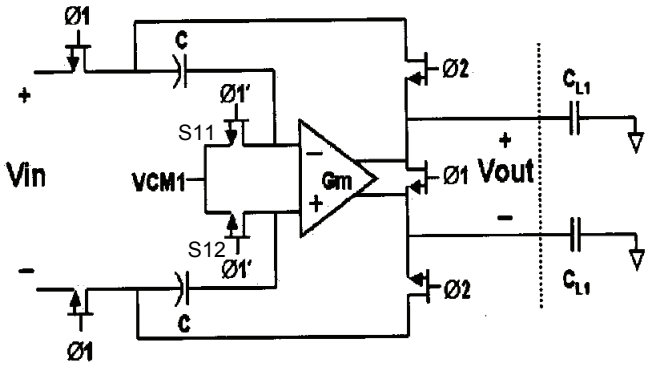



- THD simulated w/o sampling switch boosted clock → -45dB
- THD simulated with sampling switch boosted clock (see graph)

Ref: K. Vleugels et al, "A 2.5-V Sigma–Delta Modulator for Broadband Communications Applications " IEEE JSSC, VOL. 36, NO. 12, DECEMBER 2001, pp. 1887



# Differential Flip-Around T/H

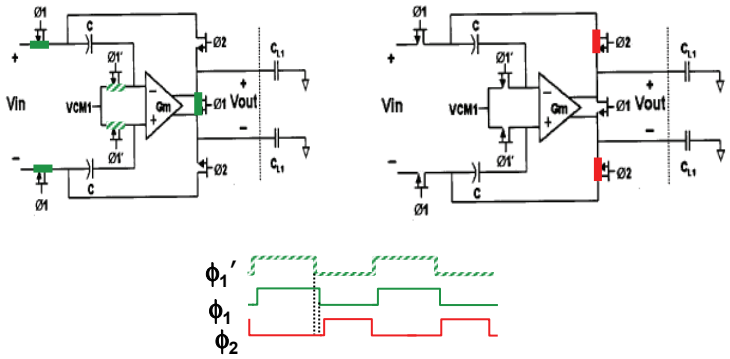



Offset voltage associated with charge injection of S11 & S12 cancelled by differential nature of the circuit

During input sampling phase→ amp outputs shorted together

Ref: W. Yang, *et al.* "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR at Nyquist Input," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001 1931

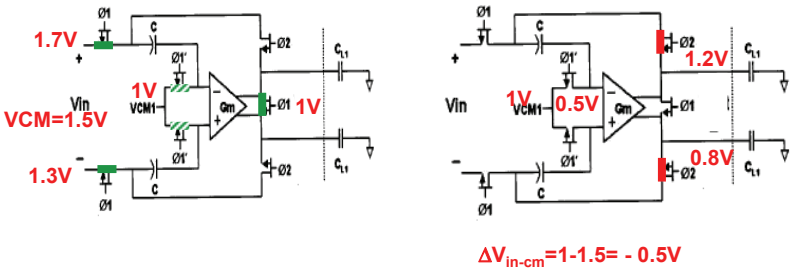
# Differential Flip-Around T/H




- Gain=1
- Feedback factor=1



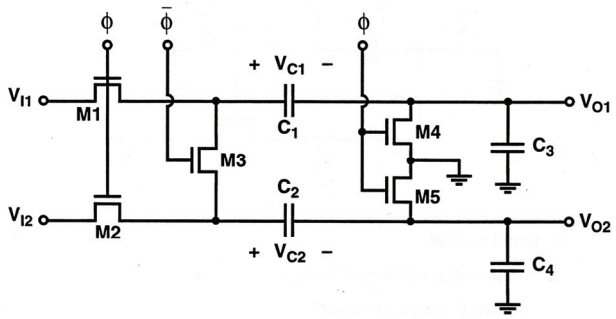
# Differential Flip-Around T/H
## Issues: Input Common-Mode Range




$\Delta V_{in\text{-}cm}$=1-1.5= - 0.5V

- $\Delta V_{in\text{-}cm}=V_{out_com}-V_{sig_com}$
  → Drawback: Amplifier needs to have large input common-mode compliance

# Input Common-Mode Cancellation

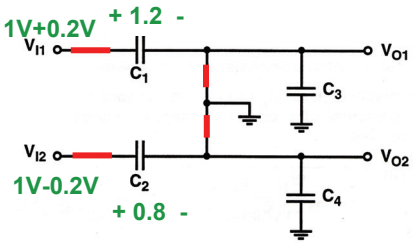


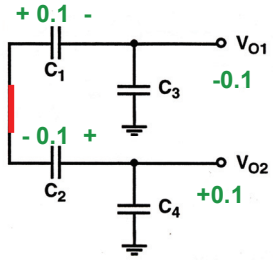

- Note: Shorting switch M3 added

Ref: R. Yen, *et al.* "A MOS Switched-Capacitor Instrumentation Amplifier," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-17, NO. 6,, DECEMBER 1982 1008



# Input Common-Mode Cancellation




Track mode (ϕ high)
$V_{C1}=V_{I1}$ , $V_{C2}=V_{I2}$
$V_{o1}=V_{o2}=0$

Hold mode (ϕ low)
$V_{o1}+V_{o2}=0$
$V_{o1}-V_{o2}= -(V_{I1}-V_{I2})(C_1/(C_1+C_3))$

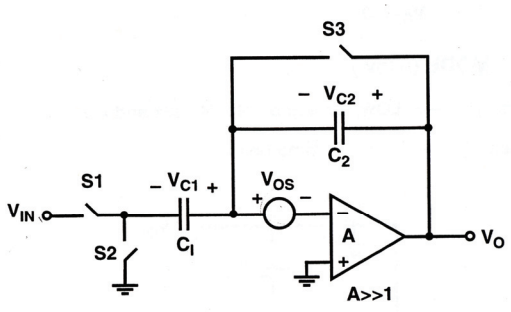
→ Input common-mode level removed

## Switched-Capacitor Techniques Combining Track & Hold with Other Functions

- T/H + Charge redistribution amplifier
- T/H & Input difference amplifier
- T/H & summing amplifier
- Differential T/H combined with gain stage
- Differential T/H including offset cancellation



## T/H + Charge Redistribution Amplifier




Track mode: (S1, S3 →on S2→ off)

$V_{C1}=V_{os}-V_{IN}$ , $V_{C2}=0$

$V_o=V_{os}$

# T/H + Charge Redistribution Amplifier Hold Mode

$V_{C1} \longrightarrow V_{os}$

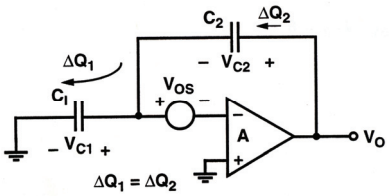
$\Delta V_{C1} = V_{os} - (V_{os} - V_{IN}) = V_{IN}$

$\Delta Q_1 = C_1 \Delta V_{C1} = C_1 V_{IN}$

$\Delta Q_2 = C_2 \Delta V_{C2} = \Delta Q_1$

$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right) V_{C1} = V_{C2}$

$V_O = V_{C2} + V_{os} = \left(\frac{C_1}{C_2}\right) V_{IN} + V_{os}$

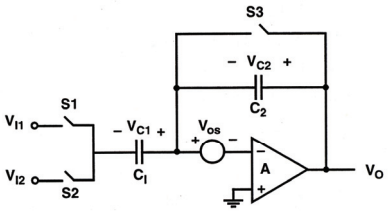


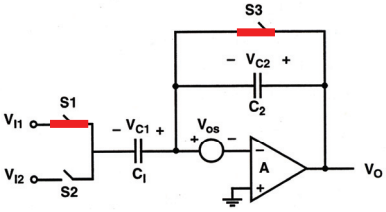

Hold/amplify mode (S1, S3 →off S2→ on)

→ Offset NOT cancelled, but not amplified
→ Input-referred offset $=(C_2/C_1) \times V_{OS}$, & often $C_2<C_1$



# T/H & Input Difference Amplifier

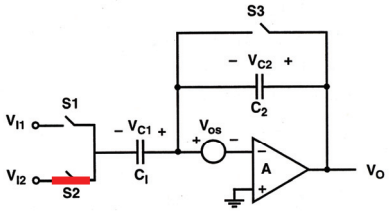



Sample mode:
(S1, S3 →on S2→ off)
$V_{C1}=V_{os} - V_{I1}$ , $V_{C2}=0$
$V_o=V_{os}$

# Input Difference Amplifier Cont'd

Subtract/Amplify mode (S1, S3 →off S2→ on)
During previous phase:
$V_{C1}=V_{os}-V_{I1}$ , $V_{C2}=0$
$V_o=V_{os}$




$$V_{C1} = V_{os} - V_{I2}$$

$$\Delta V_{C1} = (V_{os} - V_{I2}) - (V_{os} - V_{I1}) = V_{I1} - V_{I2}$$

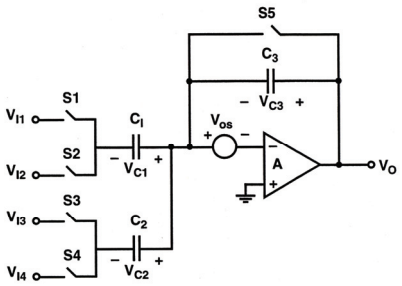
$$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right)\Delta V_{C1} = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2})$$

$$V_O = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2}) + V_{os}$$

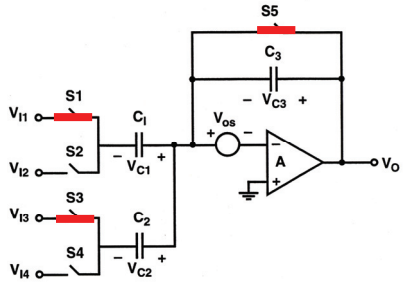
→Offset NOT cancelled, but not amplified
→Input-referred offset $=(C_2/C_1)xV_{OS}$, & $C_2<C_1$



# T/H & Summing Amplifier



# T/H & Summing Amplifier Cont'd




Sample mode (S1, S3, S5→on S2, S4→ off)

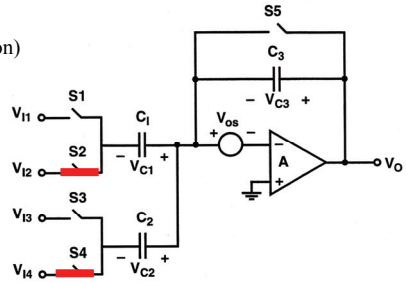
$V_{C1}=V_{os}-V_{I1}$ , $V_{C2}=V_{os}-V_{I3}$, $V_{C3}=0$

$V_o=V_{os}$



# T/H & Summing Amplifier Cont'd

Amplify mode (S1, S3, S5→off, S2, S4→ on)




$$V_{C1}=V_{os}-V_{I2} \Rightarrow \Delta V_{C1}=V_{I1}-V_{I2}$$

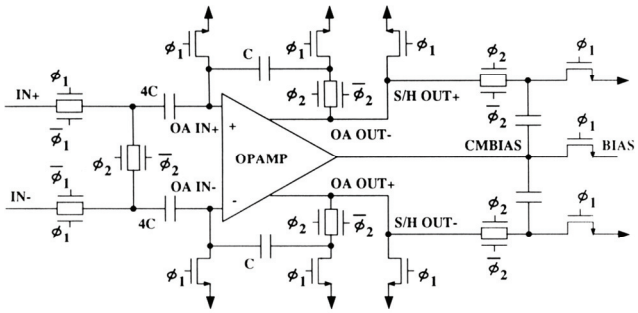
$$V_{C2}=V_{os}-V_{I4} \Rightarrow \Delta V_{C2}=V_{I3}-V_{I4}$$

$$\Delta Q_3=\Delta Q_1+\Delta Q_2=C_1\Delta V_{C1}+C_2\Delta V_{C2}$$

$$\Delta V_{C3}=\frac{\Delta Q_3}{C_3}=\left(\frac{C_1}{C_3}\right)(V_{I1}-V_{I2})+\left(\frac{C_2}{C_3}\right)(V_{I3}-V_{I4})$$

$$V_O=\left(\frac{C_1}{C_3}\right)(V_{I1}-V_{I2})+\left(\frac{C_2}{C_3}\right)(V_{I3}-V_{I4})+V_{os}$$

# Differential T/H Combined with Gain Stage

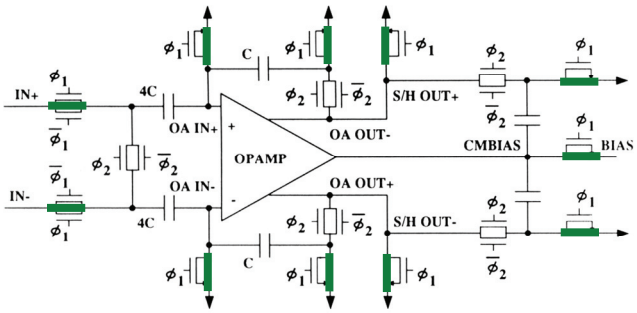



Employs the previously discussed technique to eliminate the problem associated with high common-mode voltage excursion at the input of the opamp

**Ref:** S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

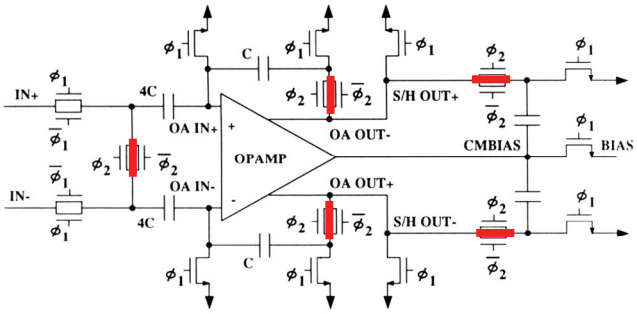


# Differential T/H Combined with Gain Stage
## $\phi 1 \rightarrow$ High




**Ref:** S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

# Differential T/H Combined with Gain Stage

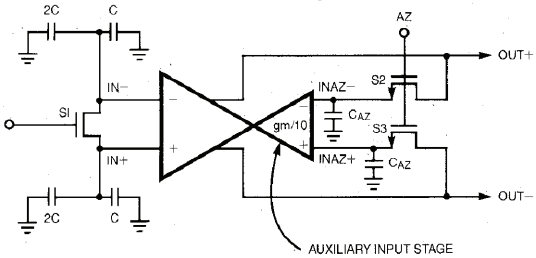



- *Gain=4C/C=4*
- Input voltage common-mode level removed → opamp can have low input common-mode compliance
- Amplifier offset NOT removed

**Ref:** S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987



# Differential T/H Including Offset Cancellation



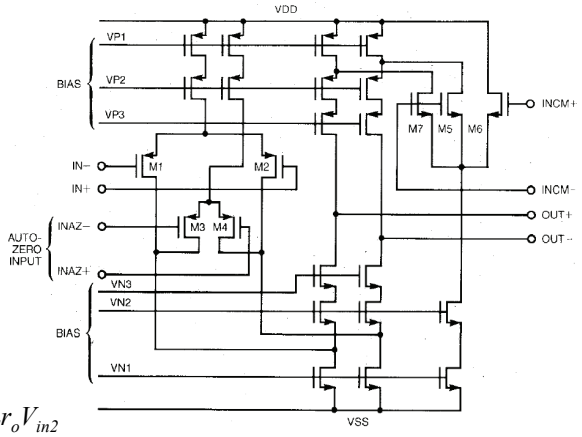

- Operation during offset cancellation phase shown
- Auxilary inputs added with $A_{main}/A_{aux}$.=10
- During offset cancellation phase:
  - Aux. amp configured in unity-gain mode: → offset stored on $C_{AZ}$ & canceled during the signal acquisition phase

**Ref:** H. Ohara, et al., "A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE Journal of Solid-State Circuits,* vol. 22, pp. 930 - 938, December 1987.

## Differential T/H Including Offset Cancellation Operational Amplifier

- Operational amplifier → dual input folded-cascode opamp
- M3,4 auxiliary input, M1,2 main input
- To achieve 1/10 gain ratio $W_{M3,4} = 1/10x\ W_{M1,2}$ & current sources are scaled by 1/10
- M5,6,7 → common-mode control
- Output stage → dual cascode → high DC gain

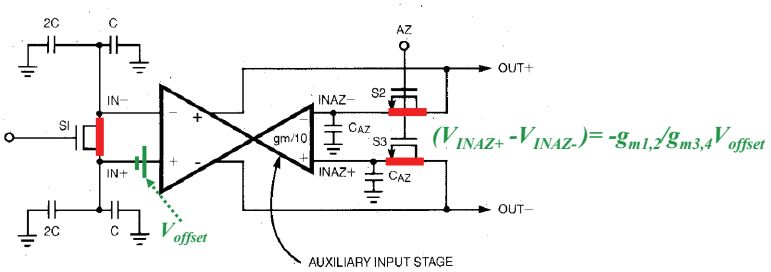
$$V_{out} = g_{m1,2} r_o V_{in1} + g_{m3,4} r_o V_{in2}$$




**Ref:** H. Ohara, et al., "A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE Journal of Solid-State Circuits,* vol. 22, pp. 930 - 938, December 1987.

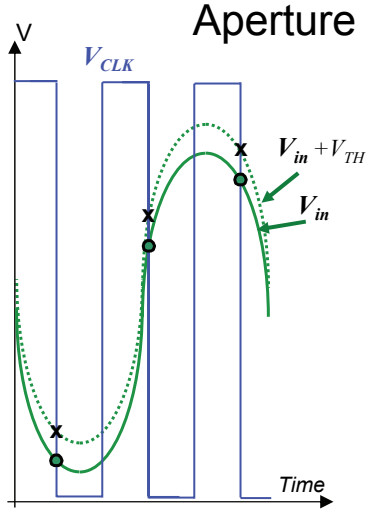


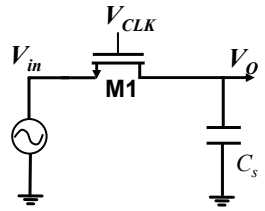
## Differential T/H Including Offset Cancellation Phase




- During offset cancellation phase AZ and S1 closed → main amplifier offset amplified by $g_{m1}/g_{m2}$ & stored on $C_{AZ}$
- Auxiliary amp chosen to have lower gain so that:
  - ❑ Aux. amp charge injection associated with opening of switch AZ → reduced by $A_{aux}/A_{main} = 1/10$
  - ❑ Insignificant increase in power dissipation resulting from addition of aux. inputs
- Requires an extra auto-zero clock phase

# Track & Hold
# Aperture Time Error



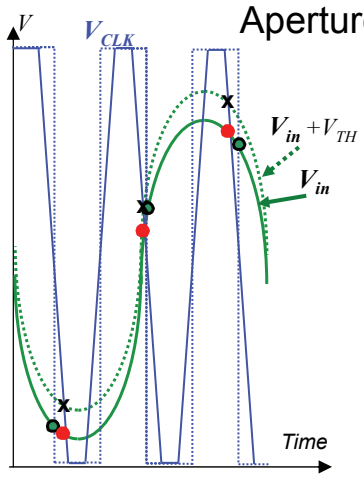




Transition from track to hold:
Occurs when device turns fully off
→ $V_{CLK}=V_{in}+V_{TH}$

Sharp fall-time wrt signal change
→ no aperture error



# Track & Hold
# Aperture Time Error




Slow falling clock → aperture error

$V_{in}=A\ sin(2\pi f_{in} t)$

$\varepsilon=f_{in} xAx\ \ t_{fall}\ /V_{CLK}$

$SDR= -20log\varepsilon - 4\ [dB]$ (imperical see Ref.)

Example:
Nyquist rate *10-bit ADC* & $A=V_{CLK}/4$
→*SQNR=62dB*
*for distortion due to aperture error < quant noise*
→ $t_{fall}< 2x10^{-3}/f_{in}$
→ *Worst case:* $f_{in}=f_s/2$
→ $t_{fall}< 4x10^{-3}/f_s$
→*e.g.* $f_s=1000MHz$, $t_{fall}<4psec$

Ref: P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitance," *IEEE Journal of Solid-State Circuits,* vol. 26, pp. 643 - 651, April 1991.

## Track & Hold
## Aperture Time Error

- Aperture error analysis applies to simple sampling network
- Bottom plate sampling → minimizes aperture error
- Boosted clock → reduces aperture error

  → Clock edge fall/rise trade-off between switch charge injection versus aperture error

Ref: P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitance," *IEEE Journal of Solid-State Circuits,* vol. 26, pp. 643 - 651, April 1991.



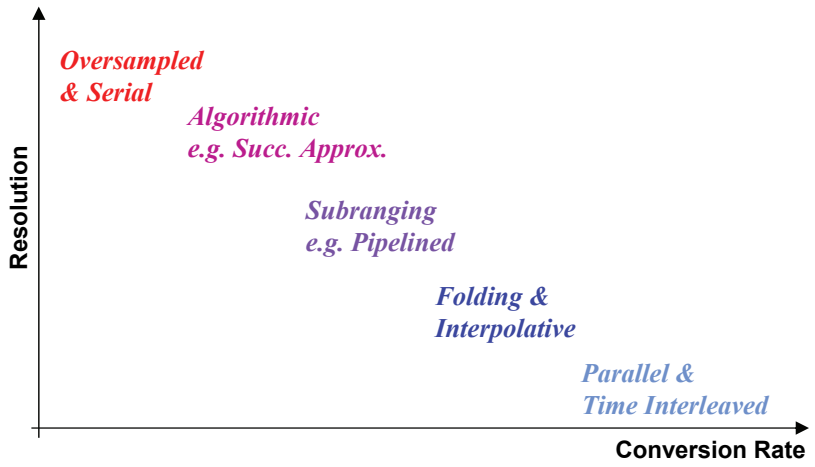
# ADC
# Architecture & Design

# ADC Architectures

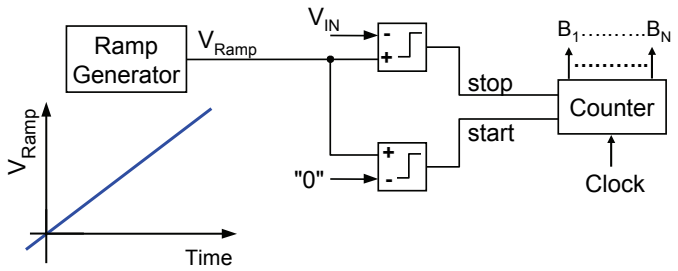
- Slope type converters
- Successive approximation
- Flash
- Time-interleaved / parallel converter
- Folding
- Residue type ADCs
  - Two-step
  - Pipeline
  - …
- Oversampled ADCs



## Various ADC Architectures Resolution/Conversion Rate



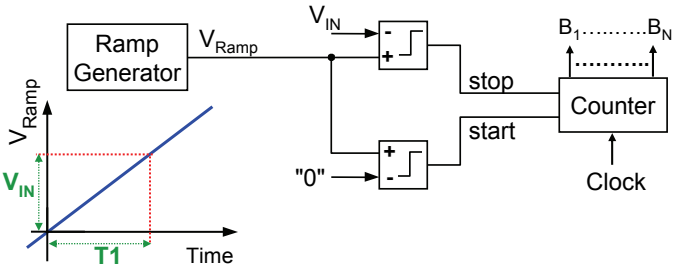
# Serial ADC
# Single Slope




- Counter starts counting @ $V_{Ramp}$=0
- Counter stops counting for $V_{IN}$=$V_{Ramp}$



# Serial ADC
# Single Slope



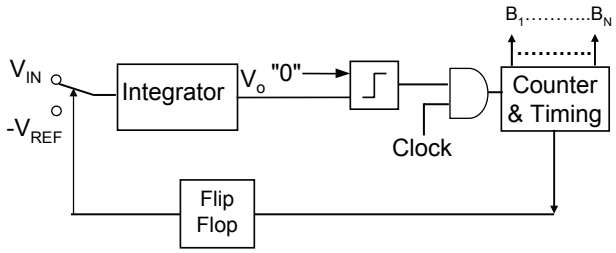

- Note that dt is proportional to $V_{IN}$
- Counter output proportional to $T1=nT_{clock}$
  - → Counter output proportional to $V_{IN}$
  - → $2^N x T_{clock} = V_{FS}$

# Single Slope ADC

- Advantages:
  - Low complexity & simple
  - INL depends on ramp linearity & not component matching
  - Inherently monotonic
- Disadvantages:
  - Slow ($2^N$ clock pulses for N-bit conversion) (e.g. N=16 $f_{clock}$=*1MHz* → needs *65000x1μs=65ms*/conversion)
  - Hard to generate precise ramp required for high resolution ADCs
  - Need to calibrate ramp slope versus $V_{IN}$
- Better: Dual Slope, Multi-Slope

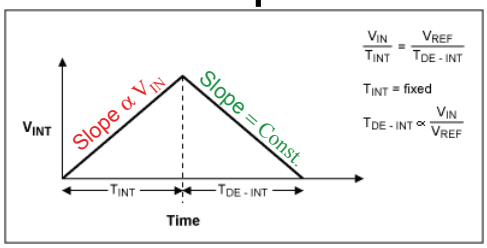


# Serial ADC
# Dual Slope




- First: $V_{IN}$ is integrated for a fixed time ($2^N x T_{CLK}$)
  → $V_o = 2^N x T_{CLK}\ V_{IN}/\tau_{intg}$
- Next: $V_o$ is de-integrated with $V_{REF}$ until $V_o$=0
  → Counter output = $2^N\ V_{IN}/V_{REF}$

# Dual Slope ADC




http://www.maxim-ic.com/appnotes.cfm/appnote_number/1041

- Integrate $V_{in}$ for fixed time ($T_{INT}$), de-integrate with $V_{REF}$ applied → $T_{De\text{-}Int} \sim 2^{N} x T_{CLK} x V_{in}/V_{REF}$
- Most laboratory DVMs use this type of ADC

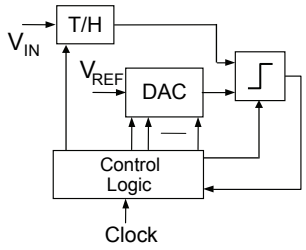


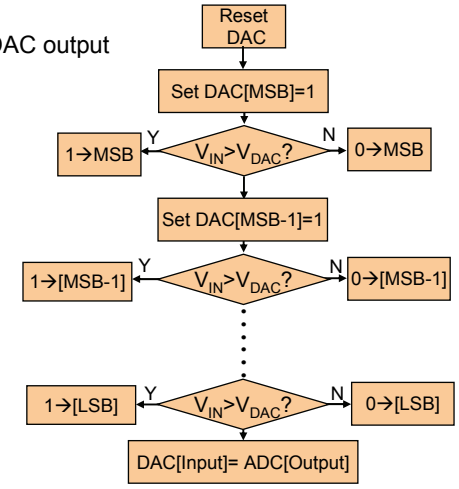
# Dual Slope ADC

- Advantage:
  - Accuracy to 1st order independent of integrator time-constant and clock period
  - Comparator offset referred to input is attenuated by integrator high DC gain
  - Insensitive to most linear error sources
  - DNL is a function of clock jitter
  - Power line (60Hz) xtalk effect on reading can be canceled by: choosing conversion time multiple of 1/60Hz
  - High accuracy achievable (16+bit)
- Disadvantage:
  - Slow (maximum $2x2^{N}xT_{clk}$ per conversion)
  - Integrator opamp offset results in ADC offset (can cancel)
  - Finite opamp gain gives rise to INL

# Successive Approximation ADC
# SAR

- Algorithmic type ADC
- Based on binary search over DAC output

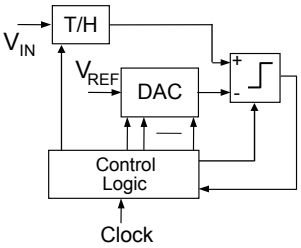


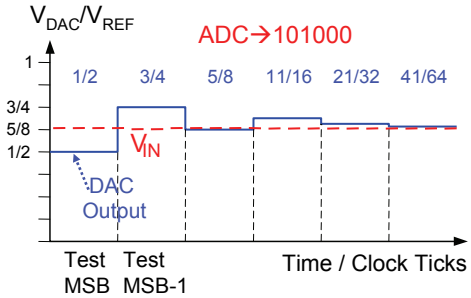






# Successive Approximation ADC

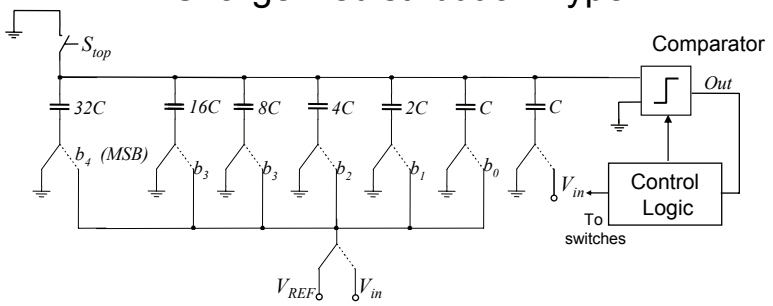
Example: 6-bit ADC & $V_{IN}=5/8V_{REF}$




- High accuracy achievable (16+ Bits)
- Required N clock cycles for N-bit conversion (much faster than slope type)
- Moderate speed (highest SAR conversion rate 2Ms/sec & 18bits)

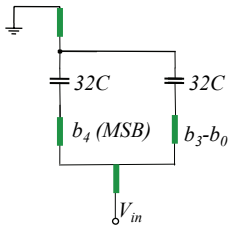
# Example: SAR ADC
# Charge Redistribution Type



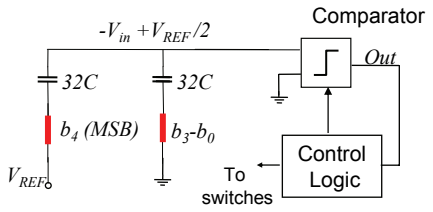

- Built with binary weighted capacitors, switches, comparator & control logic
- T/H inherent in DAC



# Charge Redistribution Type SAR DAC
# Operation: MSB



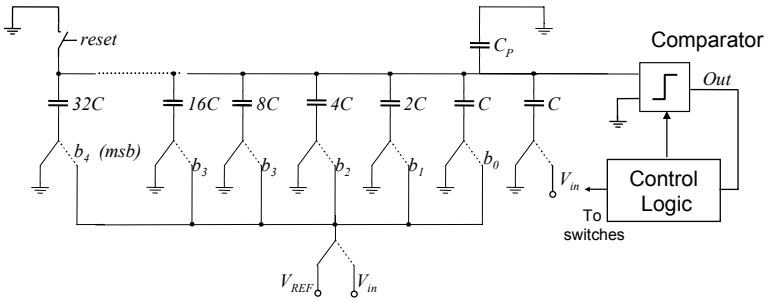

**Phase 1**




**Phase 2**

- Operation starts by connecting all top plate to gnd and all bottom plates to $V_{in}$
- To test the MSB all top plate are opened bottom plate of 32C connected to $V_{REF}$ & rest of bottom plates connected to ground → input to comparator= $-V_{in}+V_{REF}/2$
- Comparator is strobed to determine the polarity of input signal:
  - If negative MSB=1, else MSB=0
- The process continues until all bits are determined

# Example: SAR ADC
# Charge Redistribution Type



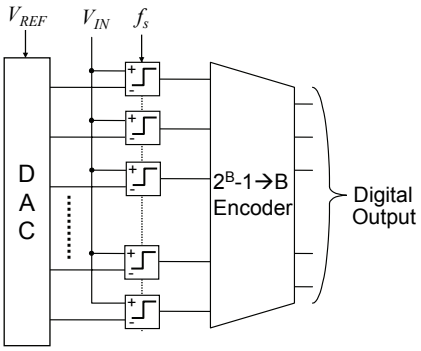

- To 1st order parasitic ($C_p$) insensitive since top plate driven from initial 0 to final 0 by the global negative feedback
- Linearity is a function of accuracy of C ratios
- Possible to add a C ratio calibration cycle (see Ref.)

Ref: H. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrating 15 bit CMOS A/D converter," *IEEE Journal of Solid-State Circuits,* vol. 19, pp. 813 - 819, December 1984.

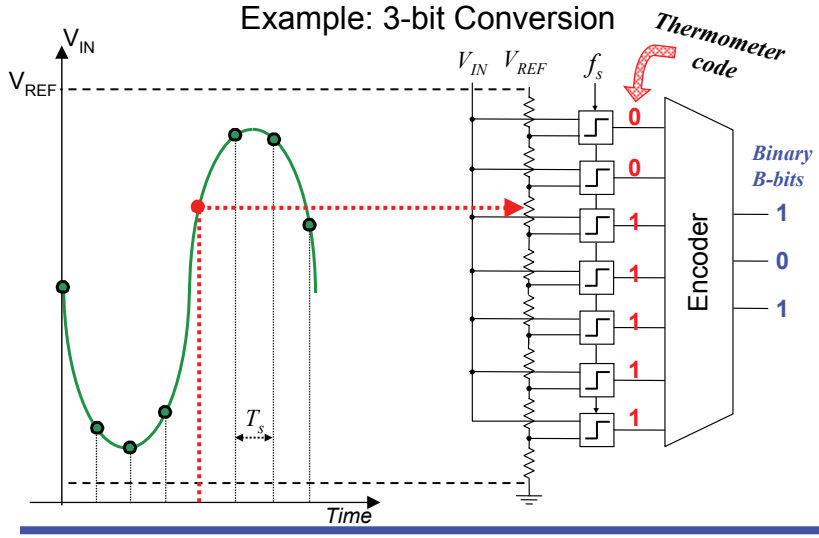


# Flash ADC

- B-bit flash ADC:
  - DAC generates all possible $2^B$ -1 levels
  - $2^B$-1 comparators compare $V_{IN}$ to DAC outputs
  - Comparator output:
    - If $V_{DAC} < V_{IN} \rightarrow 1$
    - If $V_{DAC} > V_{IN} \rightarrow 0$
  - Comparator outputs form thermometer code
  - Encoder converts thermometer to binary code
- Application example: 6-bit Flash ADC in Disk Drives with Gs/s conversion rate



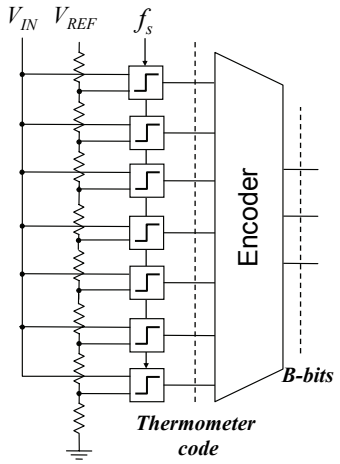
# Flash ADC Converter
## Example: 3-bit Conversion





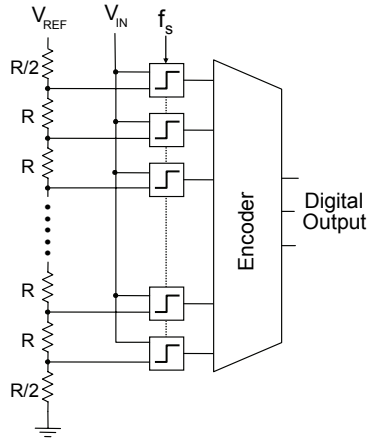

# Flash Converter Characteristics

- Very fast: only 1 clock cycle per conversion
  - ½ clock cycle→ $V_{IN}$ & $V_{DAC}$ comparison
  - ½ clock cycle→ $2^B$ -1 to B encoding
- High complexity: $2^B$-1 comparators
- Input capacitance of $2^B$-1 comparators connected to the input node:
  - → High capacitance @ input node



# Flash Converter
## Example: 8-bit ADC Design Considerations

- 8-bit→ 255 comparators
- $V_{REF}$=1V → 1LSB=4mV
- DNL<1/2LSB → Comparator input referred offset < 2mV
- Assuming close to 100% yield, 2mV =6$\sigma_{offset}$
  → $\sigma_{offset}$ < 0.33mV






# Flash ADC Converter
## Example: 8-bits ADC (continued)

→ $1\sigma_{Offset} < 0.33mV$

- Let us assume in the technology used:
  - Voffset-per-unit-sqrt(WxL)=$3\ mVx\ \mu$

$$V_{0\,ffset} = \frac{3mV}{\sqrt{W \times L}} = 0.33mV \quad \rightarrow W \times L = 83\mu^2$$

$$\text{Assuming: } C_{ox} = 9\,fF/\mu^2 \quad \rightarrow C_{GS} = \frac{2}{3} C_{ox} W \times L = 496\,fF$$

$$\rightarrow \text{Total max. input capacitance: } 255 \times 0.496 = 126.5\,pF!$$

  - Issues:
    - Si area quite large
    - Large ADC input capacitance
    - Since depending on input voltage level different number of comparator input transistors would be on/off- total input capacitance varies as input varies

    → Nonlinear input capacitance could give rise to signal distortion

Ref: M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits,* vol. 24, pp. 1433 - 1439, October 1989.

# Flash ADC Converter
## Example (continued)

Trade-offs:

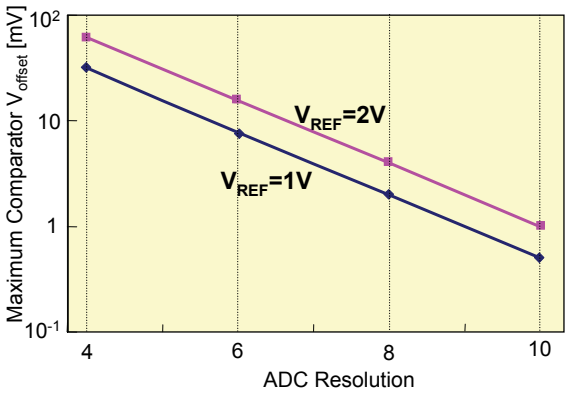
- Allowing larger DNL e.g. 1LSB instead of 0.5LSB:
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduces the input capacitance by a factor of 4!
- Reducing the ADC resolution by 1-bit
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduce the input capacitance by a factor of 4



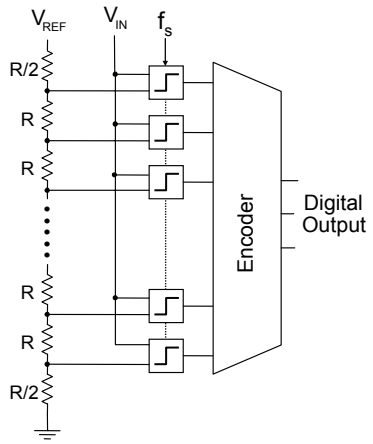
# Flash Converter
## Maximum Tolerable Comparator Offset versus ADC Resolution

Assumption:
*DNL=0.5LSB*

Note:
Graph shows max. tolerable offset, note that depending on min acceptable yield, the derived offset numbers are associated with $2\sigma$ to $6\sigma$ offset voltage



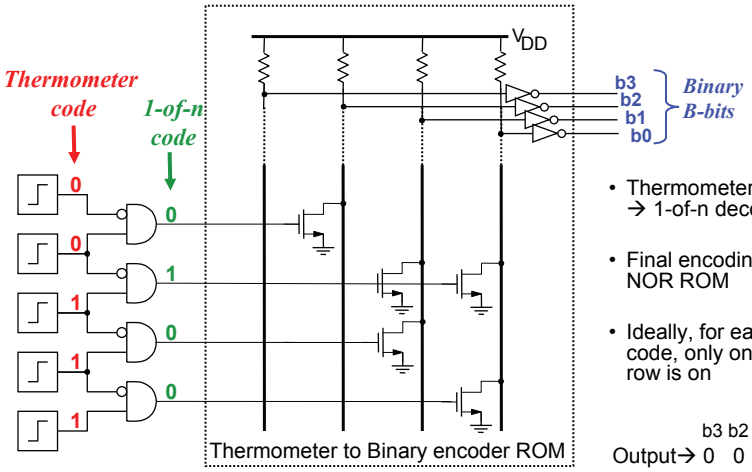
# Flash Converter Sources of Error




- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Feedthrough of input signal to reference ladder
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time
- Comparator output:
  - Sparkle codes (… 111101000 …)
  - Metastability



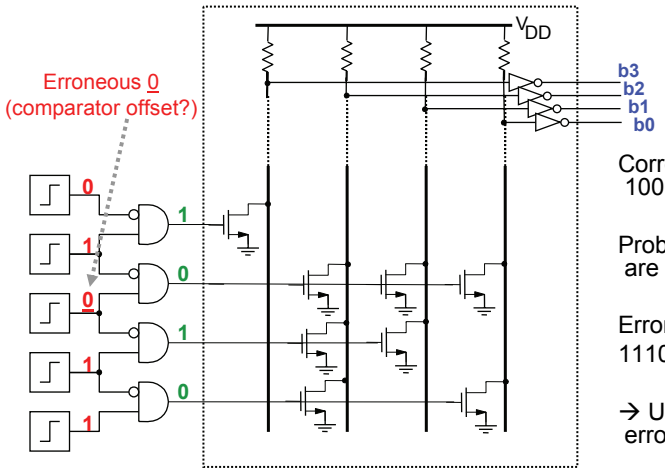
# Typical Flash Output Encoder




- Thermometer code → 1-of-n decoding
- Final encoding → NOR ROM
- Ideally, for each code, only one ROM row is on

| | b3 | b2 | b1 | b0 |
|---|---|---|---|---|
| Output→ | 0 | 0 | 1 | 1 |

# Sparkle Codes




Correct Output: 1000

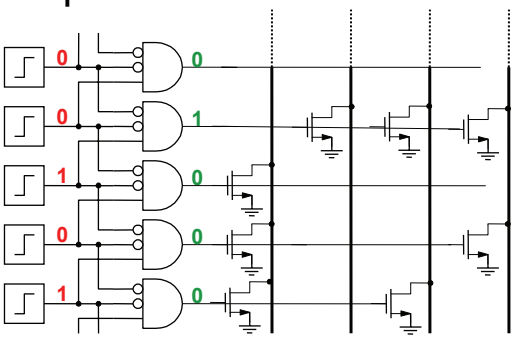
Problem: Two rows are on

Erroneous Output: 1110

→ Up to ~ ½ FS error!!



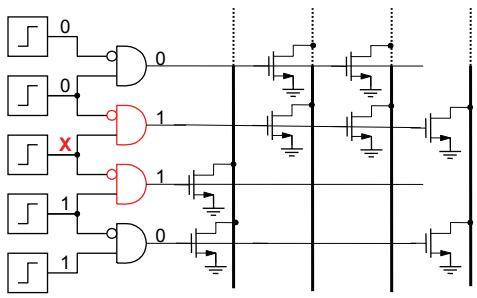
# Sparkle Tolerant Encoder




- Protects against a *single* sparkle.
- Possible to improve level of sparkle protection by increasing # of NAND gate inputs

Ref: C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," JSSC February 1990, pp. 997-1002

# Meta-Stability




Different gates interpret metastable output X differently

Correct output: 1000

Erroneous output: 0000

Solutions:
- –Latches (high power)
- –Gray encoding

Ref: C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," JSSC August 1996, pp. 1132-40



# Gray Encoding
## Example: 3bit ADC

| Thermometer Code | | | | | | | Gray | | | Binary | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $T_7$ | $T_6$ | $T_5$ | $T_4$ | $T_3$ | $T_2$ | $T_1$ | $G_3$ | $G_2$ | $G_1$ | $B_3$ | $B_2$ | $B_1$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

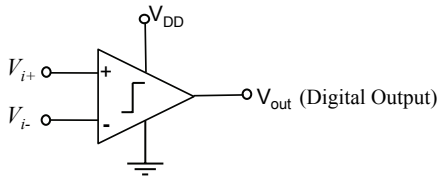
$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$

$$G_2 = T_2\overline{T_6}$$

$$G_3 = T_4$$

- Each $T_i$ affects only one $G_i$
  → Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder

# Voltage Comparators




Play an important role in majority of ADCs

Function: Compare the instantaneous value of two analog signals & generate a digital output voltage based on the sign of the difference:

$$\text{If } V_{i+} - V_{i-} > 0 \rightarrow V_{out} = \text{“}1\text{”}$$
$$\text{If } V_{i+} - V_{i-} < 0 \rightarrow V_{out} = \text{“}0\text{”}$$



# Voltage Comparator Architectures

## Comparator architectures:

- High gain amplifier with differential analog input & single-ended large swing output
  - Output swing has to be compatible with driving digital logic circuits
  - Open-loop amplification→ no frequency compensation required
  - Precise gain not required
- Latched comparators; in response to a strobe (clock edge), input stage disabled & digital output stored in a latch till next strobe
  - Two options for implementation :
    - Latch-only comparator
    - Low-gain preamplifier + high-sensitivity latch
- Sampled-data comparators
  - T/H input
  - Offset cancellation