Administrative

• Project:
  – Discussions & report submission on Frid. Dec. 4th
    (make appointment via sign-up sheet)
  – Student presentations Dec. 3rd & Dec. 8th

• Office hours @ 567 Cory:
  – Tues. Dec. 8th, 4 to 5pm
  – Wed. Dec. 9th, 10 to 11am

• Questions can also be asked via email

EE247
Lecture 26

• Bandpass ΣΔ modulators

• ADC figures of merit

• Term project student presentations

• Examples of systems utilizing analog-digital interface circuitry (not part of final exam)

• Acknowledgements
Bandpass ΔΣ Modulator

- Replace the integrator in 1st order lowpass ΣΔ with a resonator
  → 2nd order bandpass ΣΔ

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Bandpass ΔΣ Modulator

Example: 6th Order

Measured output for a bandpass ΣΔ (prior to digital filtering)

**Key Point:**

NTF → notch type shape

STF → bandpass shape

Ref:
Paolo Cusinato, et. al, “A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range”, IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001
Bandpass $\Sigma\Delta$ Characteristics

- Oversampling ratio defined as $f_s / 2B$ where $B$ = signal bandwidth

- Typically, sampling frequency is chosen to be $f_s = 4f_{\text{center}}$ where $f_{\text{center}}$ is bandpass filter center frequency

- STF has a bandpass shape while NTF has a notch or band-reject shape

- To achieve same resolution as lowpass, need twice as many integrators

Bandpass $\Sigma\Delta$ Modulator Dynamic Range As a Function of Modulator Order (K)

- Bandpass $\Sigma\Delta$ resolution for order $K$ is the same as lowpass $\Sigma\Delta$ resolution with order $L = K/2$
Example: Sixth-Order Bandpass $\Sigma\Delta$ Modulator

**Simulated noise transfer function**

**Simulated signal transfer function**

Ref:
Paolo Cusinato, et al, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range", IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001

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**Features & Measured Performance**

- Analog input full-scale: 4.4V (differential)
- Sampling frequency ($f_s$): 42.8MHz
- Center frequency ($f_c$): 10.7MHz
- Signal bandwidth: 200kHz
- OSR: 107
- Dynamic range: 74dB (200kHz band), 88dB (9kHz band)
- Peak SNDR: 61dB
- IMD (-15dB): 71dBc
- Active die area: 1mm²
- Power supply: 3.3V
- Power consumption: 76mW (adaptive biasing), 126mW (standard biasing)

Ref:
Paolo Cusinato, et al, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range", IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001
Summary
Oversampled ADCs

- Noise shaping utilized to reduce baseband quantization noise power
- Reduced precision requirement for analog building blocks compared to Nyquist rate converters
- Relaxed transition band requirements for analog anti-aliasing filters due to oversampling
- Takes advantage of low cost, low power digital filtering
- Speed is traded for resolution
- Typically used for lower frequency applications compared to Nyquist rate ADCs

ADC Figures of Merit

- Objective: Want to compare performance of different ADCs
- Can use FOM to combine several performance metrics to get one single number
- What are reasonable FOM for ADCs?
ADC Figures of Merit

\[ FOM_1 = f_s \cdot 2^{ENOB} \]

- This FOM suggests that adding a bit to an ADC is just as hard as doubling its bandwidth

- Is this a good assumption?


Survey Data

ADC Figures of Merit

$$FOM_2 = \frac{Power}{f_s \cdot 2^{ENOB}} \quad [J/\text{conv}]$$

- Sometimes inverse of this metric is used
- In typical circuits power ~ speed, $FOM_2$ captures this tradeoff correctly
- How about power vs. ENOB?
  - One more bit 2x in power?


ADC Figures of Merit

- One more bit means...
  - 6dB SNR, 4x less noise power, 4x larger $C$
  - Power ~ $Gm$ ~ $C$ increases 4x
- Even worse: Flash ADC
  - Extra bit means 2x number of comparators
  - Each of them needs double precision
  - Transistor area 4x, Current 4x to keep same current density
  - Net result: Power increases 8x
ADC Figures of Merit

- \( FOM_2 \) seems not quite appropriate, but somehow still standard in literature, papers
- "Tends to work" because:
  - Not all power in an ADC is "noise limited"
  - E.g. Digital power, biasing circuits, etc.
- Avoid comparing different resolution ADCs using \( FOM_2 \)!

\[ FOM_3 = \frac{Power}{Speed} \]

- Compare only power of ADCs with approximately same ENOB
- Useful numbers:
  - 10b (~9 ENOB) ADCs: 1 mW/MSample/sec
    Note the ISSCC 05 example: 0.33mW/MS/sec!
  - 12b (~11 ENOB) ADCs: 4 mW/MSample/sec
10-Bit ADC Power/Speed

Yoshioko ISSCC 05

12-Bit ADC Power/Speed

Loloee (ESSIRC 2002)
Material Covered in EE247

• Filters
  – Continuous-time filters
    • Biquads & ladder type filters
    • Opamp-RC, Opamp-MOSFET-C, gm-C filters
    • Automatic frequency tuning
  – Switched capacitor (SC) filters

• Data Converters
  – D/A converter architectures
  – A/D converter
    • Nyquist rate ADC- Flash, Interpolating & Folding, Pipeline ADCs,….
    • Self-calibration techniques
    • Oversampled converters

E.E. Circuit Courses
vs. Frequency Range

RF Band
500kHz
100GHz

IF Band
455kHz
10.7MHz
80MHz
100MHz

AM Radio
FM Radio
Cellular Phone

Baseband
DC
500MHz

EE240, EE247

EE242
Systems Including Analog-Digital Interface Circuitry
(Not Included in Final Exam)

- Wireline communications
  - Telephone related (DSL, ISDN, CODEC)
  - Television circuitry (Cable modems, TV tuners…)
  - Ethernet (10/1Gigabit, 10/100BaseT…)
- Wireless
  - Cellular telephone (CDMA, Analog, GSM…)
  - Wireless LAN (Blue tooth, 802.11a/b/g…)
  - Radio (analog & digital), Television
- Disk drives
- Fiber-optic systems

Wireline Communications
Telephone Based
Data Transmission Over Existing Twisted-Pair Phone Lines

- Data transmitted over existing phone lines (originally meant to carry 4kHz voice grade signal) covering distances close to 3.5 miles
  - Voice-band MODEMs (up to 56Kb/s)
  - ISDN (160Kb/s)
  - HDSL, SDSL,……
  - ADSL (up to 8Mb/s)

Data Transmission Over Twisted-Pair Phone Lines
ISDN (U-Interface) Transceiver

- Full duplex transmission (RX & TX signals sent simultaneously)
- 160kbit/sec baseband data (80kHz signal bandwidth)
- Standardized line code 2B1Q (4 level code 3:1:-1:-3)
- Max. desired loop coverage 18kft (~36dB signal attenuation)
- Final required BER (bit-error-rate) $10^{-7}$ $\rightarrow$ (min. SNDR=27dB)
ISDN (U-Interface) Transceiver

Echo Problem

- Transformer coupling to line
  - For a perfectly matched system → no leakage of TX signal into RX path
  - Unfortunately, system has poor matching + complicating factor of bridged-taps

- System full duplex transmission → RX & TX signals sent simultaneous (& at the same frequency band)
  - Leakage of TX signal to RX path (echo)
  - Worst case → echo could be \(30\,\text{dB}\) higher compared to the received signal!!
**ISDN (U-Interface) Transceiver**

**Echo Cancellation**

- Echo cancellation performed in the digital domain
  - Typically echo cancellation performed by transversal adaptive digital filter
  - Any non-linearity incurred by the analog circuitry makes echo canceller significantly more complex
  - Desirable to have high linearity analog circuitry (75dB range)

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**Simplified Transceiver Block Diagram**

- **CMA** → Control, maintenance & access unit
- **DFE** → Decision feedback equalizer
- **DEC** → Decimation filter
- **REC** → Reconstruction filter
- **LEC & NEC** → Linear/non-linear echo-canceller

To avoid stringent requirements for non-linear echo canceller:
→ high linearity analog circuitry needed (~ 75dB)

Data Transmission Over Twisted-Pair Phone Lines
DSL (Digital Subscriber Loop)

• HDSL & SDSL more like ISDN @ higher frequencies
  – Full duplex transmission with RX & TX signals on the same frequency band
Data Transmission Over Twisted-Pair Phone Lines

ADSL (Asymmetric Digital Subscriber Loop)

- In USA mostly ADSL → FDM (frequency division multiplex)
  - Signal from CO to customer on a different frequency band compared to customer to CO
    - Echo cancellation can be performed by simple filtering
  - Data rates up to 8Mbps (much higher compared to ISDN)

ADSL Signal Characteristics

- Main difference compared to ISDN: TX & RX signals on different frequency bands
  - Downstream (fast, from CO to customer) 138kHz to 1.1MHz
  - Upstream (slow, from customer to CO) 30kHz to 138kHz
    - Echo cancellation much easier
- More severe signal attenuation at high frequencies (1MHz DSL v.s. 80kHz ISDN)
Typical ADSL Analog Front-End

- ADC 16/14b with 14bit linearity, pipelined with auto. calibration @ 5Ms/s
- DAC 16/14b with 14bit linearity, with auto. calibration
- On-chip filters 3rd to 4th order LPF with $f_c = 1.1\text{MHz}$ for downstream and 138kHz upstream (typically continuous-time type filters with on-chip frequency tuning)


Note: Band selection filters are off-chip due to stringent noise requirements (3nV/√Hz)
- Discrete LC type
- Line driver on a separate bipolar chip to achieve required high output signal levels with high power efficiency typically +-12V supply
Wireless Communication Circuits

• Differ from wired comm. circuits
  – Includes RF circuitry + IF circuitry + baseband circuits (three different frequency ranges)
  – Signal scenarios in wireless receivers more challenging
  – Requirement for received signal BER in the order of $10^{-3}$ for voice-only $\rightarrow$ (min. SNR~9dB)
Typical Cellular Phone Block Diagram

Superheterodyne Receiver

- One or more intermediate frequency (IF)
- Periodic signal at a frequency equal to the desired RX signal + or – IF frequency is provided by a Local Oscillator
- RX signal is frequency shifted to a fixed frequency (IF filter center frequency)
RF Superheterodyne Receiver
Example: CDMA Receiver

- Received frequency is mixed down to a fixed IF frequency and then filtered with a bandpass filter

Why Image Reject Filter?

- Any signal at the image frequency of the RX signal with respect to Osc. frequency will fall on the desired RX signal and cause impairment
Why Image Reject Filter?

- Image reject filter attenuates signals out of the RX band
- Typically, image reject filters are ceramic or LC type filters

Quadrature Downconversion

- In systems with phase or freq. modulation, since signal is not symmetric around $f_{IF}$, directly converting down to baseband corrupts the sidebands
- Quadrature downconversion overcomes this problem
- Thus requiring two sets of baseband filters & ADCs
Effect of Adjacent Channels

• Adjacent channels can be as much as 60dB higher compared to the desired RX signal!
• Linearity of stages prior and including channel selection filters extremely important

Effect of Adjacent Channels

• Due to existence of large unwanted signals & limited dynamic range for the front-end circuitry:
  – Can not amplify the signal up front due to linearity issues
  – Need to allocate amplification/filtering specifications to RX blocks carefully
  – Can only amplify when unwanted signals are filtered adequately
  – System design critical with respect to tradeoffs affecting:
    • Gain
    • Linearity
    • Power dissipation
    • Chip area
Homodyne (Direct to Baseband) Receivers

- No intermediate frequency, signal mixed directly down to baseband
- Almost all of the filtering performed at baseband
  - Higher levels of integration possible
  - Issue to be aware of:
    - Requirements for the baseband filters more stringent
    - Since the local oscillator frequency is exactly at the same freq. as the RX signal freq., can cause major DC offsets & drive the receiver front-end into non-linear region

Example: Wireless LAN 802.11b & Bluetooth

Digital IF Receiver (IF sampling)

- IF signal is converted to digital → most of signal processing performed in the digital domain
- Performance requirement for ADC more demanding in terms of noise, linearity, and dynamic range!
- With advancements of ADCs could be the architecture of choice in the future

Typical Wireless Transmitter

- Transmit signal shipped from DSP to the analog front-end in the form of I& Q signals
- Signal converted to analog form by D/A
- Lowpass filter provides signal shaping
- In-phase & Quad. Components combined and then mixed up to RF
- Power amplifier amplifies and provides the low-impedance output
Analog Filters in Super-Heterodyne Wireless Transceivers

<table>
<thead>
<tr>
<th>Filters</th>
<th>Function</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Filter</td>
<td>Image Rejection</td>
<td>Ceramic or LC</td>
</tr>
<tr>
<td>IF Filter</td>
<td>Channel selection</td>
<td>SAW</td>
</tr>
<tr>
<td>Base-band Filters</td>
<td>Channel Selection &amp; Anti-aliasing for ADC</td>
<td>Integrated Cont.-Time or S.C.</td>
</tr>
</tbody>
</table>

Example: Dual Mode CDMA (IS95) & Analog Cellular Phone
Example: Dual Mode CDMA (IS95)& Analog Cellular Phone

• Typical baseband analog circuitry includes:
  – CDMA
    • 4bit flash type ADC clock rate 10MHz
    • 8bit segmented TX DAC clock rate 10MHz (shared with FM)
    • 7th order elliptic RX lowpass filter corner freq. 650kHz
    • 3rd order chebyshev TX lowpass filter corner freq. 650kHz
  – FM (analog)
    • 8bit successive approximation ADCs clock rate 360kHz
    • 5th order chebyshev RX lowpass filter corner frequency 14kHz
    • 3rd order butterworth TX lowpass filter corner frequency 27kHz

Summary

• Examples of systems utilizing challenging analog to digital interface circuitry- in the area of wireline & wireless systems discussed

• Analog circuits still remain the interface connecting the digital world to the real world!
Acknowledgements

• The course notes for EE247 are based on numerous sources including:
  – Prof. P. Gray’s EE290 course
  – Prof. B. Boser’s EE247 course notes
  – Prof. B. Murmann’s Nyquist ADC notes
  – Fall 2004 thru 2008 EE247 class feedback
  – Last but not least, Fall 2009 EE247 class
    • The instructor would like to thank the class of 2009 for their enthusiastic & active participation!