

### Anodic Bonding

- Bonds an electron conducting material (e.g., Si) to an ion conducting material (e.g., sodium glass = Pyrex)
- Procedure/Mechanism:
  - Press Si and glass together
  - Elevate temperature: 180-500°C
  - Apply (+) voltage to Si: 200-1500V
    - (+) voltage repels Na<sup>+</sup> ions from the glass surface
    - Get net (-) charge at glass surface
    - Attractive force between (+) Si and (-) glass → intimate contact allows fusing at elevated temp.
  - Current drops to zero when bonding is complete

The diagram shows a cross-section of a silicon wafer being bonded to a glass substrate. A metal plate is on top of the silicon. A voltage source is connected between the metal plate and the glass. Handwritten notes include "Strong attractive force" with arrows pointing to the interface, "Na<sup>+</sup>" ions being repelled, and "Fusion Bonding" at the interface. The graphs show:
 

- Temperature:** Starts at 25°C, rises to 450°C, then levels off. A note says "Elevated temperature (low glass becomes slightly conducting)".
- Pressure:** Starts at 0, rises to 1000 mbar, then levels off. A note says "Low pressure bonding".
- Voltage:** Starts at 0, rises to 1000 V, then levels off. A note says "High voltage along electrical field pulls the surface into intimate contact".
- Current:** Starts at 10 mA, drops to 1 mA, then levels off. A note says "Current nullification".

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### Anodic Bonding (cont.)

- Advantage:** high pressure of electrostatic attraction smoothes out defects
- Below:** 100 mm wafers, Pyrex glass 500 μm-thick, 430°C, 800V, N<sub>2</sub> @ 1000 mbar

The four images show the progression of anodic bonding on a wafer:
 

1. after 5 sec: Only center bond pin active
2. after 20 sec: All bond pins active
3. after 2.5 min: Bond front spreads
4. after 8 min: Bond 98% completed

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### Metal Layer Bonding

- Pattern seal rings and bond pads photolithographically
- Eutectic bonding**
  - Uses eutectic point in metal-Si phase diagrams to form silicides
  - Au and Si have eutectic point at 363°C
  - Low temperature process
  - Can bond slightly rough surfaces
  - Issue:** Au contamination of CMOS
- Solder bonding**
  - PbSn (183°C), AuSn (280°C)
  - Lower-T process
  - Can bond very rough surfaces
  - Issue:** outgassing (not good for encapsulation)
- Thermocompression**
  - Commonly done with electroplated Au or other soft metals
  - Room temperature to 300°C
  - Lowest-T process
  - Can bond rough surfaces with topography

The diagrams show cross-sections of different bonding methods:
 

- Eutectic bonding:** Shows a metal layer (Au) bonding to a silicon substrate. A note says "cut".
- Solder bonding:** Shows a solder layer (PbSn) bonding to a silicon substrate. A note says "cut".
- Thermocompression:** Shows a metal layer (Au) bonding to a silicon substrate. A note says "cut".

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### Thermocompression Bonding

- Below:** Transfer of hexsil actuator onto CMOS wafer

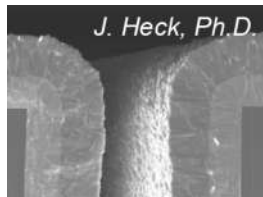
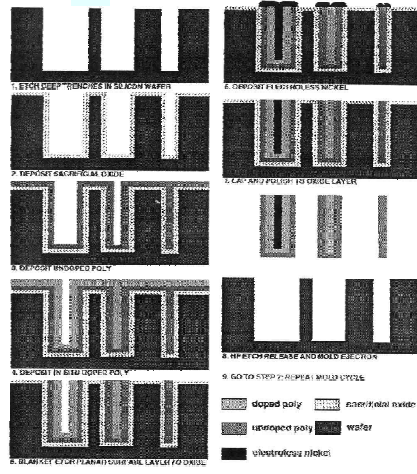
The SEM image shows a hexsil actuator transferred onto a CMOS wafer. The actuator is a circular structure with a central pad. The CMOS wafer has a grid of bond pads. The actuator is bonded to the wafer. The image is labeled "20KV X200 0007 100.0U MS".

[Singh, et al, Transducers'97]

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### Hexsil MEMS

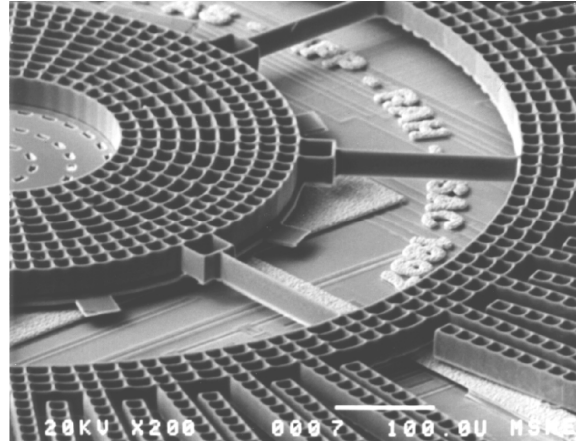
- Achieves high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Design with honeycomb structure for strength

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### Hexsil MEMS Actuator

- Below: Transfer of hexsil actuator onto CMOS wafer

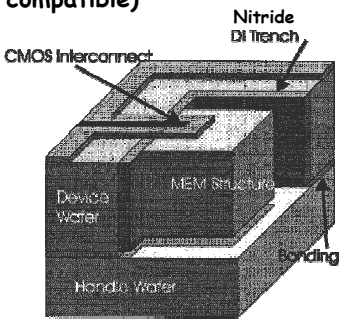
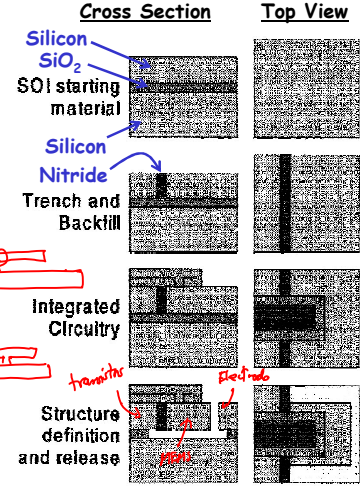


[Singh, et al, Transducers'97]

EE C245: Introduction to MEMS Design LecM 6 C. Nguyen 9/28/07 42

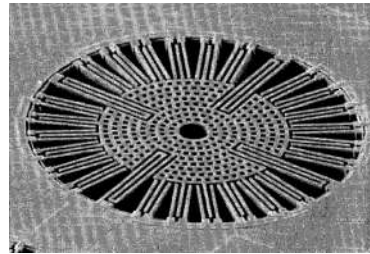
### Silicon-on-Insulator (SOI) MEMS

- No bonding required
- Si mechanical structures anchored by oxide pedestals
- Rest of the silicon can be used for transistors (i.e., CMOS compatible)

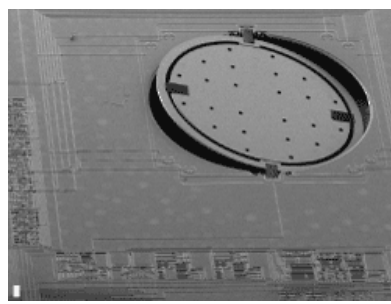



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### SOI MEMS Examples



[Brosnihan]

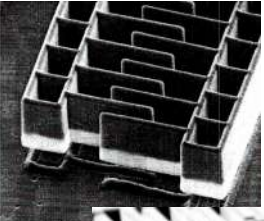
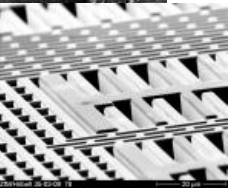


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**The SCREAM Process**

UC Berkeley

- **SCREAM: Single Crystal Reactive Etching and Metallization process**

1. Deposit oxide and photoresist

2. Lithography and oxide etch

3. Silicon etch

4. Coat sidewalls with PECVD oxide

5. Remove oxide at bottom and etch silicon

6. Plasma etch in BE, suspended to release structures

Labels in diagram: Photoresist, Oxide, Silicon substrate, Suspended beam, Electrode/Probe, Sharp tip.

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