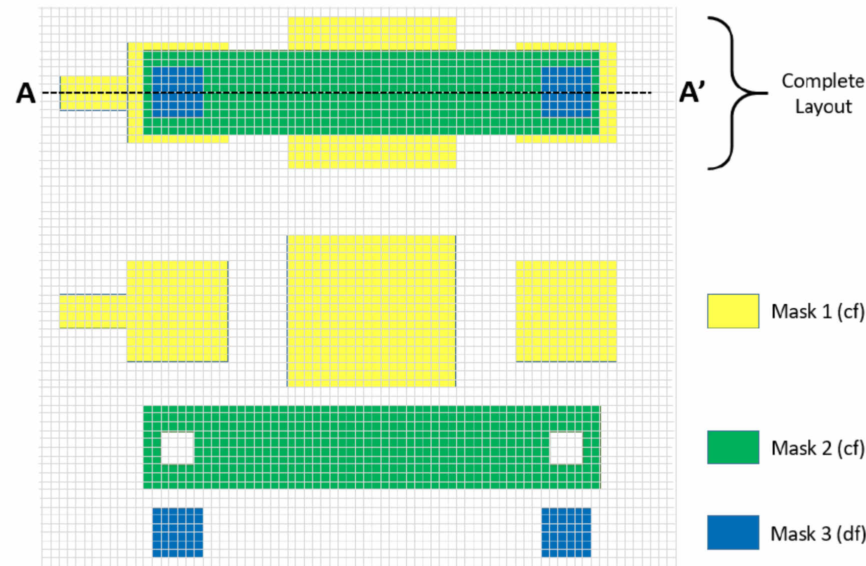
EE 247B / ME 218 Discussion 5

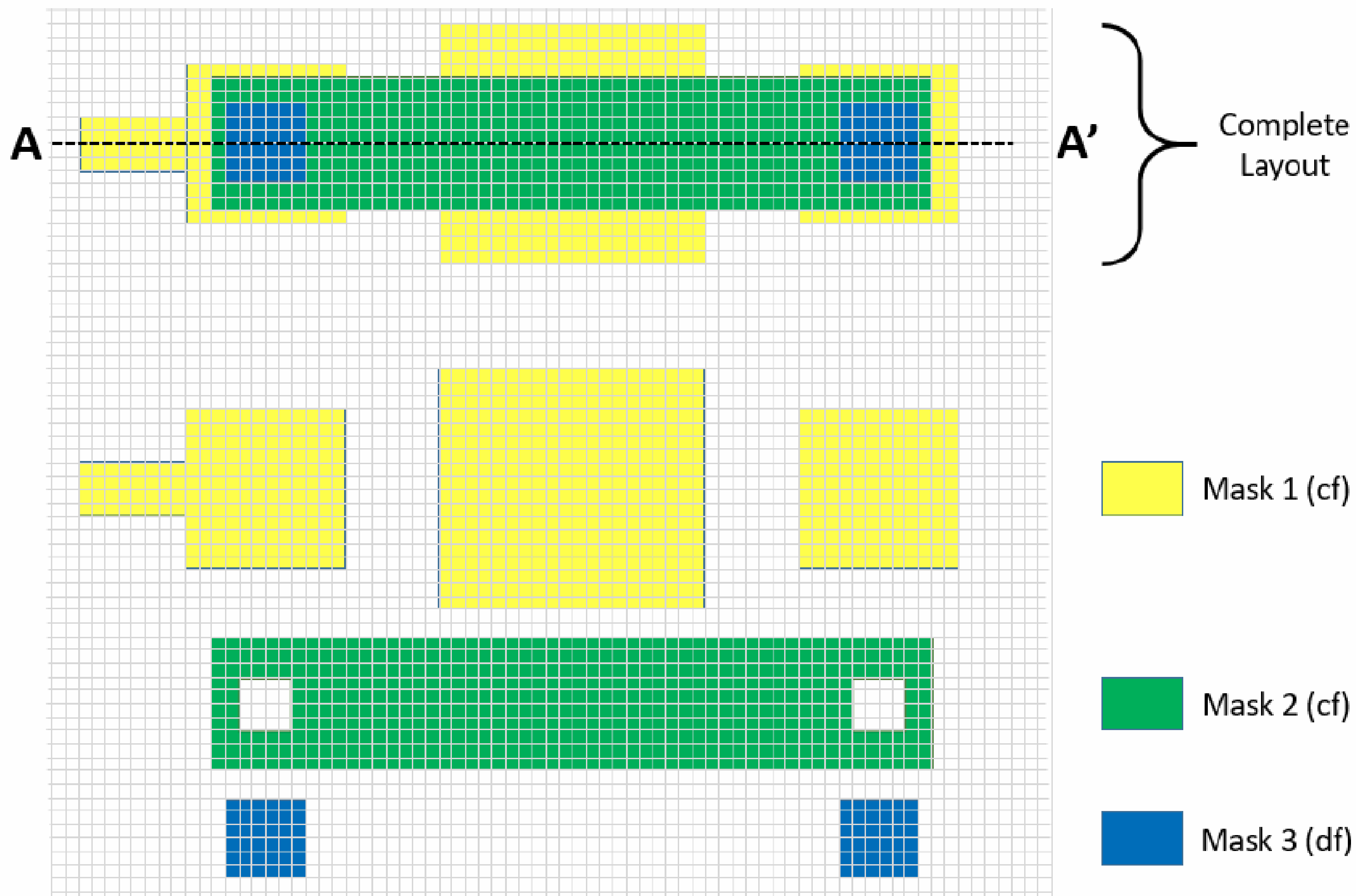
Kieran Peleaux

Example Process Flow

You are given the layout below along with the process traveler to follow. In the layout each box corresponds to 1µm2. In the mask legend, cf = “clear field” and df = “dark field”. In the process traveler, assume that all lithography steps use positive photoresist, except when otherwise indicated, and that all etch steps are 100% selective to intended film. Also, assume that RIE etches are anisotropic, but any other type of etch has some degree of isotropy. Follow the instructions after the process traveler.



Layout



Process Traveler

i. Deposit 2μm of LTO via LPCVD.
ii. Deposit 500nm of silicon rich nitride via LPCVD
iii. Deposit 300nm of *in situ*-phosphorus-doped polycrystalline silicon via LPCVD at 610°C.
iv. Lithography via Mask 1.
v. Etch polysilicon via RIE and stop on nitride.
vi. Remove photoresist.
vii. Deposit 500nm of LTO via LPCVD.
viii. Deposit 2μm of *in situ*-phosphorus-doped polycrystalline silicon via LPCVD at 610°C.
ix. Deposit 2μm of LTO via LPCVD.
x. Lithography via Mask 2.
xi. Etch oxide via RIE and stop on polysilicon.
xii. Etch polysilicon via RIE and stop on oxide.
xiii. Remove photoresist.
xiv. Lithography via Mask 3.
xv. Etch oxide via RIE and stop when the etch reaches polysilicon or nitride on the substrate.
xvi. Remove photoresist.
xvii. Deposit 3μm of *in situ*-phosphorus-doped polycrystalline silicon via LPCVD at 610°C.
xviii. CMP the polysilicon and stop on oxide.
xix. Lithography via Mask 3 using a negative resist.
xx. Etch polysilicon via RIE and stop on oxide.
xxi. Remove photoresist.
xxii. Dip in HF until structures are fully released.