PROBLEM SET #2

Issued: Tuesday, February 11, 2020

Due: Tuesday, February 25, 2020, 8:00 am via Gradescope

1. The cross-section shown in Fig. PS2.1 below is to be etched via reactive ion etching (RIE). For this problem, assume that the RIE etch is 100% anisotropic with a polysilicon etch rate of 1 μm/min, a silicon-to-oxide selectivity of 5:1 and a silicon-to-photoresist selectivity of 2:1. Draw cross-sections of the structure after etching for:

(a) 2 minutes

(b) 5 minutes

(c) 6 minutes

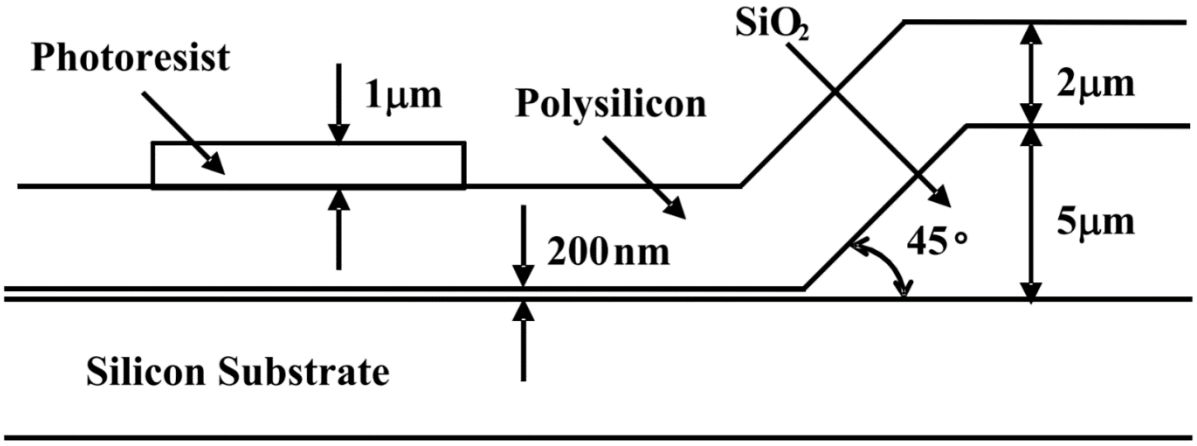

Figure PS2.1

2. Consider a silicon wafer covered with a thick film of phosphosilicate glass (PSG) that has a phosphorous concentration much greater than the solid solubility limit of phosphorous in silicon. The wafer has an initial background dopant concentration of $N_A = 2 \times 10^{15}$ cm^{-3}. The wafer is to be placed in an annealing furnace and heated for one hour according to the temperature function given in Fig. PS2.2.

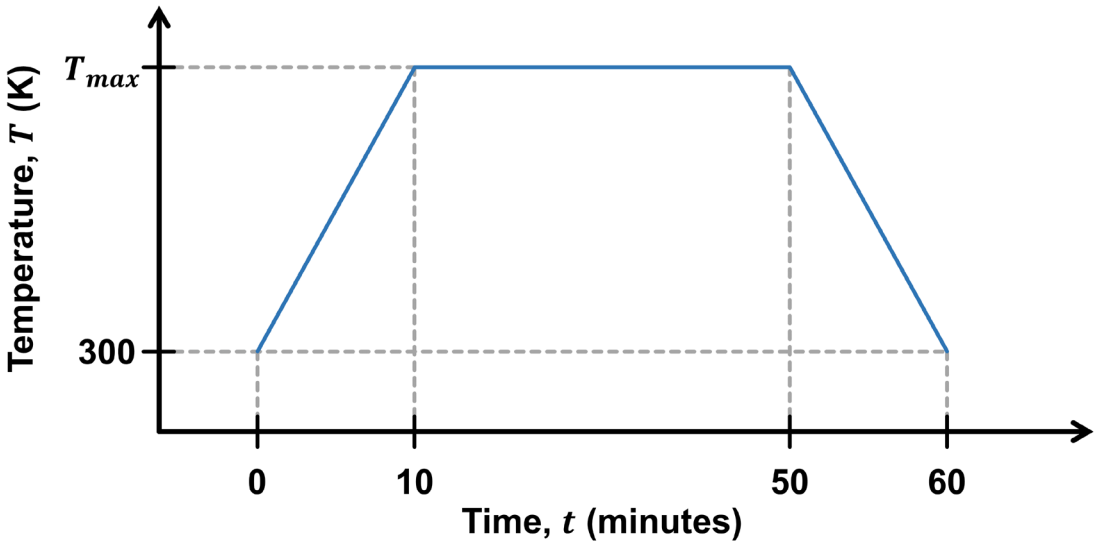

Figure PS2.2

Recall that the diffusivity of a dopant atom in a material follows an Arrhenius dependence on temperature and is given by:

$$D(T) = D_o e^{-\frac{E_A}{k_B T}}$$

Where D_o is a constant called the maximal diffusion coefficient (i.e., $\lim_{T\to\infty} D(T)$) and has units of cm^2/s, E_A is the activation energy for diffusion with units of J, k_B is the Boltzmann constant with units of J/K and T is the absolute temperature in K. Refer to page 74 of Jaeger's *Introduction to Microelectronic Fabrication* for the appropriate values of D_o and E_A.

(a) Find the value of T_{max} that yields a junction depth of 800 nm. Recall that the junction depth is defined as the depth at which $N_A = N_D$. You are advised to use a numerical tool such as MATLAB, Python, or Mathematica to solve this problem. Refer to page 75 of Jaeger for the solid solubility limit of phosphorous in silicon.

(b) Calculate the sheet resistance due to the dopant profile calculated in part (a). Refer to page 75 of Jaeger for the electrically active impurity concentration limit of phosphorous in silicon. Use the following expression for the mobility of electrons in silicon given in $\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$

[C. Hu, Modern Semiconductor Devices for Integrated Circuits. Prentice Hall: Upper Saddle River, NJ, 2010]:

$$\mu_n(x) = \frac{1318}{1 + \left(\frac{N_A + N_D(x)}{10^{17}}\right)^{0.85}} + 92$$

(c) Assuming a sheet resistance of 100 Ω/□, what is the approximate resistance between points *A* and *B* shown in Fig. PS2.3 below? *Note: do not spend too much time on this problem, an accuracy of ±20% is fine.*

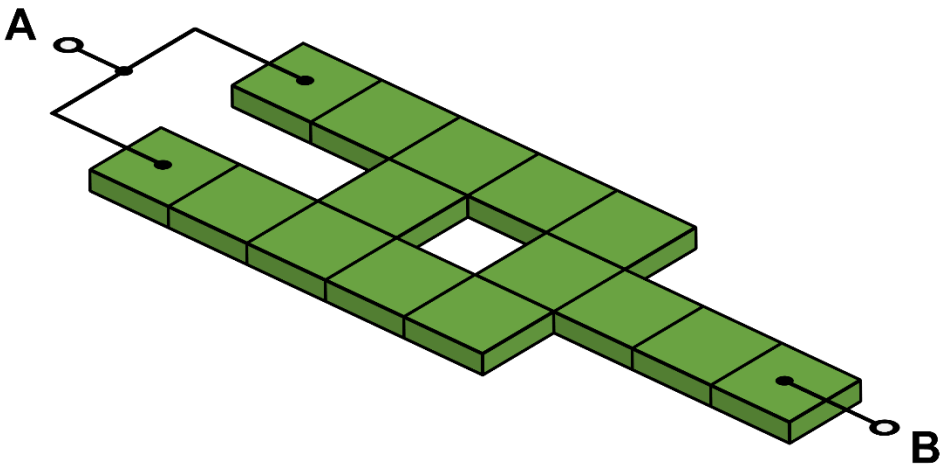

Figure PS2.3

3. Suppose you want to fabricate the structure pictured in Fig. PS2.4 below using the given fabrication process traveler.

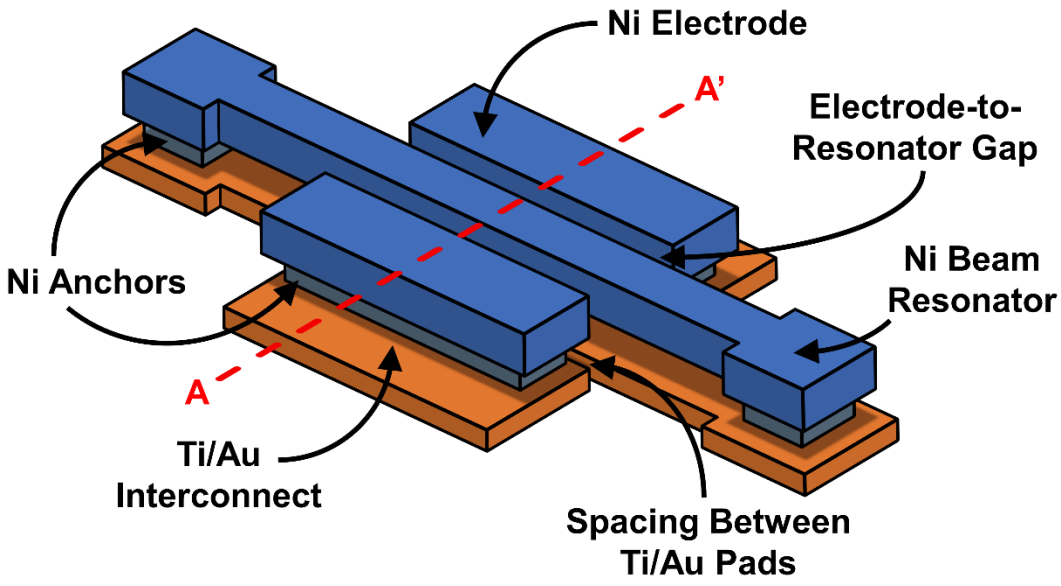

Figure PS2.4

***Process Traveler*: (Assume positive photoresist. Note that cf = "clear field" and df = "dark field".)**

(i) *Deposit 2 μm of LTO via LPCVD at 450°C.*

(ii) *Spin photoresist 2 μm-thick and pattern lithographically using **Mask 1** (df).*

(iii) *Evaporate in a non-conformal matter a sequence of 30 nm of titanium and 270 nm of gold.*

(iv) *Remove photoresist.*

(v) *Evaporate 1 μm of aluminum.*

(vi) *Lithography via **Mask 2** (df).*

(vii) *Dry etch the aluminum and stop on gold.*

(viii) *Remove photoresist.*

(ix) *Electroplate nickel in a nickel sulfamate solution at 50°C to grow over exposed gold, but not over aluminum (i.e., gold acts as a seed layer for nickel electroplating, but this particular aluminum does not). Time the electroplating to planarize the surface.*

(x) *Evaporate 20 nm of nickel to serve as a seed layer for subsequent electroplating.*

(xi) *Spin photoresist 6 μm-thick and pattern lithographically using **Mask 3** (df).*

(xii) *Electroplate nickel in a nickel sulfamate solution at 50°C to grow over exposed nickel.*

(xiii) *Remove photoresist.*

(xiv) *Remove the nickel seed layer via a wet etchant.*

(xv) *Dip in a solution of $K_4Fe(CN)_6$/NaOH, which attacks aluminum while leaving nickel, gold and oxide intact.*

(a) Sketch each of the three physical masks indicated in the process traveler that would be needed to achieve this structure. Note that you are not sketching layout; rather, you are sketching the actual masks, i.e., you are delineating the actual transparent and opaque regions on the glass or quartz plate. You need not be exact with layout dimensions; a simple sketch will suffice, as long as important features (e.g., corners, holes, etc.) are included.

(b) Draw the CAD layout, labeling the masking layers in your drawing.

(c) Draw the cross-section $A - A'$ as indicated in Figure PS2.4 *after* the following steps from the given process traveler:

1. Step (x)

2. Step (xiv)

Be sure to include dimensions as applicable (i.e., layer thicknesses) as well as layer material labels and any mentioned process nonidealities.