

Lecture 23m1: Sensing Circuits

Position-to-Voltage Conversion

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- To sense position (i.e., displacement), use a capacitive load

Again, here part-to-part I/O symmetry: ω_0

Brute force approach:

$$\frac{V_o}{V_i} = \frac{\frac{1}{sC_D}}{R_x + \frac{1}{sC_x} + sL_x + \frac{1}{sC_D}}$$

$$\frac{V_o}{V_i}(s) = \frac{\frac{C_D}{sC_D}}{1 + \frac{R_x}{sC_D} + \frac{1}{s^2C_xC_D} + \frac{L_x}{s^2C_xC_D}}$$

$$= \frac{1}{1 + \frac{R_x}{sC_D} + \frac{1}{s^2C_xC_D} + \frac{L_x}{s^2C_xC_D}}$$

$$= \frac{1}{1 + \frac{R_x}{sC_D} + \frac{1}{s^2C_xC_D} + \frac{L_x}{s^2C_xC_D}} \cdot \frac{(s\omega_0)^2}{(s\omega_0)^2}$$

$$= \frac{(s\omega_0)^2}{1 + \frac{R_x}{sC_D} + \frac{1}{s^2C_xC_D} + \frac{L_x}{s^2C_xC_D}}$$

$$= \frac{(s\omega_0)^2}{1 + \frac{R_x}{sC_D} + \frac{1}{s^2C_xC_D} + \frac{L_x}{s^2C_xC_D}} \cdot \frac{Q' \cdot \frac{L_x}{R_x}}{Q' \cdot \frac{L_x}{R_x}} = \frac{(s\omega_0)^2}{1 + \frac{R_x}{sC_D} + \frac{1}{s^2C_xC_D} + \frac{L_x}{s^2C_xC_D}} \cdot Q' \cdot \frac{L_x}{R_x}$$

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Position-to-Voltage Conversion

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- To sense position (i.e., displacement), use a capacitive load

DC Gain Term: $\frac{V_o}{V_i}(s) = \frac{C_D/C_D}{1 + C_x/C_D} \cdot \frac{(s\omega_0)^2}{s^2 + (s\omega_0)^2 + (s\omega_0)^2}$

Lad-Parr Biquad: $\frac{V_o}{V_i}(s) = \frac{C_D/C_D}{1 + C_x/C_D} \cdot \frac{(s\omega_0)^2}{s^2 + (s\omega_0)^2 + (s\omega_0)^2}$

To maximize gain $\rightarrow 1$, need $C_D \ll C_x$ (must minimize C_D)

Note: Can we similar short-cut to the R core.

- Get DC response $\rightarrow C$'s dominate.
- Then:

$$\frac{V_o}{V_i}(s) = (\text{DC Gain}) \cdot \frac{1}{s} \cdot \Theta(s, \omega_0, Q') \cdot \omega_0 Q'$$

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Problems With Pure-C Position Sensing

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- To sense position (i.e., displacement), use a capacitive load

Interconnect Bond Pad

$\frac{V_o}{V_i}(s) = \frac{C_D/C_D}{1 + C_x/C_D} \cdot \frac{1}{s} \cdot \Theta(s, \omega_0, Q') \cdot \omega_0 Q'$

Integration yields displacement.

To maximize gain, minimize C_D . \Rightarrow Problem: parasitic capacitance

$C_D \rightarrow C_D + C_{Pi} + C_{Pb}$

\Rightarrow DC Gain: $\frac{C_D/(C_D + C_{Pi} + C_{Pb})}{1 + C_x/(C_D + C_{Pi} + C_{Pb})}$

Output will get smaller!

Remedy: Suppress C_p via use of op amps.

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The Op Amp Integrator Advantage

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- The virtual ground provided by the ideal op amp eliminates the parasitic capacitance C_p allows C_2 to dominate

i_1

v_1

F_{dI}

d_1

d_2

m

b

k

i_0

C_1

C_2

V_P

R_2

C_2

V_o

$R_2 \gg \frac{1}{sC_2}$

$i_0 = i_0(R_{21} \frac{1}{sC_2}) \approx -i_0(\frac{1}{sC_2})$

$\approx -\frac{V_o}{R_x} \cdot \Theta(s) \frac{1}{sC_2} \Rightarrow \frac{V_o}{V_i}(s) = -\frac{1}{R_x C_2} \Theta(s)$

(for biasing)

$R_2 \gg \frac{1}{sC_2}$

$R_2 = 0.52$

Can drive next stage's R_x without interference to i_0 transfer function!

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Differential Position Sensing

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Differential Position Sensing

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Buffer-Bootstrapped Position Sensing

Includes capacitance from interconnects, bond pads, and C_{gs} of the op amp
 C_{gd} = gate-to-drain capacitance of the input MOS transistor

- Bootstrap the ground lines around the interconnect and bond pads
 - No voltage across C_p
 - It's effectively not there!

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Effect of Finite Op Amp Gain

Total ADXL-50 Sense $C \sim 100\text{fF}$

$$+V_p \rightarrow V_0$$

$$-V_p \rightarrow N_o = A_o(V_i - N_o) = A_o(N_i - N_o) \rightarrow N_o(1 + A_o) = A_o N_i \rightarrow \frac{N_o}{N_i} = \frac{A_o}{1 + A_o}$$

$$\text{Get } Z_i = \frac{V_i}{I_i} : I_i = (N_i - N_o) S C_p = N_i \left(1 - \frac{A_o}{1 + A_o}\right) S C_p = N_i \frac{1}{1 + A_o} S C_p$$

$$\therefore \frac{N_i}{I_i} = Z_i = \frac{1}{S \left[\frac{C_p}{1 + A_o} \right]} \rightarrow C_{eff} = \frac{C_p}{1 + A_o}$$

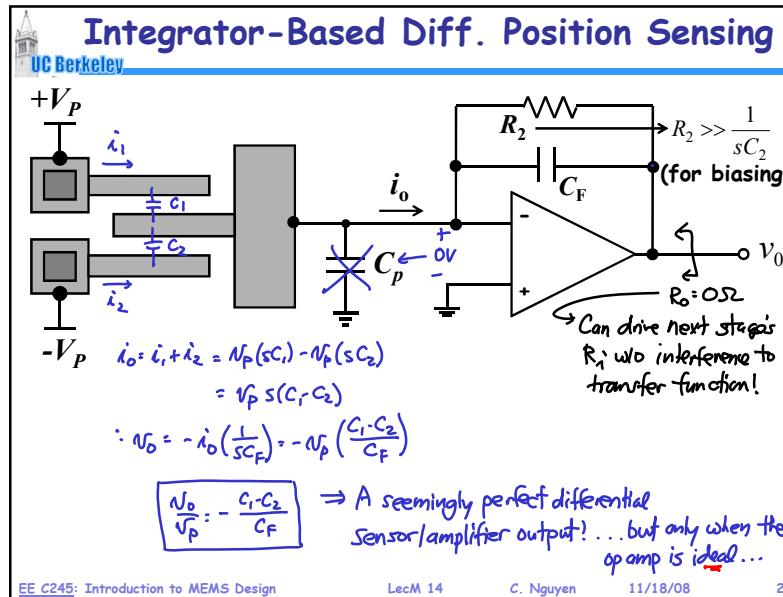
Ex: $A_o = 100$, $C_p = 2\text{pF}$
 $\Rightarrow C_{eff} = \frac{2\text{pF}}{101} = 20\text{fF}$

No longer zero!
 Not negligible compared w/ ADXL-50 $C_{tot} \sim 100\text{fF}$!

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