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Non-Ideal Operational Amplifiers

8

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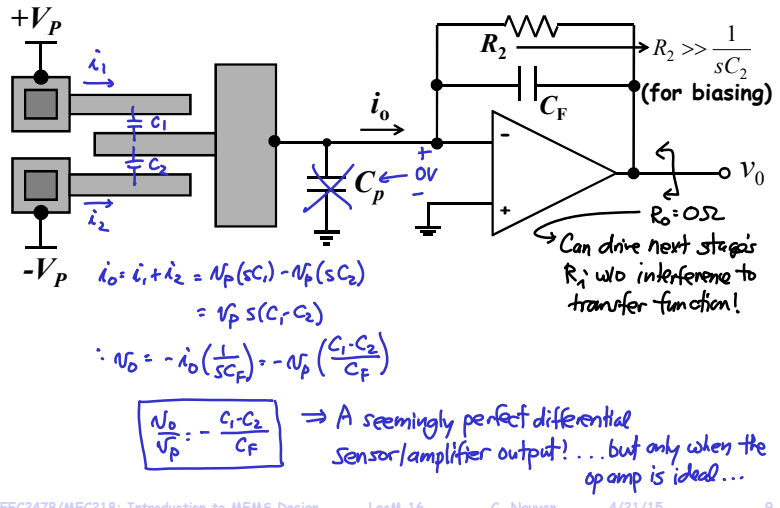
Integrator-Based Diff. Position Sensing



9

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Actual Op Amps Are Not Ideal

- Actual op amps, of course, are not ideal; rather, they …
  - Generate noise
  - Have finite gain, A_o
  - Have finite bandwidth, ω_b
  - Have finite input resistance, R_i
  - Have finite input capacitance, C_i
  - Have finite output resistance, R_o
  - Have an offset voltage V_{OS} between their (+) and (-) terminals
  - Have input bias currents
  - Have an offset I_{OS} between the bias currents into the (+) and (-) terminals
  - Have finite slew rate
  - Have finite output swing (governed by the supply voltage used, -L to +L)
- And what's worse: All of the above can be temperature (or otherwise environmentally) dependent!

10

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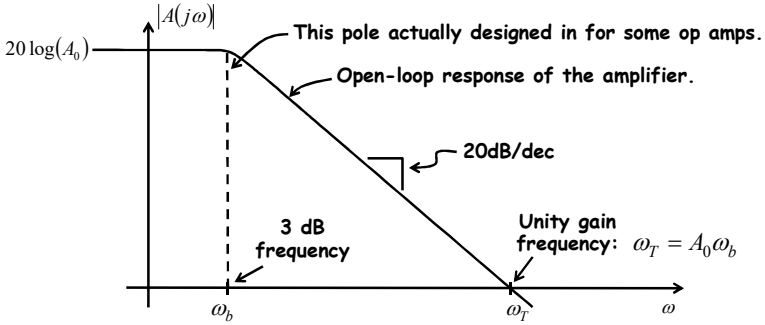
Finite Op Amp Gain and Bandwidth

- For an ideal op amp: $A = \infty$
- In reality, the gain is given by: $A(s) = \dfrac{A_0}{1 + \dfrac{s}{\omega_b}}$ ← Finite Gain; Finite Bandwidth
- For $\omega >> \omega_b$:

$$A(s) \approx \frac{A_0}{(s/\omega_b)} = \frac{A_0\omega_b}{s} = \frac{\omega_T}{s}$$

→ Integrator w/ time const. $1/\omega_T$



11

Op Amp Non-Idealities

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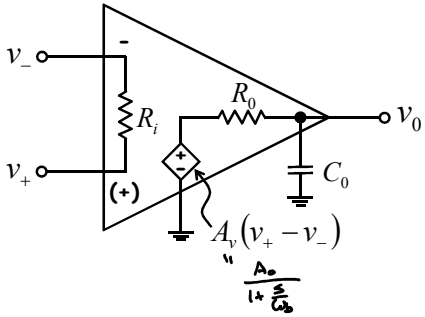
Op Amp Non-Idealities → R_i & R_0

Input resistance R_i and Output Resistance R_0:

With finite R_i and R_0, and finite gain and BW, the op amp equivalent circuit becomes:



⇒ Basically reduces down to a voltage-amplifier model

⇒ Add an output C_0 to model a single pole response, where

$$w_b = \frac{1}{R_0 C_0}$$

12

Input Offset Voltage V_{OS}

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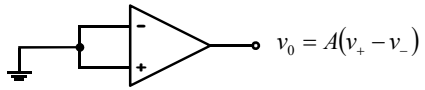
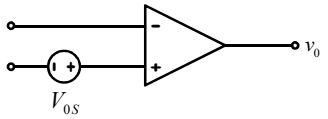
Input Offset Voltage, V_{OS}:



Ideal case: $v_0 = 0$

Reality: $v_0 \neq 0$ (usually, $v_0 = L^+$ or L^- : it rails out!)

Why? Internal mismatches within the op amp → cause a dc offset. Model this with an equivalent input offset voltage V_{OS}.



Typically, V_{OS} = 1mV – 5mV

13

Effect of V_{OS} on Op Amp Circuits

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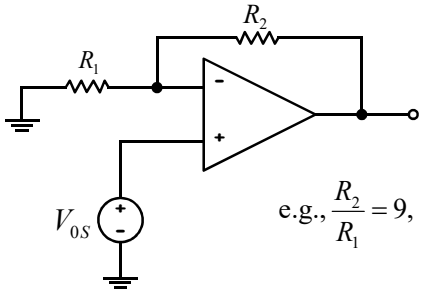
Example: Non-Inverting Amplifier



$$V_0 = V_{OS}\left(1 + \frac{R_2}{R_1}\right)$$

e.g., $\frac{R_2}{R_1} = 9$, $V_{OS} = 5mV \rightarrow V_0 = 50mV$

(not so bad …)

14

Effect of V_{OS} on Op Amp Circuits (cont.)

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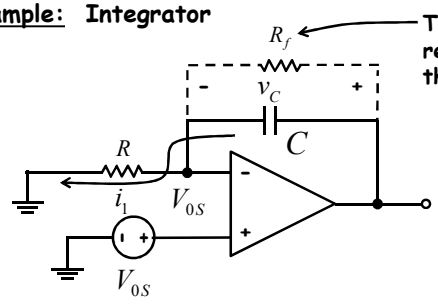
Example: Integrator



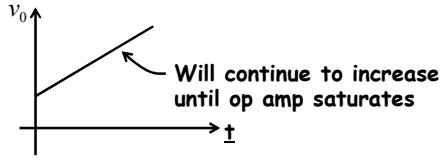
To fix this, place a resistor in shunt with the C → then:

$$v_0 = V_{OS}\left(1 + \frac{R_f}{R}\right)$$

$$v_0 = V_{OS} + \frac{1}{C}\int_0^t i_1 dt$$

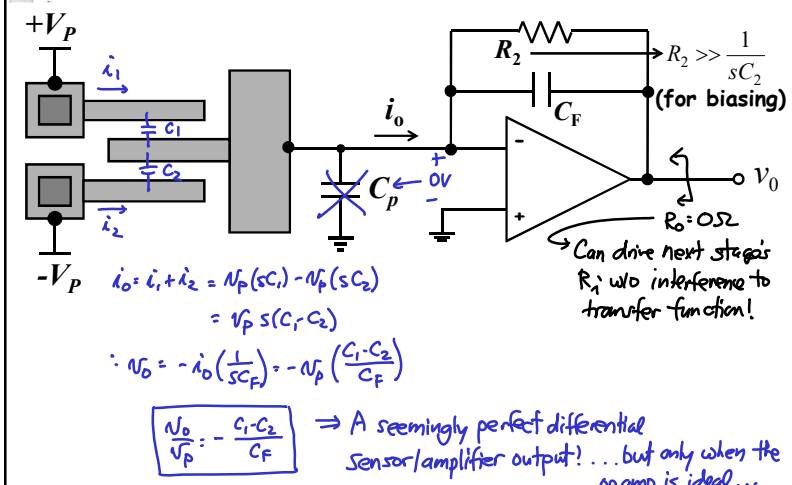
$$= V_{OS} + \frac{1}{C}\int_0^t \frac{V_{OS}}{R} dt$$

$$= V_{OS}\left(1 + \frac{t}{RC}\right) + v_C|_{t=0}$$



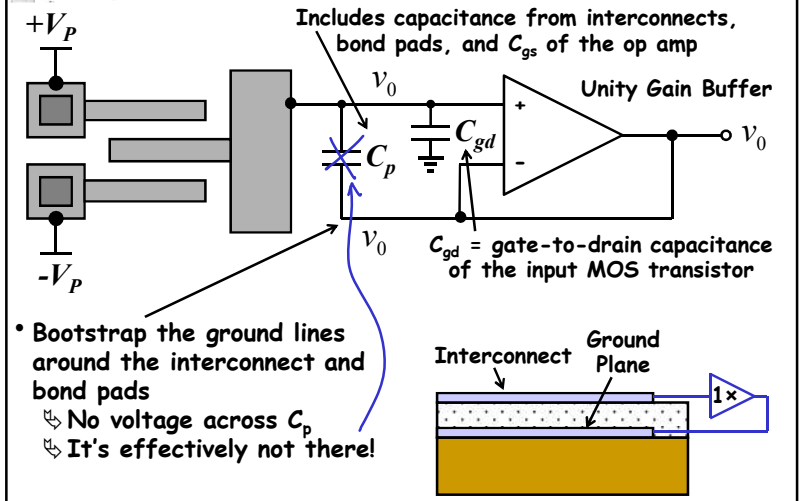
15

Integrator-Based Diff. Position Sensing



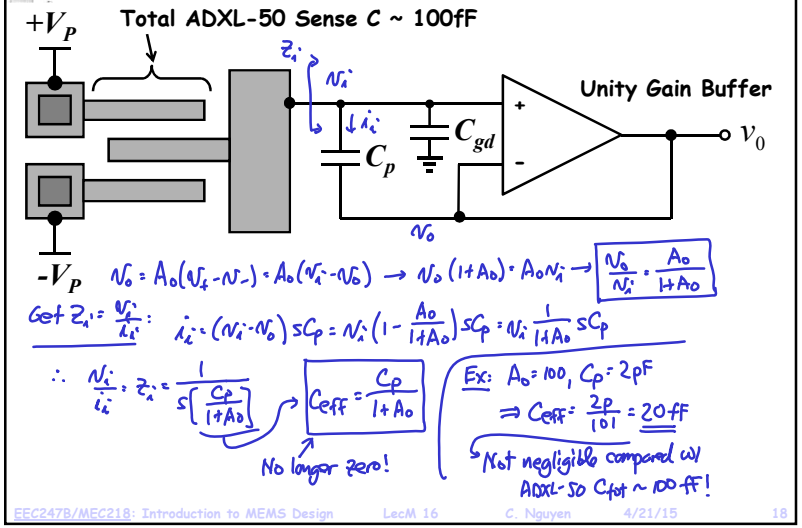
16

Buffer-Bootstrapped Position Sensing



17

Effect of Finite Op Amp Gain



18

Integration of MEMS and Transistors

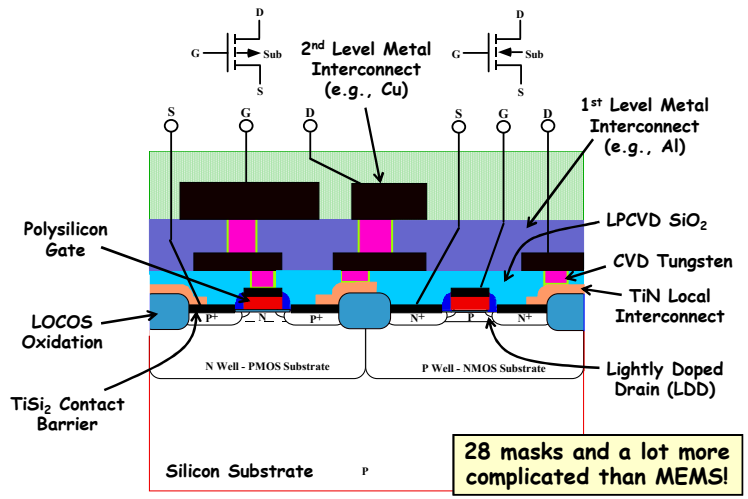
19

Integrate or Not?

- Benefits:
  - Lower parasitic capacitance and resistance → improved sensitivity and resolution, higher operation frequency
  - Better reliability
  - Reduced size → lower cost?
  - Reduced packaging complexity → integration is a form of packaging → lower cost?
  - Higher integration density supports greater functionality
- Challenges:
  - Temperature ceilings imposed by the transistors or MEMS
  - Protecting one process from the other
  - Surface topography of MEMS
  - Material incompatibilities
  - Multiplication of yield losses (versus non-integrated)
  - Acceptance by transistor foundries

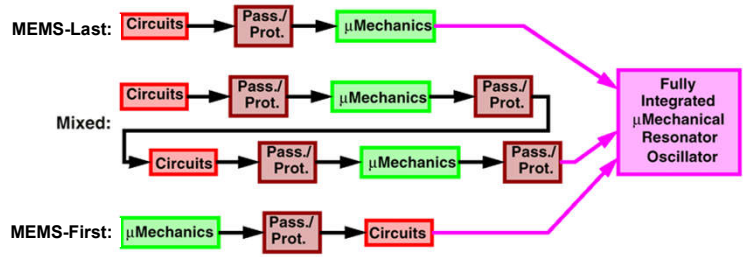
20

250 nm CMOS Cross-Section



21

Merged MEMS/Transistor Technologies (Process Philosophy)

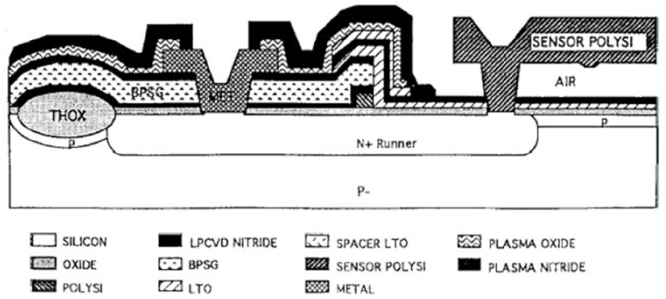


- Mixed:
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product
- MEMS-first or MEMS-last:
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

22

Analog Devices BiMEMS Process

- Interleaved MEMS and 4 µm BiMOS processes (28 masks)
- Diffused n+ runners used to interconnect MEMS & CMOS
- Relatively deep junctions allow for MEMS poly stress anneal
- Used to manufacture the ADXL-50 accelerometer and Analog Devices family of accelerometers



23

Analog Devices BiMEMS Process (cont)

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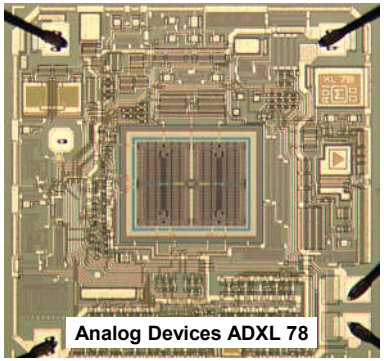
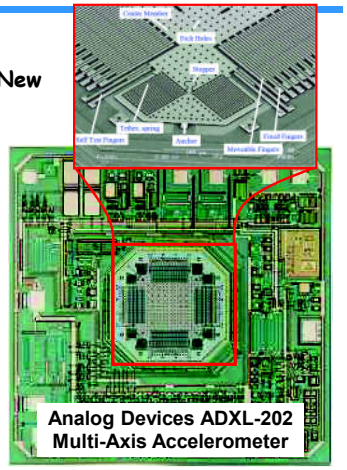
- Examples:

Old → New





- Can you list the advances in the process from old to new?

24

Merged MEMS/Transistor Technologies (Process Philosophy)

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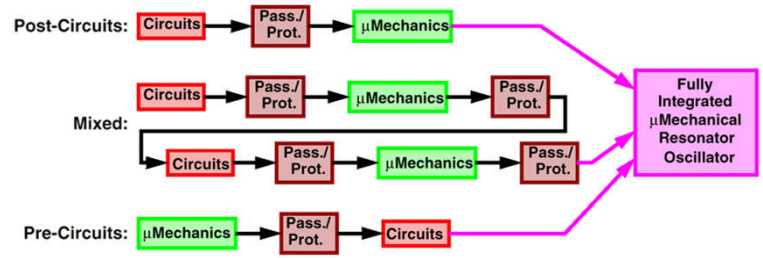

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25

MEMS-First Integration

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- Modular technology minimizes product updating effort
  - Module 1: micromachining process (planar technology)
  - Module 2: transistor process (planar IC technology)
- Adv.: (ideally) no changes needed to the transistor process
- Adv.: high temperature ceiling for some MEMS materials
- Challenges:
  - Reducing topography after MEMS processing so transistors can be processed
  - Maximizing the set of permissible MEMS materials; the materials must be able to withstand transistor processing temperatures
  - Getting transistor foundries to accept pre-processed wafers

26

MEMS-First Integration

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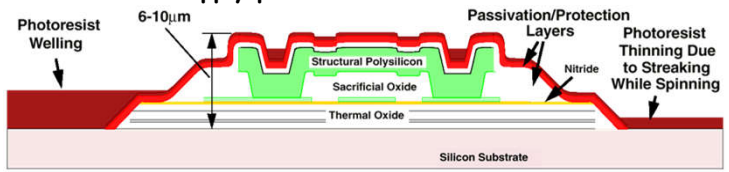
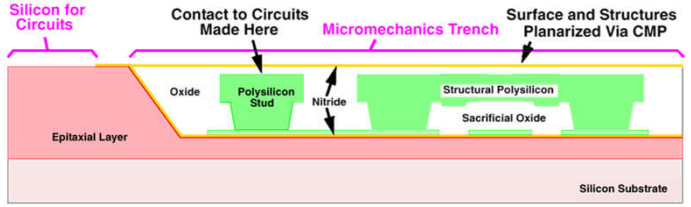
- Problem: µstructural topography interferes with lithography
  - difficult to apply photoresist for submicron circuits



- Soln.: build µmechanics in a trench, then planarize before circuit processing [Smith *et al*, IEDM'95]

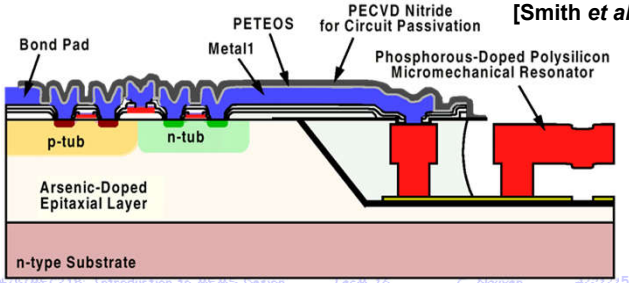


27

MEMS-First Ex: Sandia's iMEMS

- Used to demonstrate functional fully integrated oscillators
- Issues:
  - lithography and etching may be difficult in trench ⇨ may limit dimensions (not good for RF MEMS)
  - µmechanical material must stand up to IC temperatures (>1000°C) ⇨ problem for some metal materials
  - might be contamination issues for foundry IC's

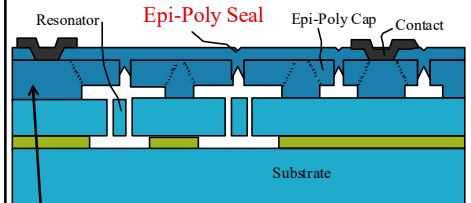
[Smith *et al*, IEDM'95]



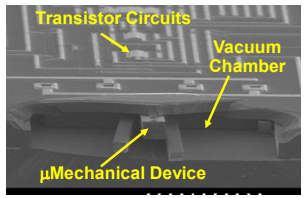
28

Bosch/Stanford MEMS-First Process

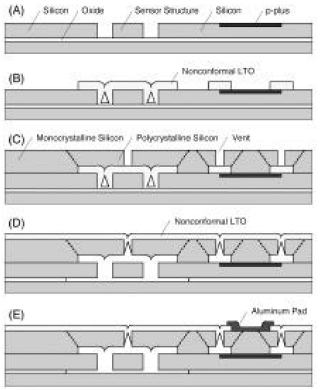
- Single-crystal silicon microstructures sealed under epi-poly encapsulation covers
- Many masking steps needed, but very stable structures



Epi-silicon for CMOS



[Kim, Kenny Trans'05]



29

Problems With MEMS-First

- Many masking steps needed, plus CMP required → cost can grow if you're not careful
- Processes using trenches sacrifice lithographic resolution in microstructures
- MEMS must withstand transistor processing temperatures
  - Precludes the use of structural materials with low temperature req'mts: metals, polymers, etc.
- Exotic MEMS (e.g., ZnO) that can contaminate transistors during their processing are not permissible
  - thus, not truly modular
- Foundry acceptance not guaranteed and might be rare

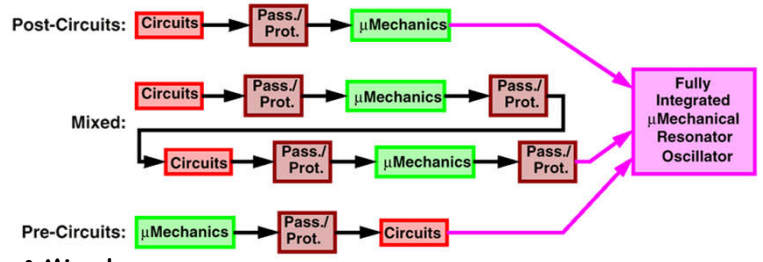
30

Foundry Acceptance of MEMS-First?

- Is a CMP'ed silicon surface sufficiently pure for fabrication of aggressively scaled transistors? How about if an oxide is grown over the CMP'ed surface and removed via a wet etch to yield a "pristine" surface?
- Is epi silicon grown as part of a sealing process sufficiently pure for fabrication of aggressively scaled transistors?
- CMOS is many times more difficult to run than MEMS
  - Feature sizes on the nm scale for billions of devices
  - Contamination a big issue: many foundries may not accept pre-processed wafers for contamination reasons
  - Many foundries will not accept any pre-processed wafers, MEMS or not → just can't guarantee working transistor circuits with unknowns in starting silicon

31

Merged MEMS/Transistor Technologies (Process Philosophy)



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  - problem: custom process for each product
- MEMS-first or MEMS-last:
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

32

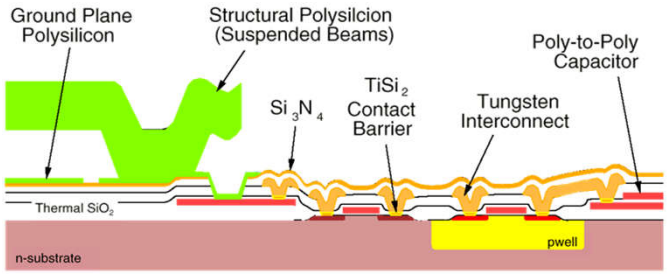
MEMS-Last Integration

- Modular technology minimizes product updating effort
  - Module 1: transistor process (planar IC technology)
  - Module 2: micromachining process (planar technology)
- Adv.: foundry friendly
  - Virtually any foundry can be used → can use the lowest cost transistor circuits (big advantage)
- Adv.: topography after circuit fabrication is quite small, especially given the use of CMP to planarize the metallization layers
- Issue: limited thermal budget ⇨ limits the set of usable structural materials
  - Metallization goes bad if temperature gets too high
  - Aluminum grows hillocks and spikes junctions if T>500°C
  - Copper diffusion can be an issue at high temperature
  - Low-k dielectrics used around metals may soon lower the temperature ceiling to only 320°C

33

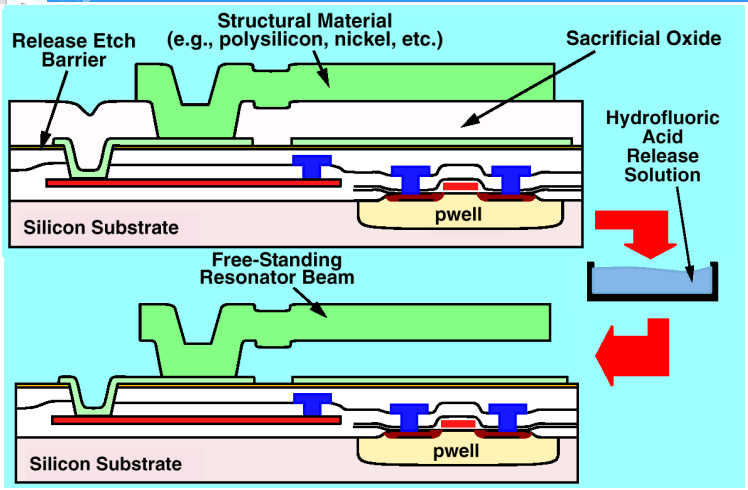
Berkeley Polysilicon MICS Process

- Uses surface-micromachined polysilicon microstructures with silicon nitride layer between transistors & MEMS
  - Polysilicon dep. T~600°C; nitride dep. T~835°C
  - 1100°C RTA stress anneal for 1 min.
  - metal and junctions must withstand temperatures ~835°C
  - tungsten metallization used with $TiSi_2$ contact barriers
  - *in situ* doped structural polySi; rapid thermal annealing



34

Surface Micromachining



- Fabrication steps compatible with planar IC processing

35

Single-Chip Ckt/MEMS Integration

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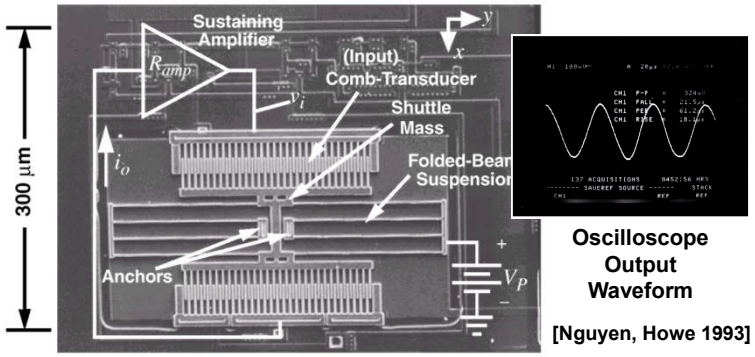
- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)



Oscilloscope Output Waveform

[Nguyen, Howe 1993]

- To allow the use of >600°C processing temperatures, tungsten (instead of aluminum) is used for metallization

36

Usable MEMS-Last Integration

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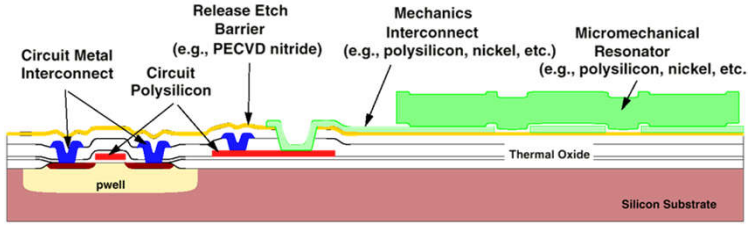
- Problem: tungsten is not an accepted primary interconnect metal
- Challenge: retain conventional metallization
  - minimize post-CMOS processing temperatures
  - explore alternative structural materials (e.g., plated nickel, SiGe [Franke, Howe *et al*, MEMS'99])
  - Limited set of usable structural materials → not the best situation, but workable



37

Poly-SiGe MICS Process

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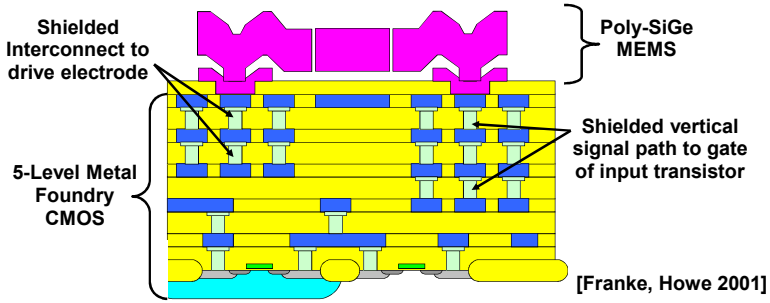
- MICS = "Modular Integration of Circuits and Structures"
- MEMS-last process, where SiGe micromechanics are planar processed directly above conventional foundry circuits
  - enabled by lower deposition temperature of SiGe ~450°C
  - *Adv.*: alleviates contamination issues of pre-circuit processes, allowing a wider choice of IC technologies



[Franke, Howe 2001]

38

Polysilicon Germanium

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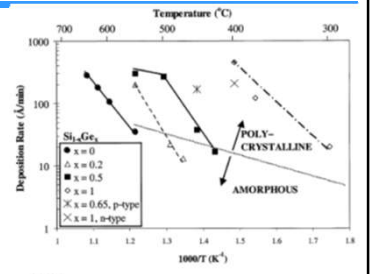
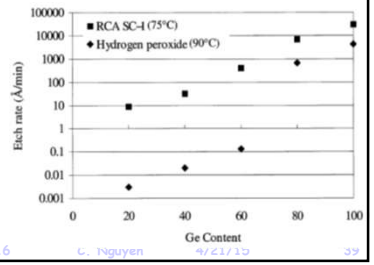
- Deposition
  - LPCVD thermal decomposition of GeH_4 and SiH_4 or Si_2H_6
  - Rate >50 Å/min, T < 475°C, P = 300-600 mT
  - At higher [Ge]: rate ↑, T ↓
  - In-situ doping, ion implantation
- Dry Etching
  - Similar to poly-Si, use F, Cl, and Br⁻ containing plasmas
  - Rate ~0.4 μm/min
- Wet Etching
  - H_2O_2 @ 90°C: can get 4 orders of magnitude selectivity between >80% and <60% Ge content
  - Good release etchant

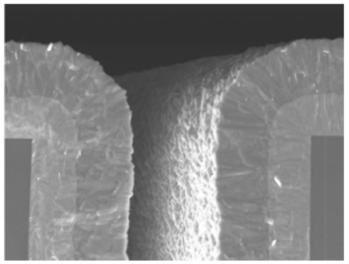


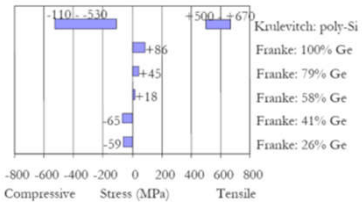


39

Poly-SiGe Mechanical Properties

- Conformal deposition
- Low as-deposited stress (when its done right)
- Young's modulus ~ 146 GPa (for poly-$Si_{0.35}Ge_{0.65}$)
- Density ~4280 kg/m^3
- Acoustic velocity ~5840 m/s (25% lower than polysilicon)
  - Harder to achieve high frequency devices
- Fracture strain 1.7% (compared to 1.5% for MUMPS polySi)
- Q=30,000 for n-type poly-Ge in vacuum

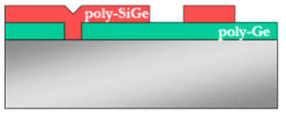


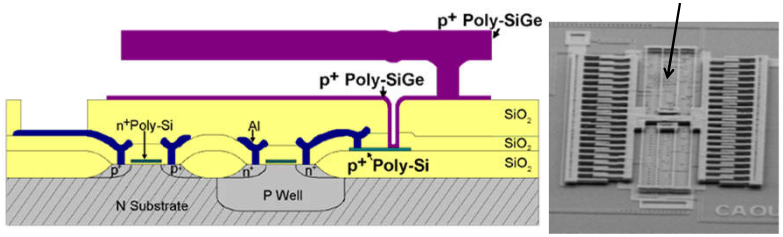


40

UCB Poly-SiGe MICS Process

- 2 μm standard CMOS process w/ Al metallization
- P-type poly-$Si_{0.35}Ge_{0.65}$ structural material; poly-Ge sacrificial material
- Process:
  - Passivate CMOS w/ LTO @ 400°C
  - Open vias to interconnect runners
  - Deposit & pattern ground plane
  - RTA anneal to lower resistivity (550°C, 30s)

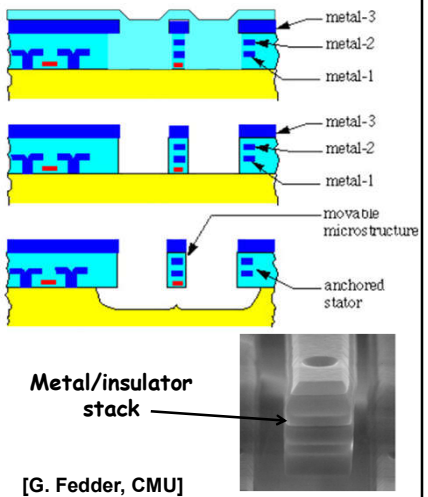




41

ASIMPS Ckt/MEMS Integration Process

- MEMS constructed from metal/insulator laminates of foundry CMOS
- Top metal layer used as etch mask for CHF_3/O_2 oxide etch
- Structures released via a final SF_6 isotropic dry etch
- Independent electrostatic actuation possible due to multiple insulated metal layers
- Stress issues can be tricky
  - Must design defensively against warping

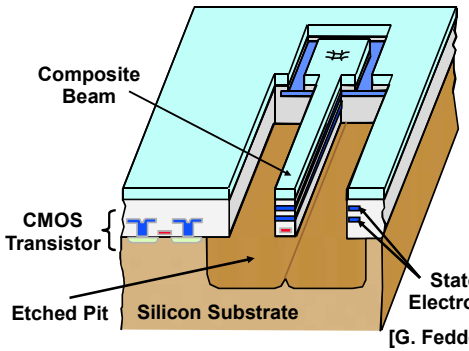


[G. Fedder, CMU]

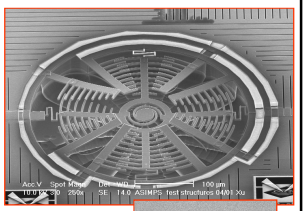
42

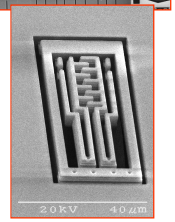
ASIMPS Ckt/MEMS Integration Process

- Direct integration of Al/oxide MEMS structure with silicon CMOS or SiGe BiCMOS circuits
- Multiple electrodes within structures
- Derivatives for bulk silicon structures

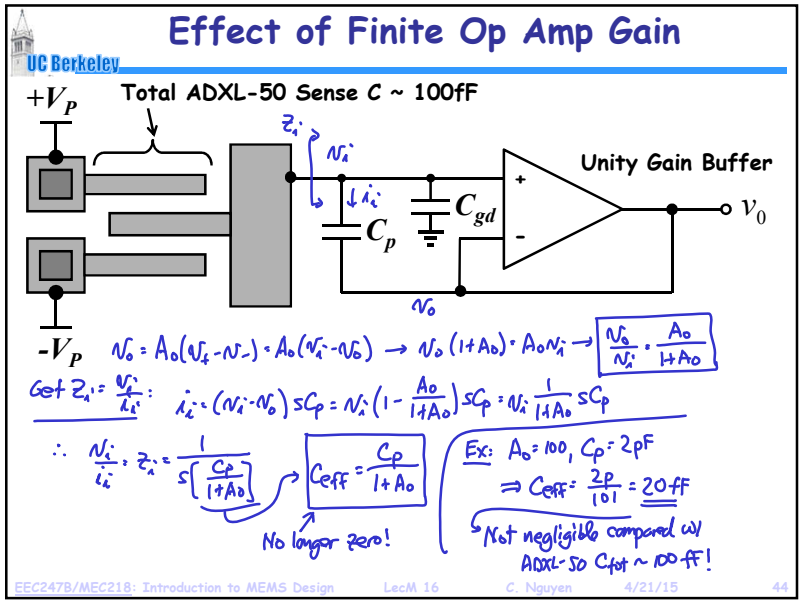


[G. Fedder, CMU]





43



44