

UC Berkeley

## Non-Ideal Operational Amplifiers

EE247B/ME218: Introduction to MEMS Design    LecM 16    C. Nguyen    4/21/15    8

UC Berkeley

## Integrator-Based Diff. Position Sensing

$i_o = i_1 + i_2 = N_p(sC_1) - N_p(sC_2)$   
 $= V_p s(C_1 - C_2)$   
 $\therefore V_o = -i_o \left( \frac{1}{sC_F} \right) = -N_p \left( \frac{C_1 - C_2}{C_F} \right)$

$\frac{V_o}{V_p} = - \frac{C_1 - C_2}{C_F} \Rightarrow$  A seemingly perfect differential sensor/amplifier output! ... but only when the op amp is ideal...

$R_2 \gg \frac{1}{sC_2}$  (for biasing)  
 $R_0 = 0\Omega$   
 Can drive next stages  $R_1$  w/o interference to transfer function!

EE247B/ME218: Introduction to MEMS Design    LecM 16    C. Nguyen    4/21/15    9

8

9

UC Berkeley

## Actual Op Amps Are Not Ideal

- Actual op amps, of course, are not ideal; rather, they ...
  - ☞ Generate noise
  - ☞ Have finite gain,  $A_o$
  - ☞ Have finite bandwidth,  $\omega_b$
  - ☞ Have finite input resistance,  $R_i$
  - ☞ Have finite input capacitance,  $C_i$
  - ☞ Have finite output resistance,  $R_o$
  - ☞ Have an offset voltage  $V_{OS}$  between their (+) and (-) terminals
  - ☞ Have input bias currents
  - ☞ Have an offset  $I_{OS}$  between the bias currents into the (+) and (-) terminals
  - ☞ Have finite slew rate
  - ☞ Have finite output swing (governed by the supply voltage used, -L to +L)
- And what's worse: All of the above can be temperature (or otherwise environmentally) dependent!

EE247B/ME218: Introduction to MEMS Design    LecM 16    C. Nguyen    4/21/15    10

10

UC Berkeley

## Finite Op Amp Gain and Bandwidth

- For an ideal op amp:  $A = \infty$
- In reality, the gain is given by:  $A(s) = \frac{A_0}{1 + \frac{s}{\omega_b}}$ 
  - $A_0$  ← Finite Gain
  - $\omega_b$  ← Finite Bandwidth
- For  $\omega \gg \omega_b$ :  $A(s) \approx \frac{A_0}{(s/\omega_b)} = \frac{A_0 \omega_b}{s} = \frac{\omega_T}{s} \rightarrow$  Integrator w/ time const.  $1/\omega_T$

$20 \log(A_0)$   
 This pole actually designed in for some op amps.  
 Open-loop response of the amplifier.  
 20dB/dec  
 3 dB frequency  $\omega_b$   
 Unity gain frequency:  $\omega_T = A_0 \omega_b$

EE247B/ME218: Introduction to MEMS Design    LecM 16    C. Nguyen    4/21/15    11

11

### Op Amp Non-Idealities

UC Berkeley

**Op Amp Non-Idealities →  $R_i$  &  $R_o$**

**Input resistance  $R_i$  and Output Resistance  $R_o$ :**

With finite  $R_i$  and  $R_o$ , and finite gain and BW, the op amp equivalent circuit becomes:

⇒ Basically reduces down to a voltage-amplifier model  
 ⇒ Add an output  $C_o$  to model a single pole response, where

$$w_b = \frac{1}{R_o C_o}$$

$A_v = \frac{A_o}{1 + sC_o/R_o}$

EEC247B/MEC218: Introduction to MEMS Design    LecM 16    C. Nguyen    4/21/15    12

12

### Input Offset Voltage $V_{OS}$

UC Berkeley

**Input Offset Voltage,  $V_{OS}$ :**

$v_o = A(v_+ - v_-)$

**Ideal case:**  $v_o = 0$   
**Reality:**  $v_o \neq 0$  (usually,  $v_o = L^+$  or  $L^-$ : it rails out!)

**Why? Internal mismatches within the op amp → cause a dc offset. Model this with an equivalent input offset voltage  $V_{OS}$ .**

Typically,  $V_{OS} = 1mV - 5mV$

EEC247B/MEC218: Introduction to MEMS Design    LecM 16    C. Nguyen    4/21/15    13

13

### Effect of $V_{OS}$ on Op Amp Circuits

UC Berkeley

**Example: Non-Inverting Amplifier**

$$V_o = V_{OS} \left( 1 + \frac{R_2}{R_1} \right)$$

e.g.,  $\frac{R_2}{R_1} = 9$ ,  $V_{OS} = 5mV \rightarrow V_o = 50mV$   
 (not so bad ...)

EEC247B/MEC218: Introduction to MEMS Design    LecM 16    C. Nguyen    4/21/15    14

14

### Effect of $V_{OS}$ on Op Amp Circuits (cont.)

UC Berkeley

**Example: Integrator**

To fix this, place a resistor in shunt with the  $C \rightarrow$  then:

$$v_o = V_{OS} \left( 1 + \frac{R_f}{R} \right)$$

$$v_o = V_{OS} + \frac{1}{C} \int_0^t i_1 dt$$

$$= V_{OS} + \frac{1}{C} \int_0^t \frac{V_{OS}}{R} dt$$

$$= V_{OS} \left( 1 + \frac{t}{RC} \right) + v_C|_{t=0}$$

Will continue to increase until op amp saturates

EEC247B/MEC218: Introduction to MEMS Design    LecM 16    C. Nguyen    4/21/15    15

15

### Integrator-Based Diff. Position Sensing

UC Berkeley

$+V_P$   
 $-V_P$

$i_1$   
 $i_2$

$C_1$   
 $C_2$

$i_o$

$R_2 \gg \frac{1}{sC_2}$  (for biasing)

$C_F$

$R_0 = 0\Omega$

$V_0$

Can drive next stage's  $R_1$  w/o interference to transfer function!

$i_o = i_1 + i_2 = N_p(sC_1) - N_p(sC_2) = N_p s(C_1 - C_2)$

$\therefore V_0 = -i_o \left(\frac{1}{sC_F}\right) = -N_p \left(\frac{C_1 - C_2}{C_F}\right)$

$\frac{V_0}{V_p} = -\frac{C_1 - C_2}{C_F} \Rightarrow$  A seemingly perfect differential sensor/amplifier output! ... but only when the op amp is ideal...

EEEC247B/MEEC218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 16

16

### Buffer-Bootstrapped Position Sensing

UC Berkeley

$+V_P$   
 $-V_P$

Includes capacitance from interconnects, bond pads, and  $C_{gs}$  of the op amp

$V_0$

Unity Gain Buffer

$C_p$

$C_{gd}$  = gate-to-drain capacitance of the input MOS transistor

$V_0$

• Bootstrap the ground lines around the interconnect and bond pads

- ⊗ No voltage across  $C_p$
- ⊗ It's effectively not there!

Interconnect  
 Ground Plane

1x

EEEC247B/MEEC218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 17

17

### Effect of Finite Op Amp Gain

UC Berkeley

$+V_P$   
 $-V_P$

Total ADXL-50 Sense  $C \sim 100\text{fF}$

$N_i$

$i_i$

$C_p$

$C_{gd}$

Unity Gain Buffer

$V_0$

$N_0 = A_0(N_i - N_0) \Rightarrow N_0(1 + A_0) = A_0 N_i \Rightarrow \frac{N_0}{N_i} = \frac{A_0}{1 + A_0}$

Get  $Z_i = \frac{V_i}{i_i}$ :  $i_i = (N_i - N_0) sC_p = N_i \left(1 - \frac{A_0}{1 + A_0}\right) sC_p = N_i \frac{1}{1 + A_0} sC_p$

$\therefore \frac{N_i}{i_i} = Z_i = \frac{1}{s \left[\frac{C_p}{1 + A_0}\right]} \Rightarrow C_{\text{eff}} = \frac{C_p}{1 + A_0}$

No longer zero!

Ex:  $A_0 = 100$ ,  $C_p = 2\text{pF}$   
 $\Rightarrow C_{\text{eff}} = \frac{2\text{pF}}{101} = 20\text{fF}$   
 Not negligible compared w/ ADXL-50  $C_{\text{tot}} \sim 100\text{fF}$ !

EEEC247B/MEEC218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 18

18

### Integration of MEMS and Transistors

UC Berkeley

EEEC247B/MEEC218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 19

19

### Integrate or Not?

UC Berkeley

- Benefits:**
  - Lower parasitic capacitance and resistance → improved sensitivity and resolution, higher operation frequency
  - Better reliability
  - Reduced size → lower cost?
  - Reduced packaging complexity → integration is a form of packaging → lower cost?
  - Higher integration density supports greater functionality
- Challenges:**
  - Temperature ceilings imposed by the transistors or MEMS
  - Protecting one process from the other
  - Surface topography of MEMS
  - Material incompatibilities
  - Multiplication of yield losses (versus non-integrated)
  - Acceptance by transistor foundries

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 20

20

### 250 nm CMOS Cross-Section

UC Berkeley

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 21

21

### Merged MEMS/Transistor Technologies (Process Philosophy)

UC Berkeley

- Mixed:**
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product
- MEMS-first or MEMS-last:**
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 22

22

### Analog Devices BiMEMS Process

UC Berkeley

- Interleaved MEMS and 4 μm BiMOS processes (28 masks)
- Diffused n+ runners used to interconnect MEMS & CMOS
- Relatively deep junctions allow for MEMS poly stress anneal
- Used to manufacture the ADXL-50 accelerometer and Analog Devices family of accelerometers

SILICON	LPCVD NITRIDE	SPACER LTO	PLASMA OXIDE
OXIDE	BPSG	SENSOR POLYSI	PLASMA NITRIDE
POLYSI	LTO	METAL	

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 23

23

### Analog Devices BiMEMS Process (cont)

UC Berkeley

• **Examples:**

Old → New

Analog Devices ADXL 78

Analog Devices ADXL-202 Multi-Axis Accelerometer

• Can you list the advances in the process from old to new?

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 24

24

### Merged MEMS/Transistor Technologies (Process Philosophy)

UC Berkeley

Post-Circuits: Circuits → Pass./Prot. → μMechanics

Mixed: Circuits → Pass./Prot. → μMechanics → Pass./Prot. and Circuits → Pass./Prot. → μMechanics → Pass./Prot.

Pre-Circuits: μMechanics → Pass./Prot. → Circuits

• **Mixed:**

- ⌘ **problem:** multiple passivation/protection steps ⇒ large number of masks required
- ⌘ **problem:** custom process for each product

• **MEMS-first or MEMS-last:**

- ⌘ **adv.:** modularity ⇒ flexibility ⇒ less development time
- ⌘ **adv.:** low pass./protection complexity ⇒ fewer masks

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 25

25

### MEMS-First Integration

UC Berkeley

- **Modular technology** minimizes product updating effort
  - ⌘ **Module 1:** micromachining process (planar technology)
  - ⌘ **Module 2:** transistor process (planar IC technology)
- **Adv.:** (ideally) no changes needed to the transistor process
- **Adv.:** high temperature ceiling for some MEMS materials
- **Challenges:**
  - ⌘ Reducing topography after MEMS processing so transistors can be processed
  - ⌘ Maximizing the set of permissible MEMS materials; the materials must be able to withstand transistor processing temperatures
  - ⌘ Getting transistor foundries to accept pre-processed wafers

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 26

26

### MEMS-First Integration

UC Berkeley

- **Problem:** μstructural topography interferes with lithography
  - ⌘ difficult to apply photoresist for submicron circuits

- **Soln.:** build μmechanics in a trench, then planarize before circuit processing [Smith et al, IEDM'95]

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 27

27

### MEMS-First Ex: Sandia's iMEMS

UC Berkeley

- Used to demonstrate functional fully integrated oscillators
- Issues:
  - lithography and etching may be difficult in trench  $\Rightarrow$  may limit dimensions (not good for RF MEMS)
  - $\mu$ mechanical material must stand up to IC temperatures ( $>1000^\circ\text{C}$ )  $\Rightarrow$  problem for some metal materials
  - might be contamination issues for foundry IC's

[Smith et al, IEDM'95]

EEEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 28

28

### Bosch/Stanford MEMS-First Process

UC Berkeley

- Single-crystal silicon microstructures sealed under epi-poly encapsulation covers
- Many masking steps needed, but very stable structures

[Kim, Kenny Trans'05]

EEEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 29

29

### Problems With MEMS-First

UC Berkeley

- Many masking steps needed, plus CMP required  $\rightarrow$  cost can grow if you're not careful
- Processes using trenches sacrifice lithographic resolution in microstructures
- MEMS must withstand transistor processing temperatures
  - Precludes the use of structural materials with low temperature req'ts: metals, polymers, etc.
- Exotic MEMS (e.g., ZnO) that can contaminate transistors during their processing are not permissible
  - thus, not truly modular
- Foundry acceptance not guaranteed and might be rare

EEEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 30

30

### Foundry Acceptance of MEMS-First?

UC Berkeley

- Is a CMP'd silicon surface sufficiently pure for fabrication of aggressively scaled transistors? How about if an oxide is grown over the CMP'd surface and removed via a wet etch to yield a "pristine" surface?
- Is epi silicon grown as part of a sealing process sufficiently pure for fabrication of aggressively scaled transistors?
- CMOS is many times more difficult to run than MEMS
  - Feature sizes on the nm scale for billions of devices
  - Contamination a big issue: many foundries may not accept pre-processed wafers for contamination reasons
  - Many foundries will not accept any pre-processed wafers, MEMS or not  $\rightarrow$  just can't guarantee working transistor circuits with unknowns in starting silicon

EEEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 31

31

### Merged MEMS/Transistor Technologies (Process Philosophy)

Post-Circuits: Circuits → Pass./Prot. → μMechanics

Mixed: Circuits → Pass./Prot. → μMechanics → Pass./Prot. → Fully Integrated μMechanical Resonator Oscillator

Pre-Circuits: μMechanics → Pass./Prot. → Circuits → Fully Integrated μMechanical Resonator Oscillator

- **Mixed:**
  - ↳ **problem:** multiple passivation/protection steps ⇒ large number of masks required
  - ↳ **problem:** custom process for each product
- **MEMS-first or MEMS-last:**
  - ↳ **adv.:** modularity ⇒ flexibility ⇒ less development time
  - ↳ **adv.:** low pass./protection complexity ⇒ fewer masks

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 32

32

### MEMS-Last Integration

- **Modular technology** minimizes product updating effort
  - ↳ **Module 1:** transistor process (planar IC technology)
  - ↳ **Module 2:** micromachining process (planar technology)
- **Adv.:** foundry friendly
  - ↳ Virtually any foundry can be used → can use the lowest cost transistor circuits (big advantage)
- **Adv.:** topography after circuit fabrication is quite small, especially given the use of CMP to planarize the metallization layers
- **Issue:** limited thermal budget ⇒ limits the set of usable structural materials
  - ↳ Metallization goes bad if temperature gets too high
  - ↳ Aluminum grows hillocks and spikes junctions if  $T > 500^{\circ}\text{C}$
  - ↳ Copper diffusion can be an issue at high temperature
  - ↳ Low-k dielectrics used around metals may soon lower the temperature ceiling to only  $320^{\circ}\text{C}$

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 33

33

### Berkeley Polysilicon MICS Process

- **Uses surface-micromachined polysilicon microstructures with silicon nitride layer between transistors & MEMS**
  - ↳ Polysilicon dep.  $T \sim 600^{\circ}\text{C}$ ; nitride dep.  $T \sim 835^{\circ}\text{C}$
  - ↳  $1100^{\circ}\text{C}$  RTA stress anneal for 1 min.
  - ↳ metal and junctions must withstand temperatures  $\sim 835^{\circ}\text{C}$
  - ↳ tungsten metallization used with  $\text{TiSi}_2$  contact barriers
  - ↳ *in situ* doped structural polySi; rapid thermal annealing

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 34

34

### Surface Micromachining

Structural Material (e.g., polysilicon, nickel, etc.)

Release Etch Barrier

Sacrificial Oxide

Hydrofluoric Acid Release Solution

Free-Standing Resonator Beam

• **Fabrication steps compatible with planar IC processing**

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 35

35

### Single-Chip Ckt/MEMS Integration

UC Berkeley

- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)

Oscilloscope Output Waveform  
 [Nguyen, Howe 1993]

- To allow the use of  $>600^{\circ}\text{C}$  processing temperatures, tungsten (instead of aluminum) is used for metallization

EE247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 36

36

### Usable MEMS-Last Integration

UC Berkeley

- Problem:** tungsten is not an accepted primary interconnect metal
- Challenge:** retain conventional metallization
  - minimize post-CMOS processing temperatures
  - explore alternative structural materials (e.g., plated nickel, SiGe [Franke, Howe et al, MEMS'99])
  - Limited set of usable structural materials  $\rightarrow$  not the best situation, but workable

EE247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 37

37

### Poly-SiGe MICS Process

UC Berkeley

- MICS = "Modular Integration of Circuits and Structures"
- MEMS-last process, where SiGe micromechanics are planar processed directly above conventional foundry circuits
  - enabled by lower deposition temperature of SiGe  $\sim 450^{\circ}\text{C}$
  - Adv.: alleviates contamination issues of pre-circuit processes, allowing a wider choice of IC technologies

[Franke, Howe 2001]

EE247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 38

38

### Polysilicon Germanium

UC Berkeley

- Deposition**
  - LPCVD thermal decomposition of  $\text{GeH}_4$  and  $\text{SiH}_4$  or  $\text{Si}_2\text{H}_6$
  - Rate  $>50 \text{ \AA}/\text{min}$ ,  $T < 475^{\circ}\text{C}$ ,  $P = 300\text{-}600 \text{ mT}$
  - At higher [Ge]: rate  $\uparrow$ ,  $T \downarrow$
  - In-situ doping, ion implantation
- Dry Etching**
  - Similar to poly-Si, use F, Cl, and Br<sup>-</sup> containing plasmas
  - Rate  $\sim 0.4 \mu\text{m}/\text{min}$
- Wet Etching**
  - $\text{H}_2\text{O}_2$  @  $90^{\circ}\text{C}$ : can get 4 orders of magnitude selectivity between  $>80\%$  and  $<60\%$  Ge content
  - Good release etchant

EE247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 39

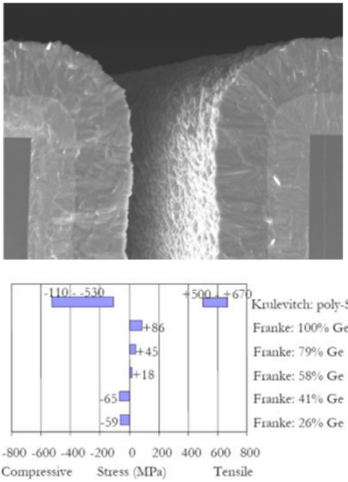
39



### Poly-SiGe Mechanical Properties

UC Berkeley

- Conformal deposition
- Low as-deposited stress (when its done right)
- Young's modulus  $\sim 146$  GPa (for poly-Si<sub>0.35</sub>Ge<sub>0.65</sub>)
- Density  $\sim 4280$  kg/m<sup>3</sup>
- Acoustic velocity  $\sim 5840$  m/s (25% lower than polysilicon)
  - Harder to achieve high frequency devices
- Fracture strain 1.7% (compared to 1.5% for MUMPS polySi)
- Q=30,000 for n-type poly-Ge in vacuum



Stress (MPa) values: -110, -530, -65, -59, +18, +45, +86, +500, +670

Legend:

- Krulevitch: poly-Si
- Franke: 100% Ge
- Franke: 79% Ge
- Franke: 58% Ge
- Franke: 41% Ge
- Franke: 26% Ge

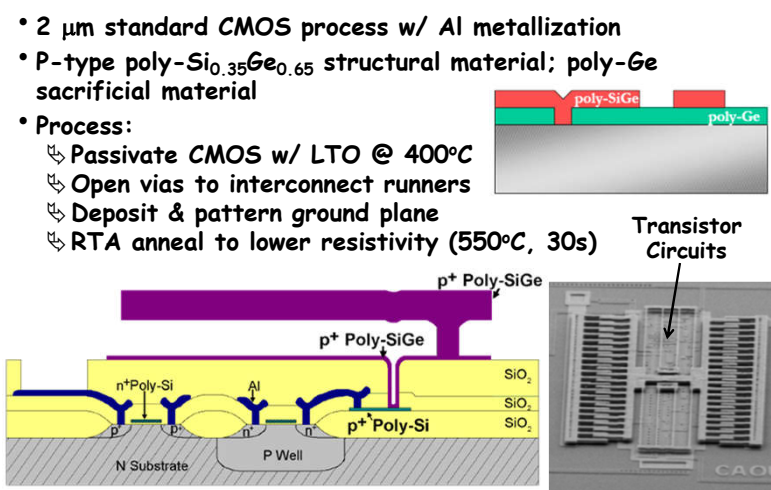
EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 40

40

### UCB Poly-SiGe MICS Process

UC Berkeley

- 2  $\mu\text{m}$  standard CMOS process w/ Al metallization
- P-type poly-Si<sub>0.35</sub>Ge<sub>0.65</sub> structural material; poly-Ge sacrificial material
- Process:
  - Passivate CMOS w/ LTO @ 400°C
  - Open vias to interconnect runners
  - Deposit & pattern ground plane
  - RTA anneal to lower resistivity (550°C, 30s)



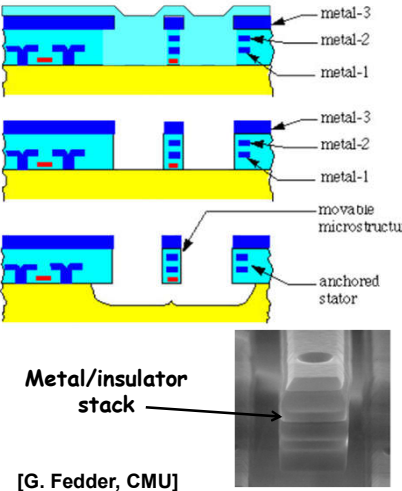
EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 41

41

### ASIMPS Ckt/MEMS Integration Process

UC Berkeley

- MEMS constructed from metal/insulator laminates of foundry CMOS
- Top metal layer used as etch mask for CHF<sub>3</sub>/O<sub>2</sub> oxide etch
- Structures released via a final SF<sub>6</sub> isotropic dry etch
- Independent electrostatic actuation possible due to multiple insulated metal layers
- Stress issues can be tricky
  - Must design defensively against warping



Labels: metal-3, metal-2, metal-1, movable microstructure, anchored stator, Metal/insulator stack

[G. Fedder, CMU]

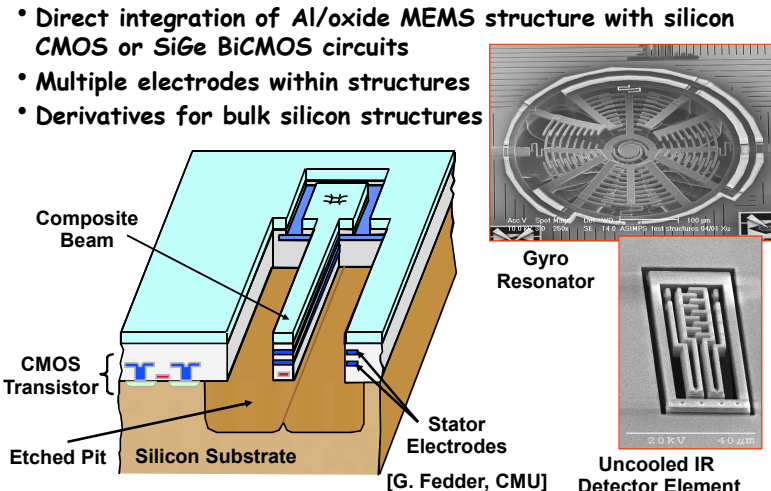
EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 42

42

### ASIMPS Ckt/MEMS Integration Process

UC Berkeley

- Direct integration of Al/oxide MEMS structure with silicon CMOS or SiGe BiCMOS circuits
- Multiple electrodes within structures
- Derivatives for bulk silicon structures



Labels: Composite Beam, CMOS Transistor, Etched Pit, Silicon Substrate, Stator Electrodes

EEC247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 43

43

UC Berkeley

### Effect of Finite Op Amp Gain

Total ADXL-50 Sense C ~ 100ff

Unity Gain Buffer

$V_0$

Handwritten equations:

$$N_0 = A_0(N_i - N_-) = A_0(N_i - N_0) \rightarrow N_0(1 + A_0) = A_0 N_i \rightarrow \frac{N_0}{N_i} = \frac{A_0}{1 + A_0}$$

Get  $Z_i = \frac{V_i}{i_i}$ :  $i_i = (N_i - N_0) s C_p = N_i \left(1 - \frac{A_0}{1 + A_0}\right) s C_p = N_i \frac{1}{1 + A_0} s C_p$

$$\therefore \frac{N_i}{i_i} = Z_i = \frac{1}{s \left[ \frac{C_p}{1 + A_0} \right]} \rightarrow C_{eff} = \frac{C_p}{1 + A_0}$$

No longer zero!

Ex:  $A_0 = 100, C_p = 2 \text{ pF}$   
 $\Rightarrow C_{eff} = \frac{2 \text{ pF}}{101} = 20 \text{ ff}$   
 Not negligible compared w/ ADXL-50 Ctot ~ 100 ff!

EE247B/ME218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 44

44