EE C247B – ME C218 Introduction to MEMS Design Spring 2020

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Module 16: Sensing Ckt. Non-Idealities & Integration

Lecture Outline

- Reading: Senturia Chpt. 14, 15
- Lecture Topics:
  - Ideal Op Amps
  - Op Amp Non-Idealities
  - MEMS-Transistor Integration
    - Mixed
    - MEMS-First
    - MEMS-Last

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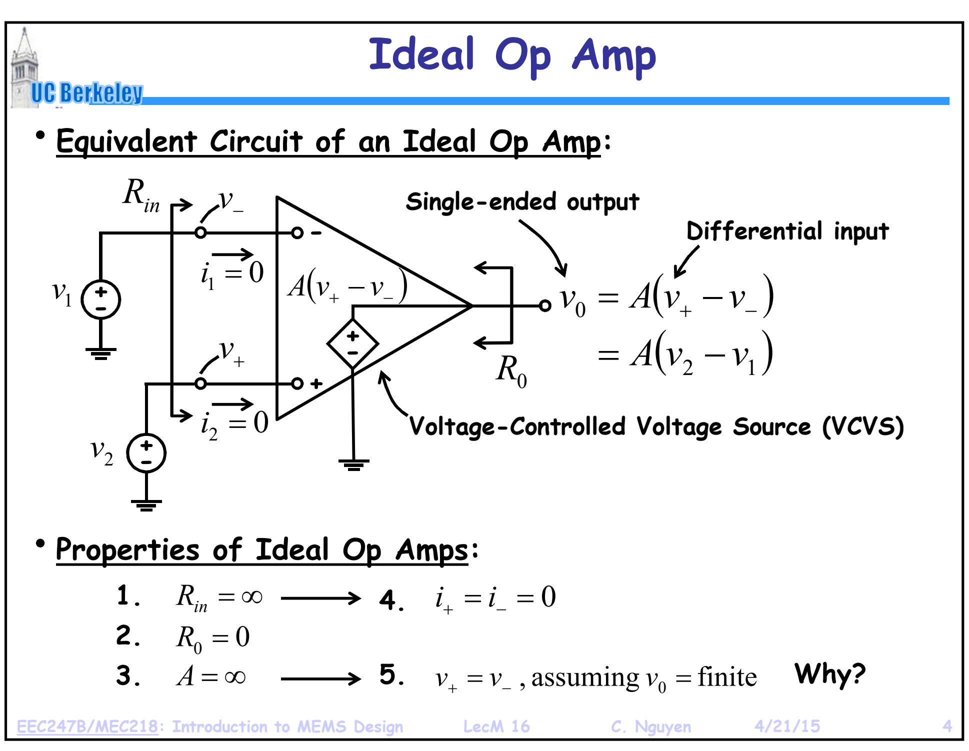

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Ideal Op Amp (cont)

- **Properties of Ideal Op Amps:**

  1. $R_{in} = \infty$ ⟶ 4. $i_+ = i_- = 0$
  2. $R_0 = 0$
  3. $A = \infty$ ⟶ 5. $v_+ = v_-$, assuming $v_0 = \text{finite}$

  Why? Because for

  $$\infty(v_+ - v_-) = v_0 = \text{finite}$$

  $$\therefore v_+ - v_- = 0 \rightarrow v_+ = v_-$$

  $$\underbrace{v_+ - v_-}_{\frac{v_0}{\infty}} \Rightarrow \text{virtual short circuit (virtual ground)}$$

- Big assumption! $(v_0 = \text{finite})$
- How can we assume this? We can assume this only when there is an appropriate negative feedback path!

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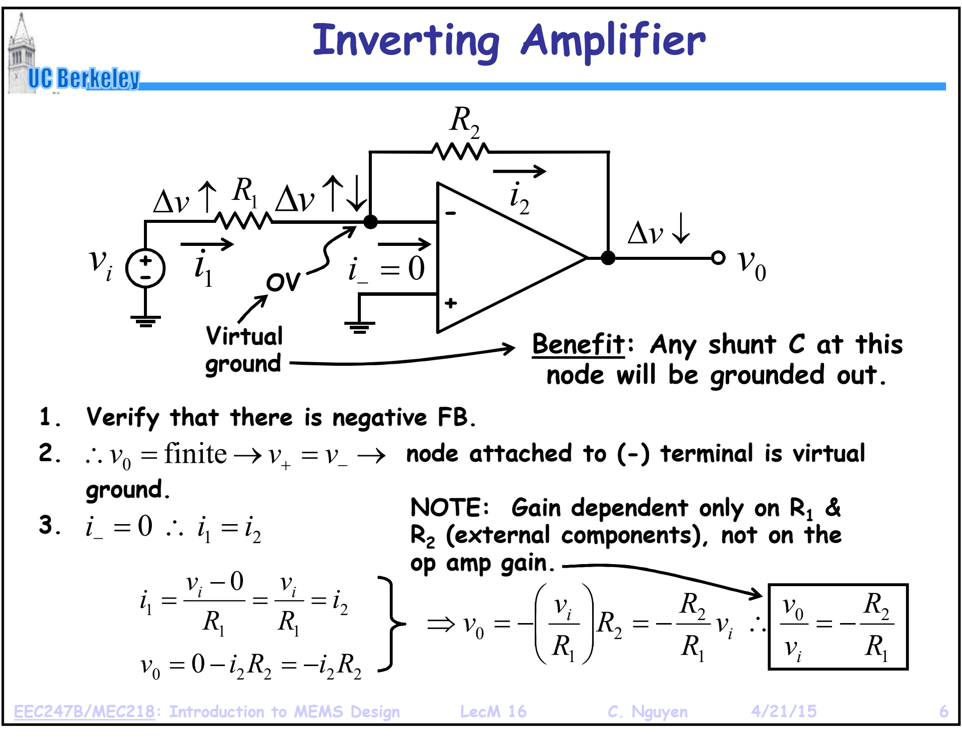
Inverting Amplifier



1. Verify that there is negative FB.
2. $\therefore v_0 = \text{finite} \rightarrow v_+ = v_- \rightarrow$ node attached to (-) terminal is virtual ground.
3. $i_- = 0 \;\therefore\; i_1 = i_2$

NOTE: Gain dependent only on R_1 & R_2 (external components), not on the op amp gain.

$$\left.\begin{array}{l} i_1 = \dfrac{v_i - 0}{R_1} = \dfrac{v_i}{R_1} = i_2 \\ v_0 = 0 - i_2 R_2 = -i_2 R_2 \end{array}\right\} \Rightarrow v_0 = -\left(\frac{v_i}{R_1}\right) R_2 = -\frac{R_2}{R_1} v_i \;\therefore\; \boxed{\frac{v_0}{v_i} = -\frac{R_2}{R_1}}$$

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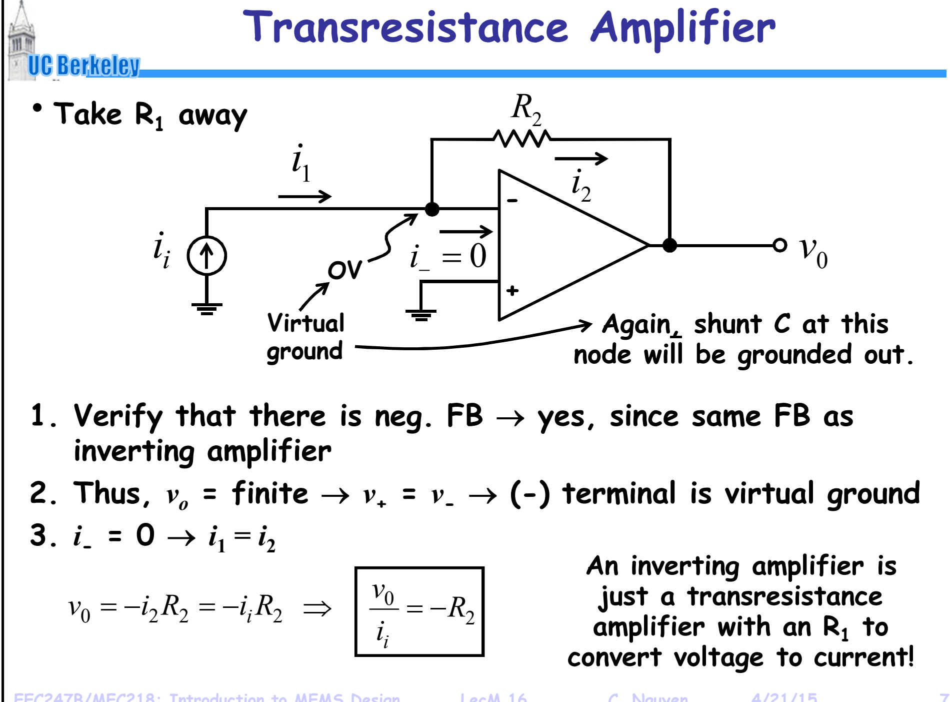

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Non-Ideal Operational Amplifiers

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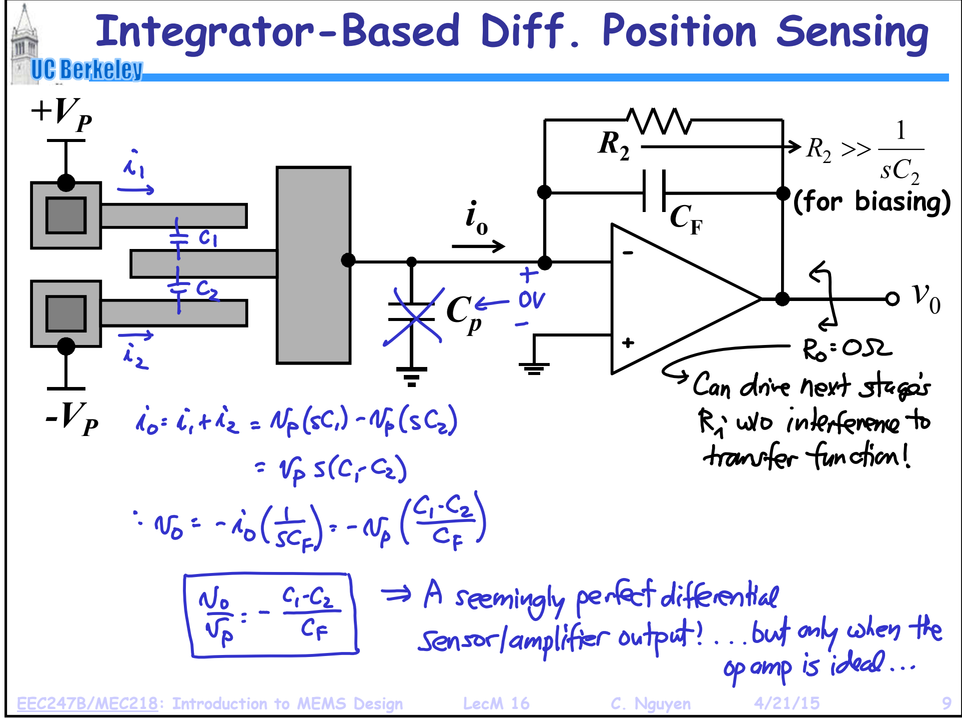

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Actual Op Amps Are Not Ideal

- Actual op amps, of course, are not ideal; rather, they …
  - Generate noise
  - Have finite gain, A_o
  - Have finite bandwidth, ω_b
  - Have finite input resistance, R_i
  - Have finite input capacitance, C_i
  - Have finite output resistance, R_o
  - Have an offset voltage V_{OS} between their (+) and (-) terminals
  - Have input bias currents
  - Have an offset I_{OS} between the bias currents into the (+) and (-) terminals
  - Have finite slew rate
  - Have finite output swing (governed by the supply voltage used, -L to +L)
- And what's worse: All of the above can be temperature (or otherwise environmentally) dependent!

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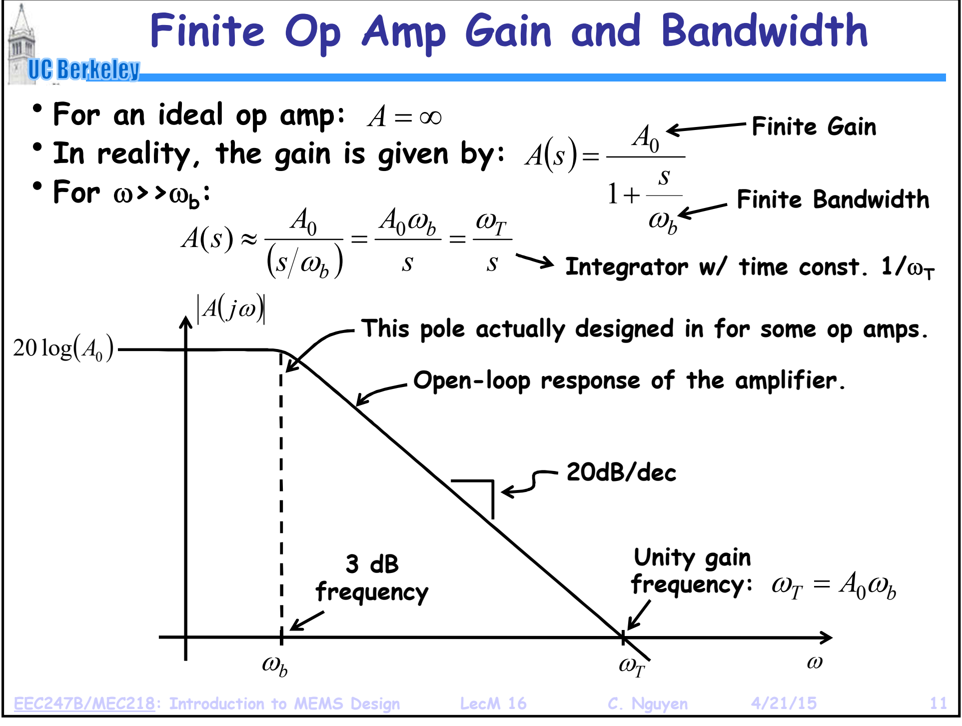

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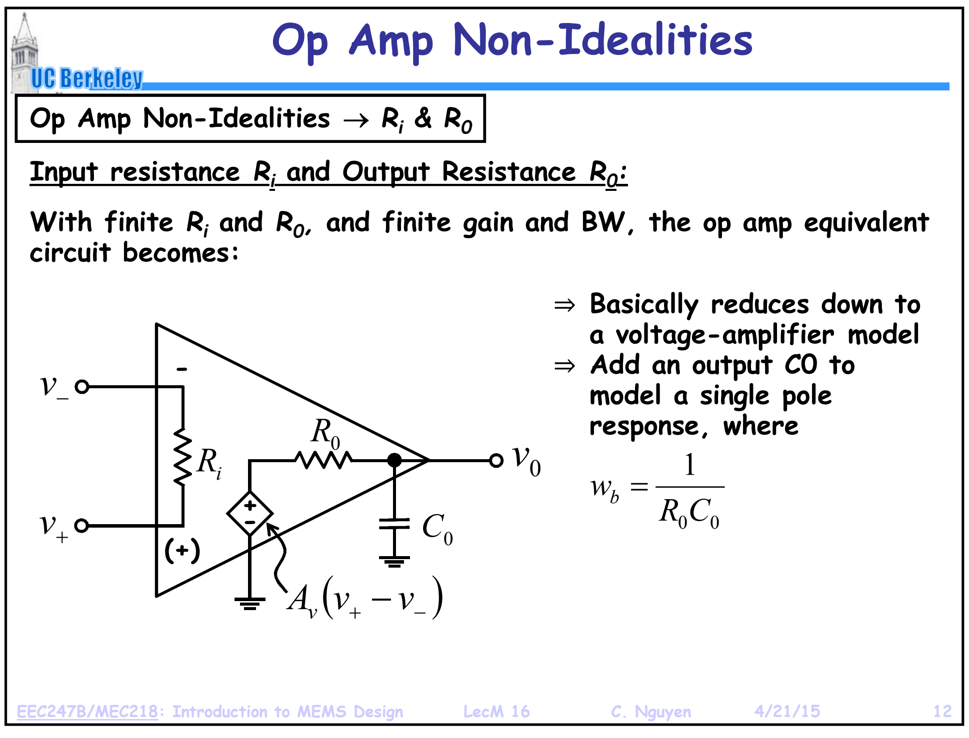

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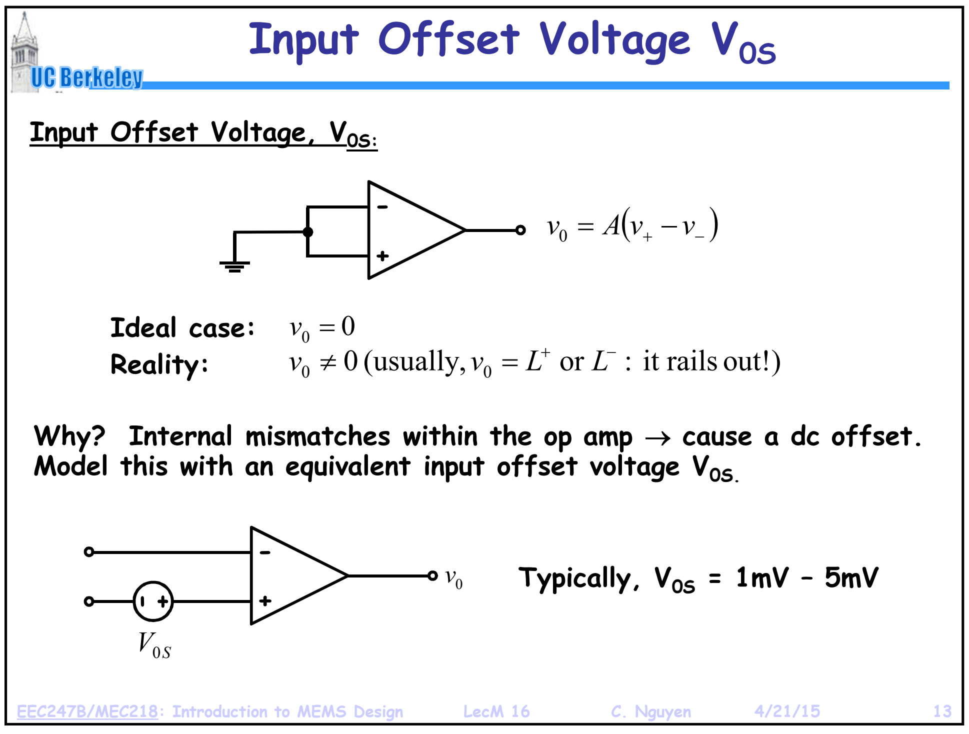

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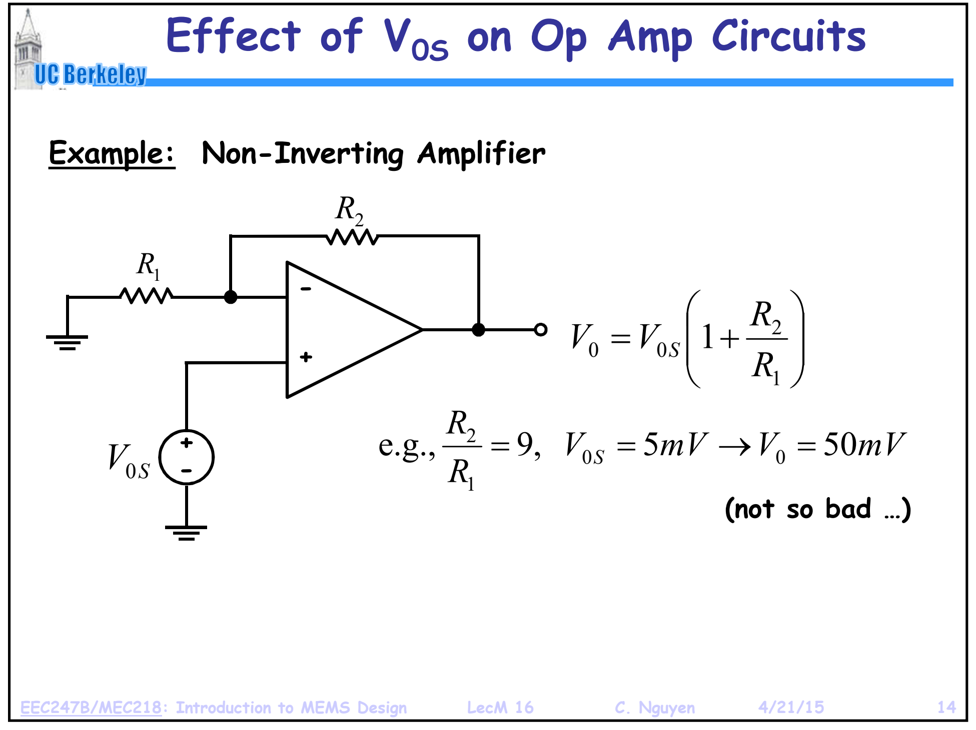

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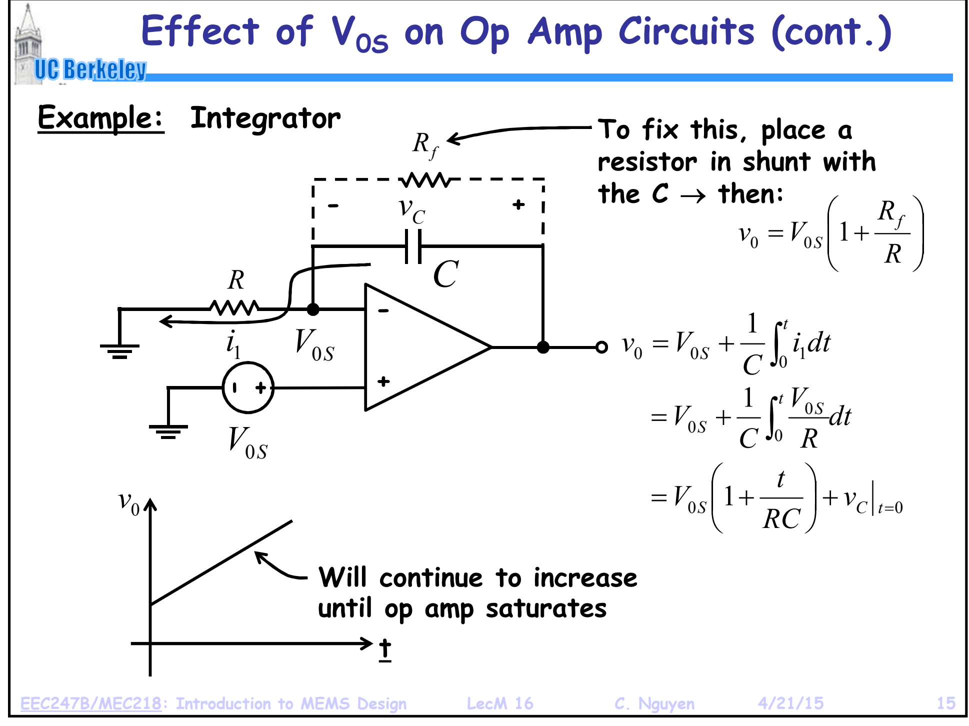

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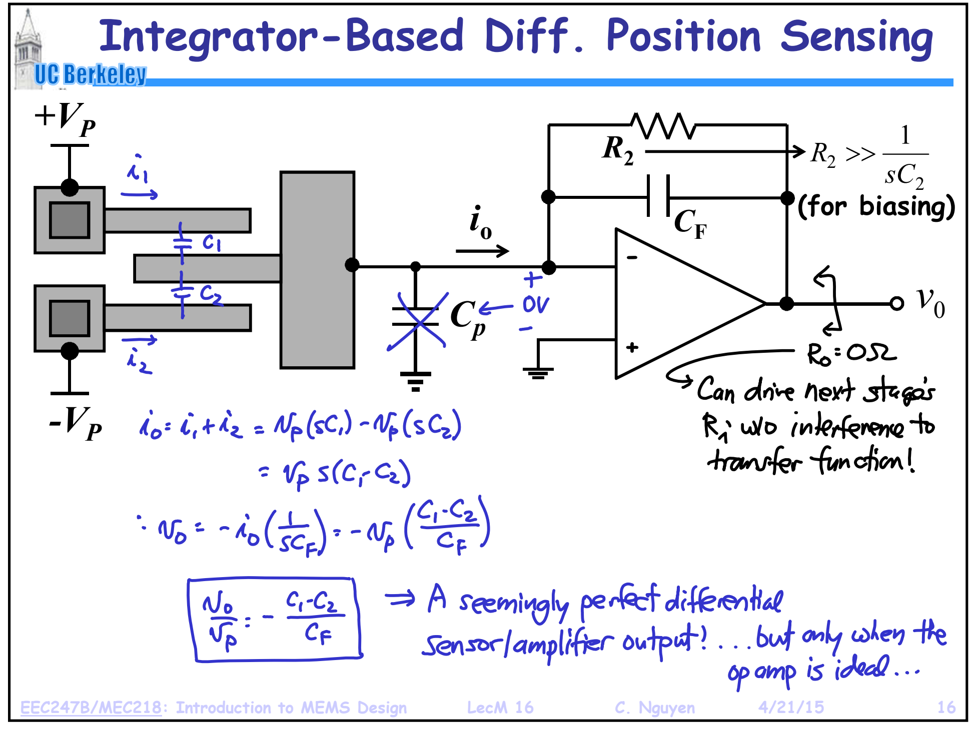

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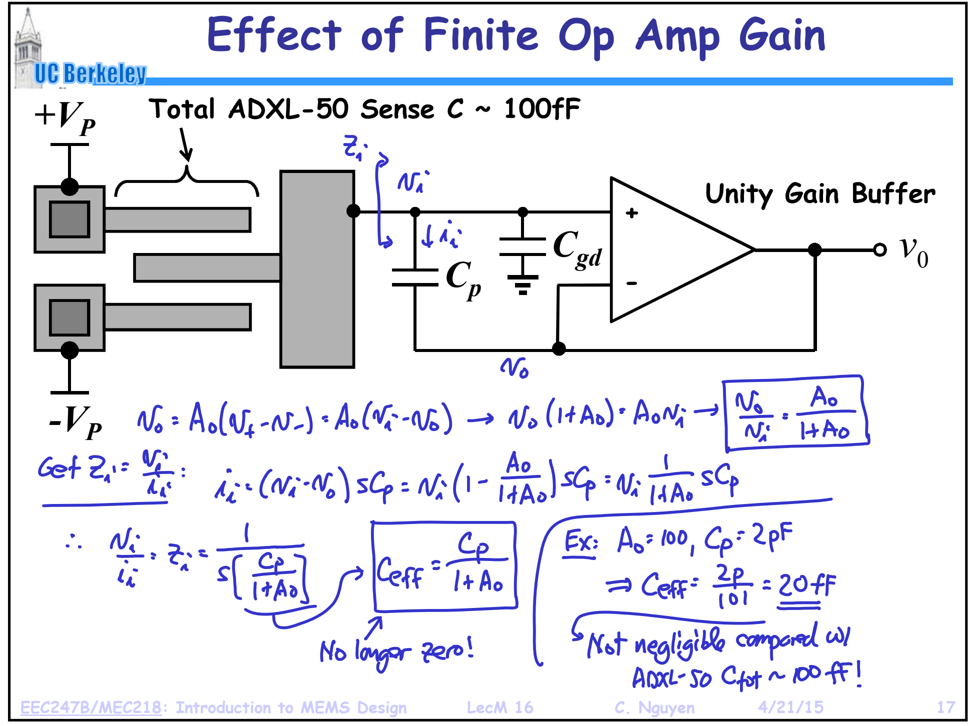

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Integration of MEMS and Transistors

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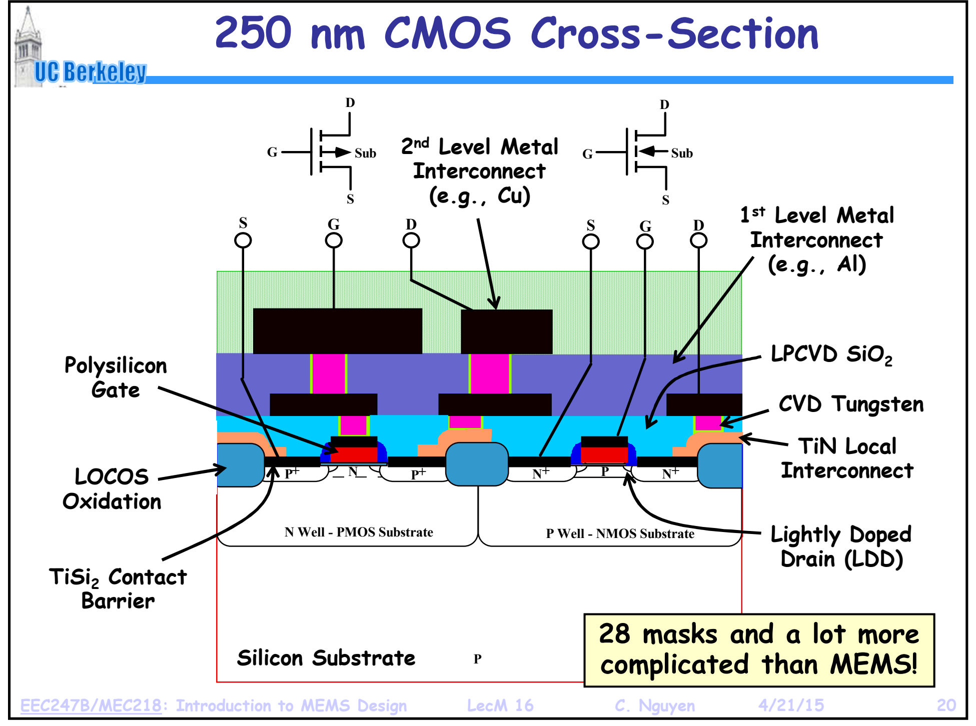
Integrate or Not?

- Benefits:
  - Lower parasitic capacitance and resistance → improved sensitivity and resolution, higher operation frequency
  - Better reliability
  - Reduced size → lower cost?
  - Reduced packaging complexity → integration is a form of packaging → lower cost?
  - Higher integration density supports greater functionality
- Challenges:
  - Temperature ceilings imposed by the transistors or MEMS
  - Protecting one process from the other
  - Surface topography of MEMS
  - Material incompatibilities
  - Multiplication of yield losses (versus non-integrated)
  - Acceptance by transistor foundries

250 nm CMOS Cross-Section



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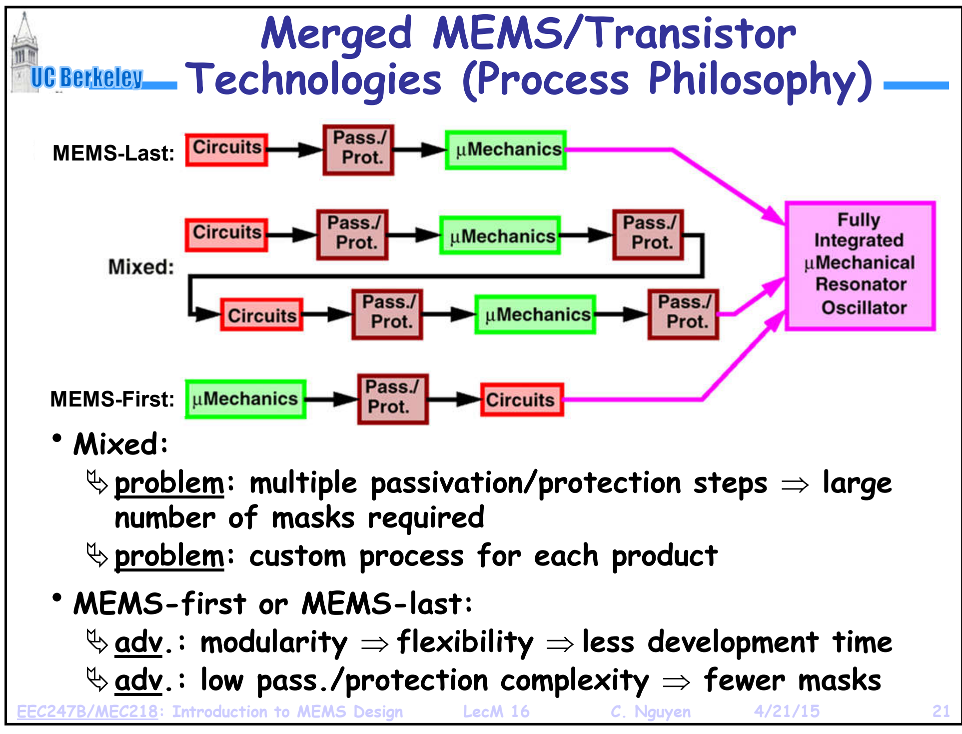

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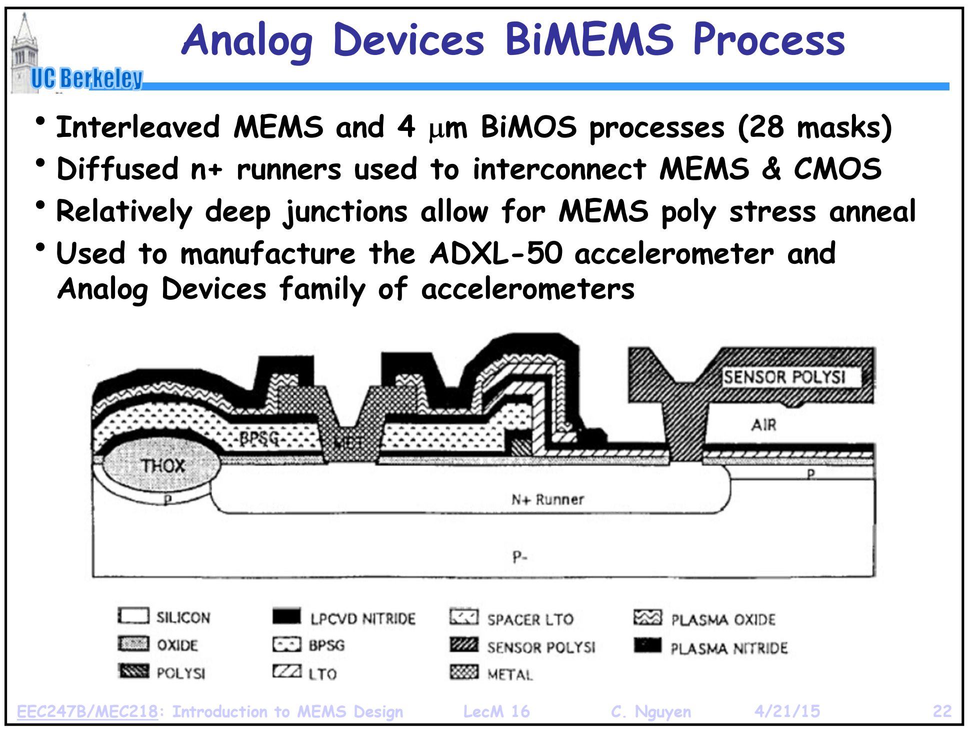

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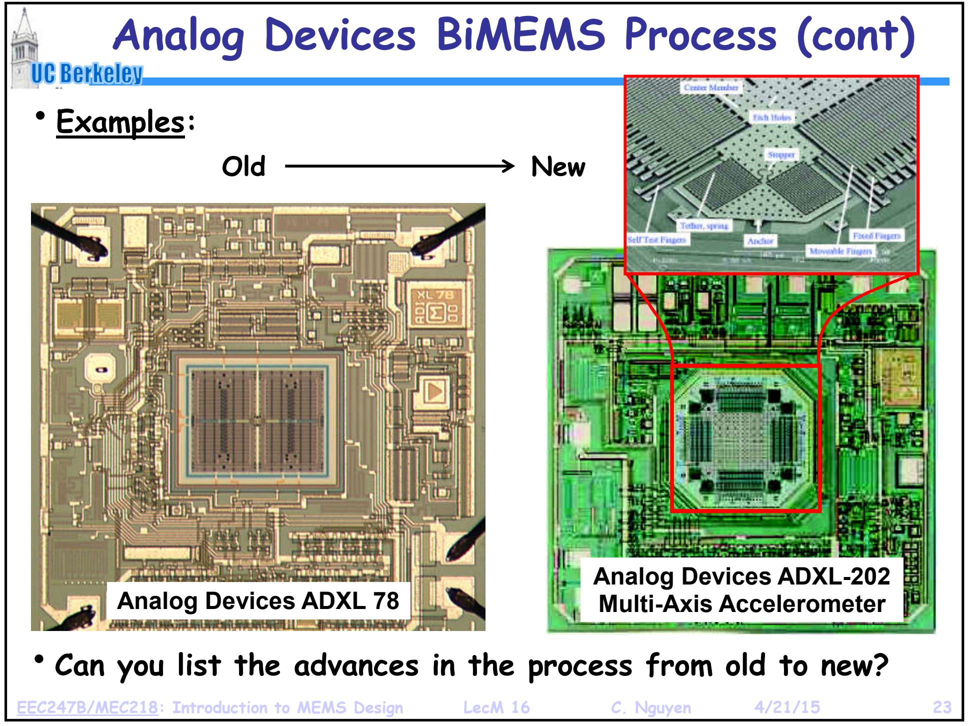

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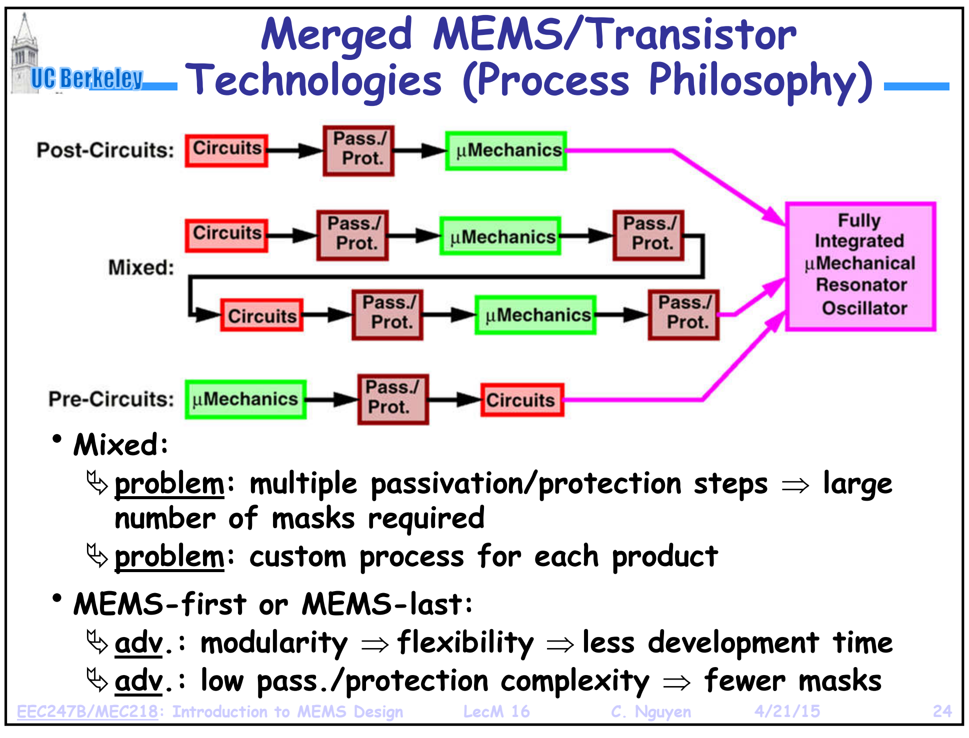

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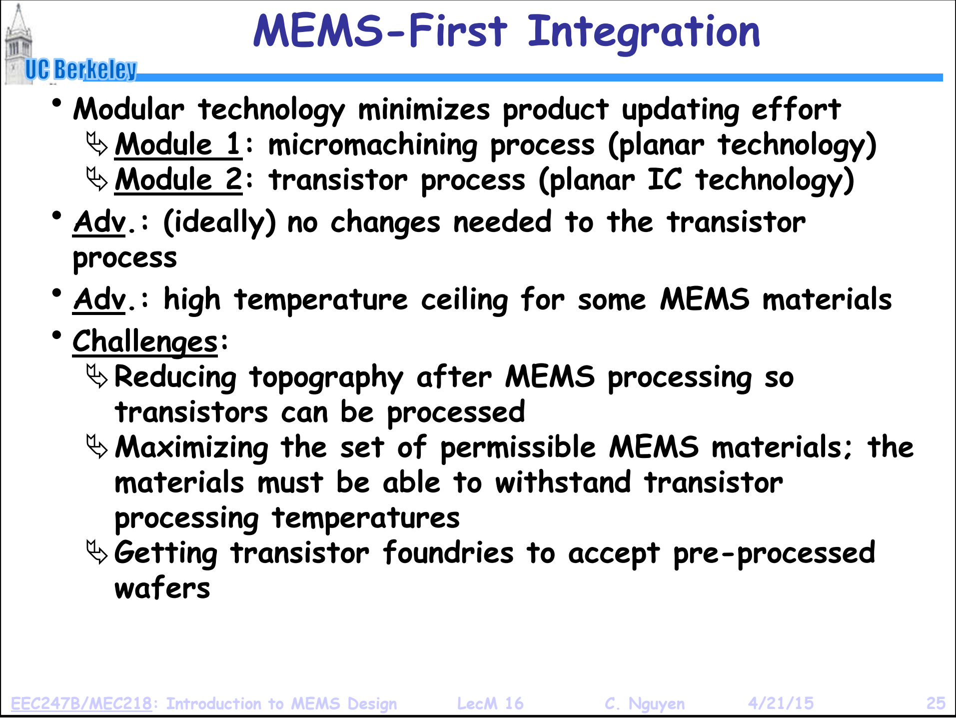

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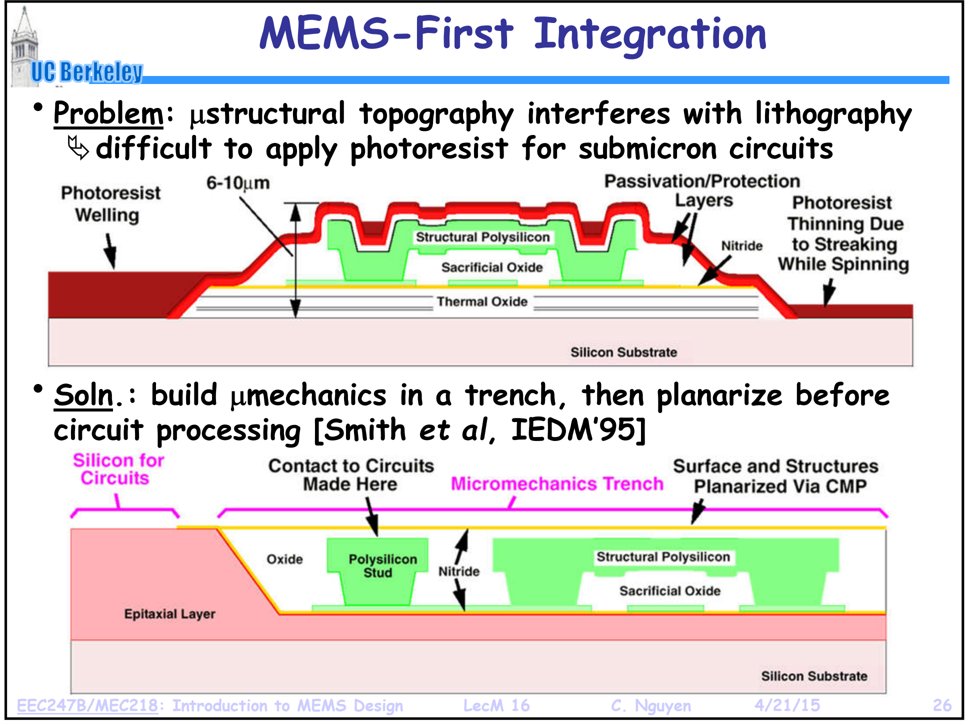

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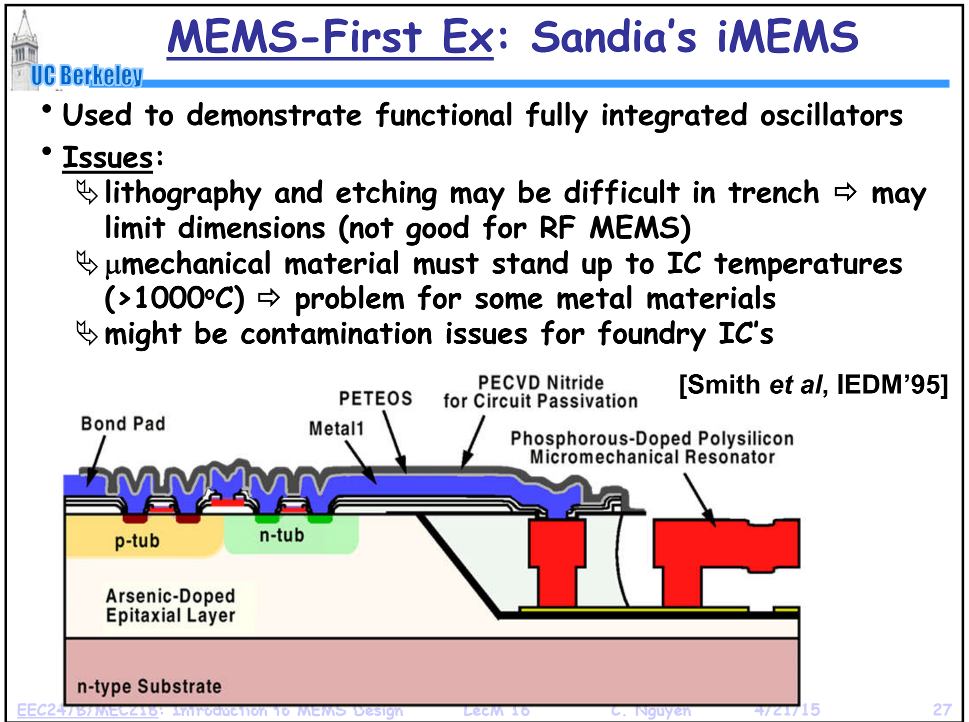

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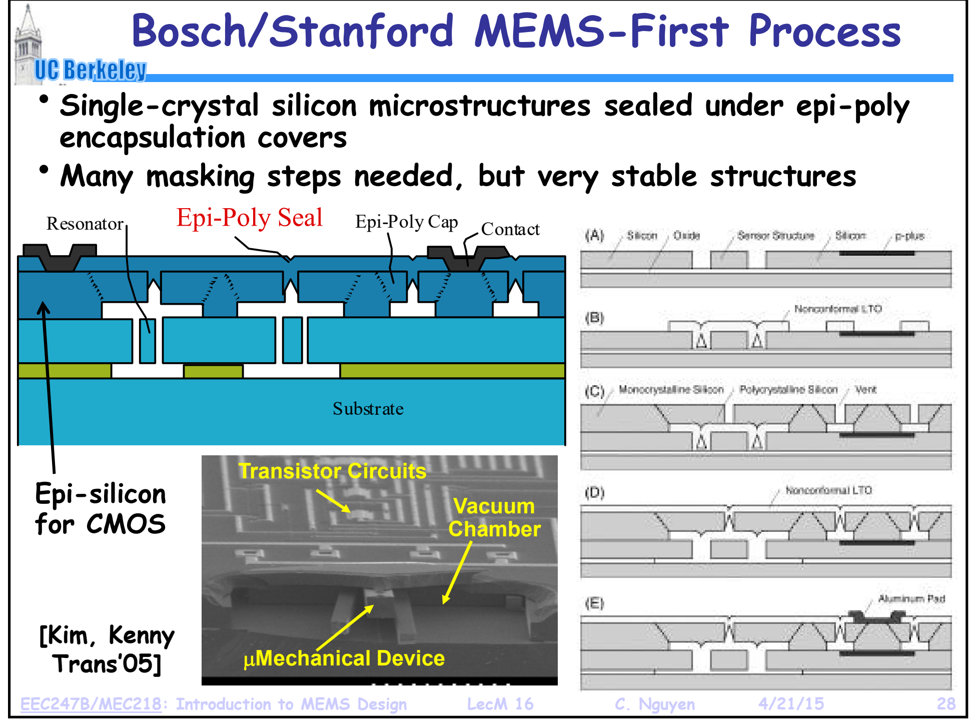

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Problems With MEMS-First

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- Many masking steps needed, plus CMP required → cost can grow if you're not careful
- Processes using trenches sacrifice lithographic resolution in microstructures
- MEMS must withstand transistor processing temperatures
  - Precludes the use of structural materials with low temperature req'mts: metals, polymers, etc.
- Exotic MEMS (e.g., ZnO) that can contaminate transistors during their processing are not permissible
  - thus, not truly modular
- Foundry acceptance not guaranteed and might be rare

Foundry Acceptance of MEMS-First?

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- Is a CMP'ed silicon surface sufficiently pure for fabrication of aggressively scaled transistors? How about if an oxide is grown over the CMP'ed surface and removed via a wet etch to yield a "pristine" surface?
- Is epi silicon grown as part of a sealing process sufficiently pure for fabrication of aggressively scaled transistors?
- CMOS is many times more difficult to run than MEMS
  - Feature sizes on the nm scale for billions of devices
  - Contamination a big issue: many foundries may not accept pre-processed wafers for contamination reasons
  - Many foundries will not accept any pre-processed wafers, MEMS or not → just can't guarantee working transistor circuits with unknowns in starting silicon

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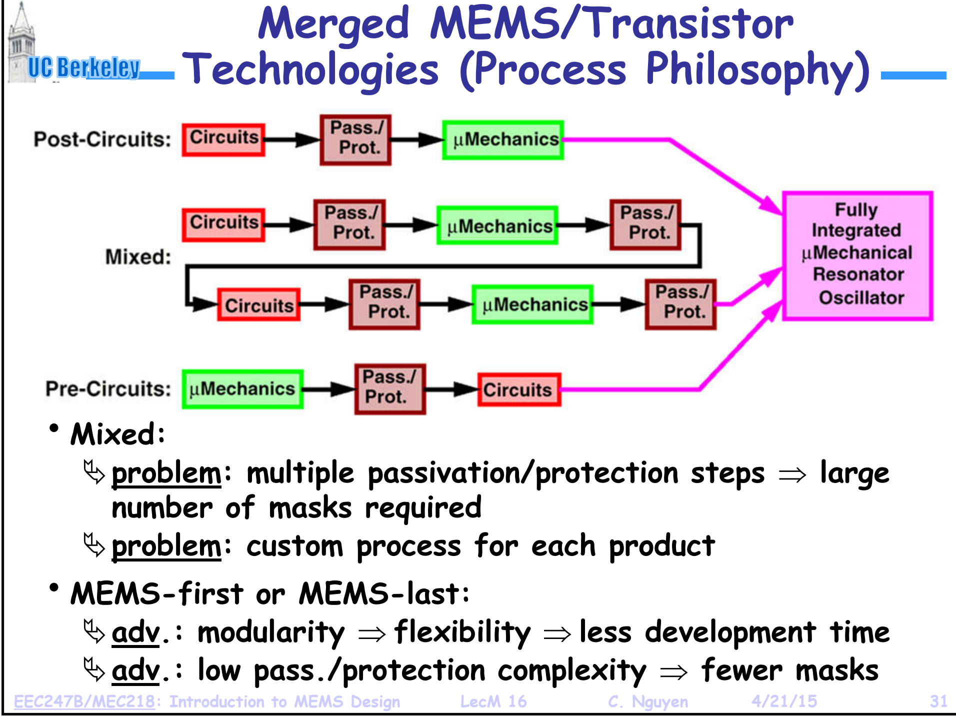

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MEMS-Last Integration

- Modular technology minimizes product updating effort
  - ↳ Module 1: transistor process (planar IC technology)
  - ↳ Module 2: micromachining process (planar technology)
- Adv.: foundry friendly
  - ↳ Virtually any foundry can be used → can use the lowest cost transistor circuits (big advantage)
- Adv.: topography after circuit fabrication is quite small, especially given the use of CMP to planarize the metallization layers
- Issue: limited thermal budget limits the set of usable structural materials
  - ↳ Metallization goes bad if temperature gets too high
  - ↳ Aluminum grows hillocks and spikes junctions if T>500°C
  - ↳ Copper diffusion can be an issue at high temperature
  - ↳ Low-k dielectrics used around metals may soon lower the temperature ceiling to only 320°C

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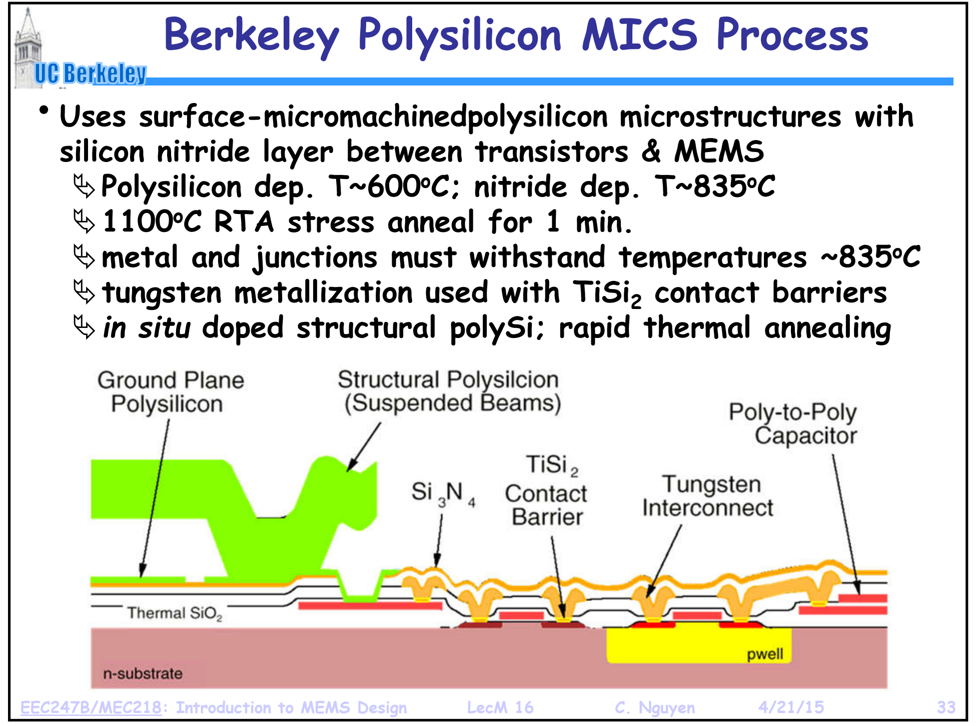

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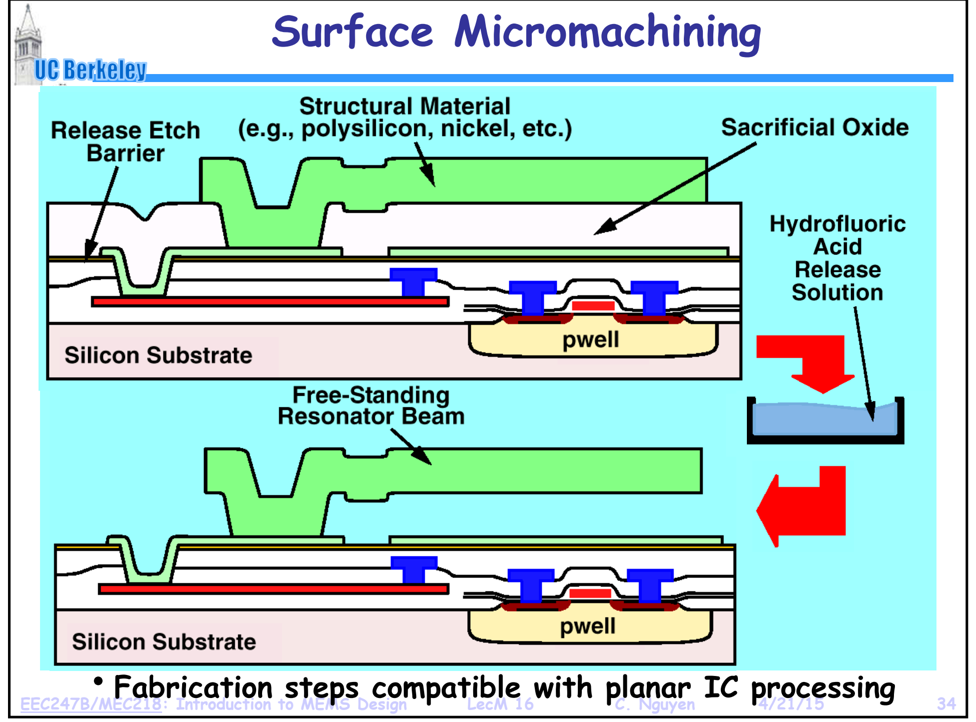

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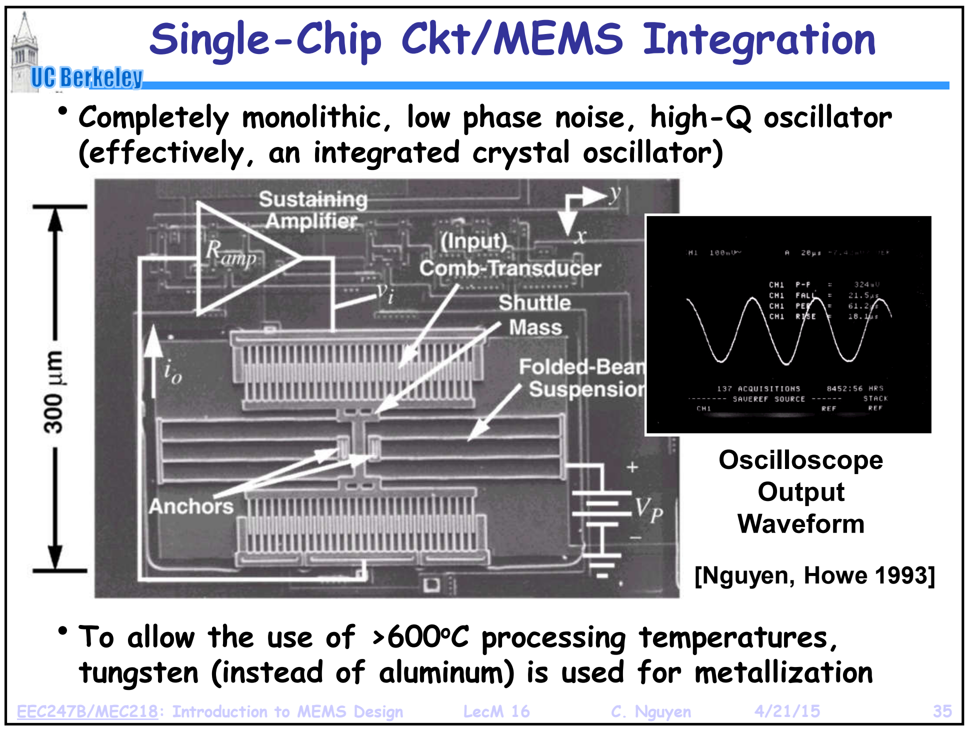

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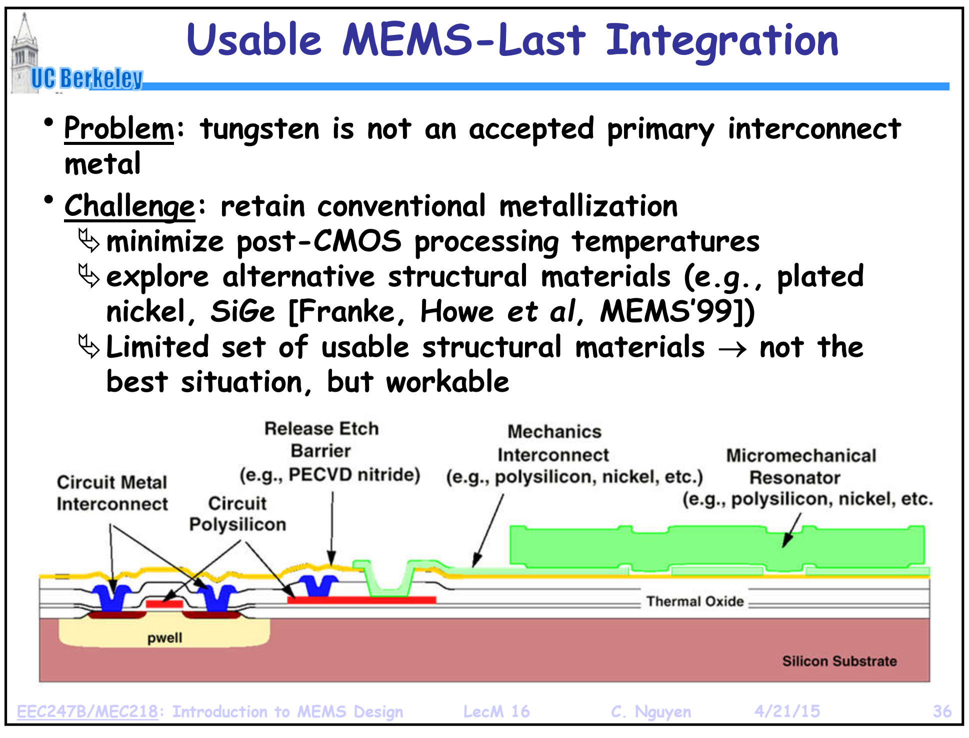

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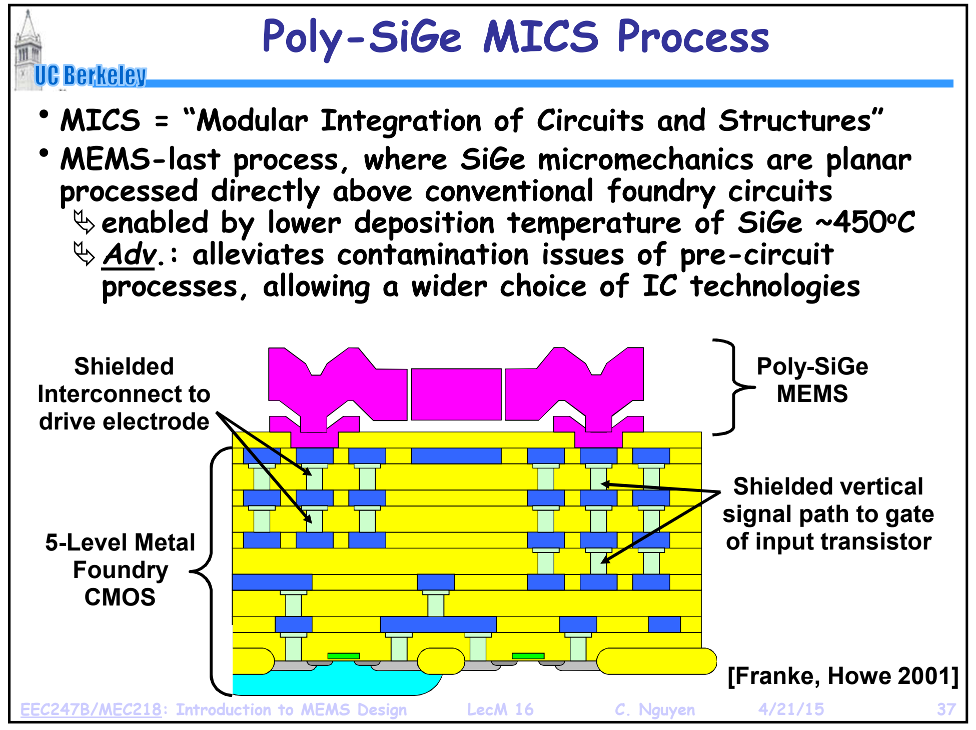

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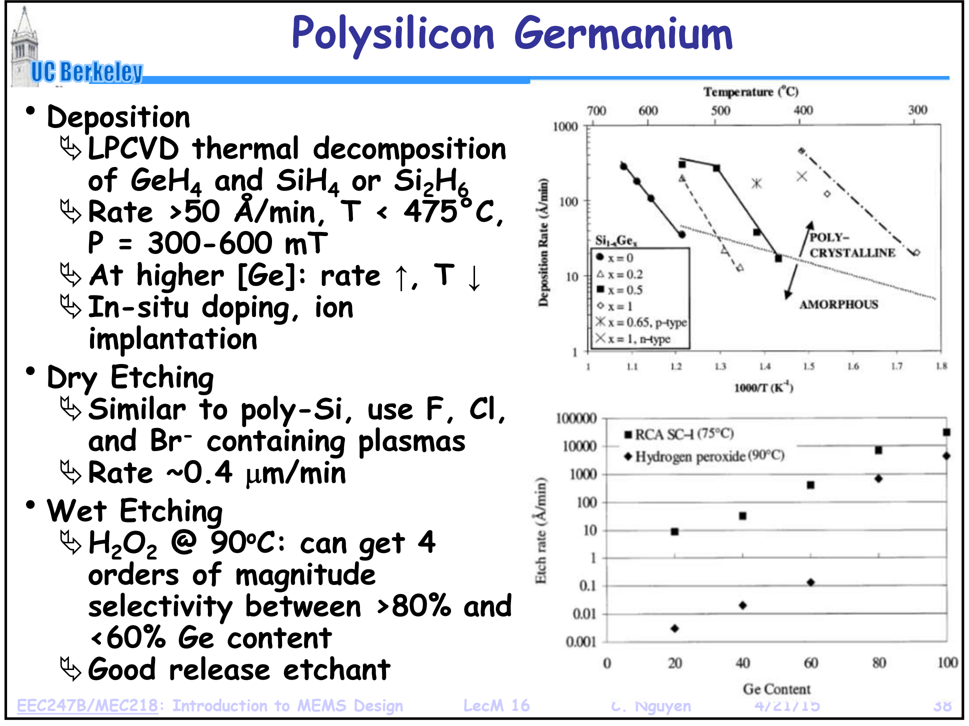

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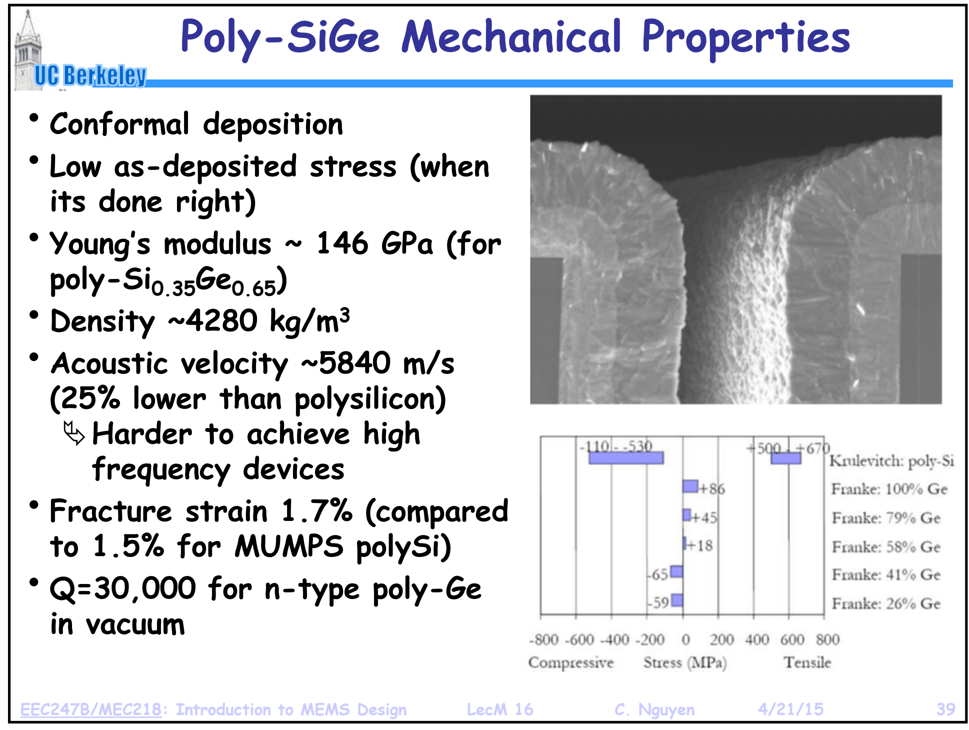

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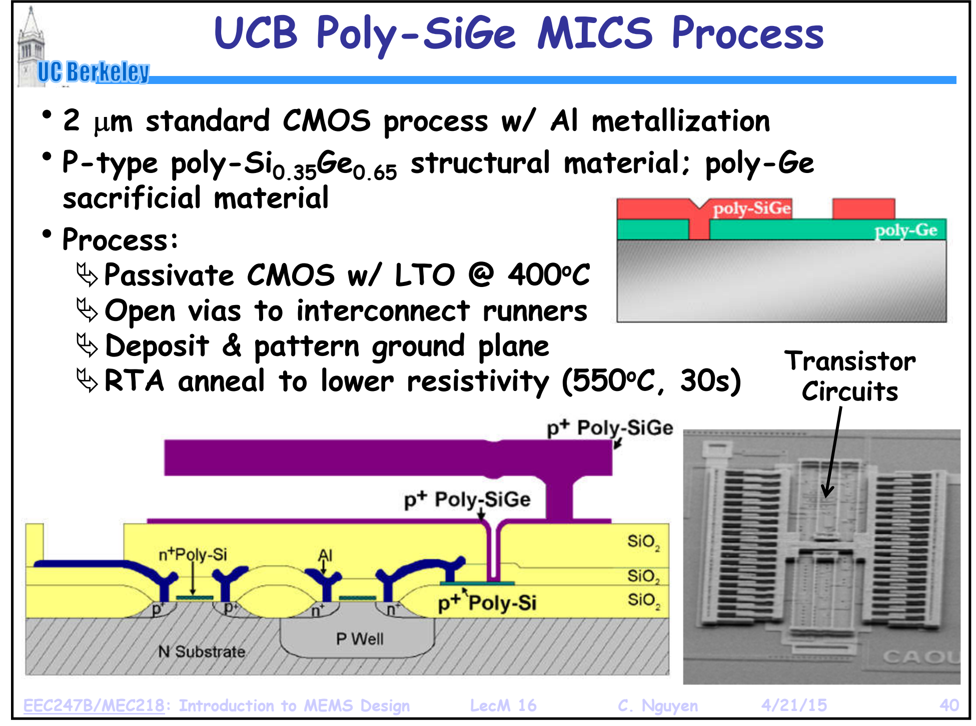

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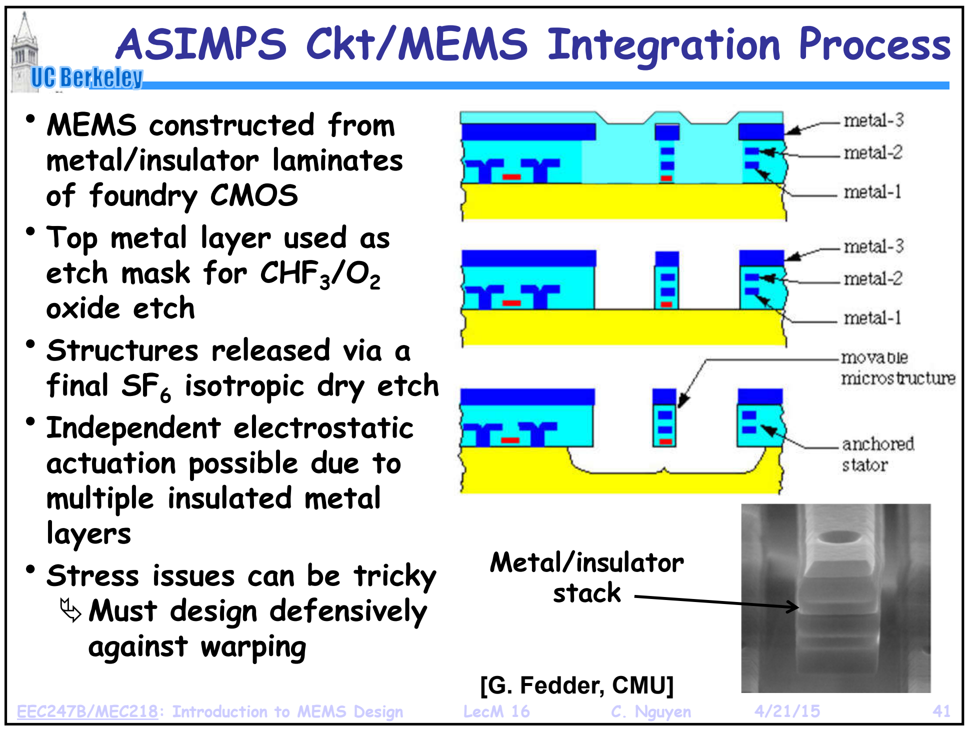

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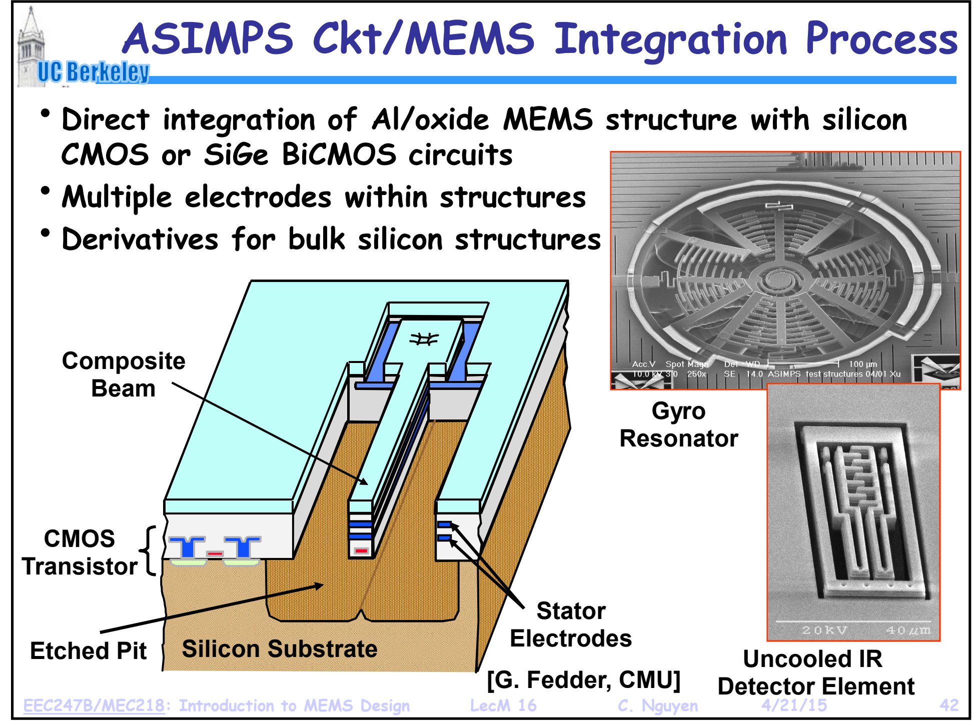

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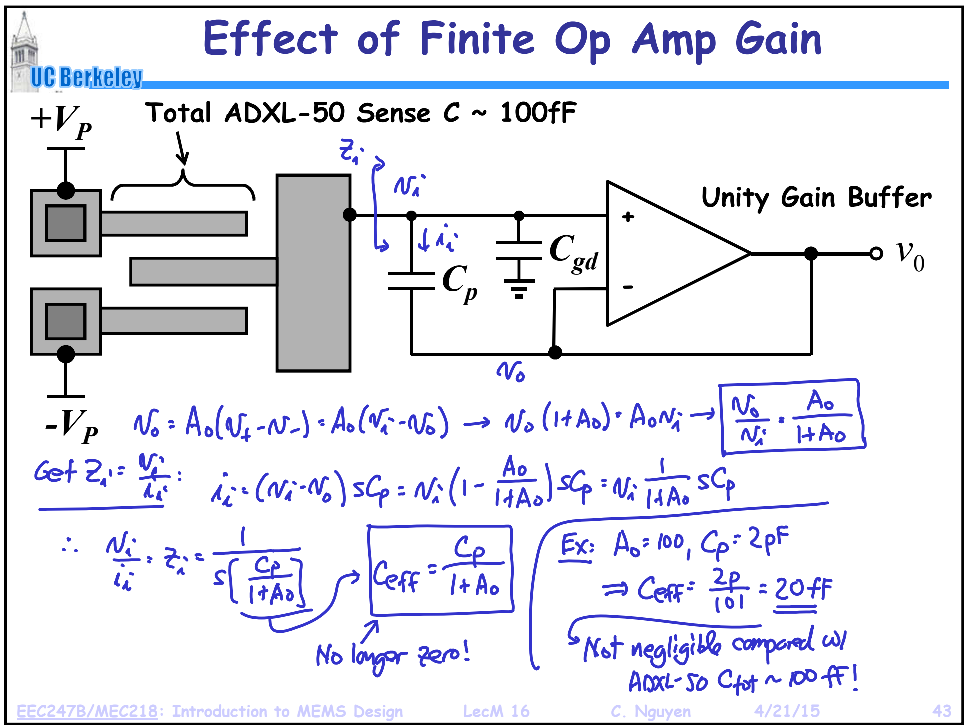

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