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EE C247B – ME C218
Introduction to MEMS Design
Spring 2020

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Lecture Module 6: Bulk Micromachining

1

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Lecture Outline

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handouts: "Bulk Micromachining of Silicon"
- Lecture Topics:
  - Bulk Micromachining
  - Anisotropic Etching of Silicon
  - Boron-Doped Etch Stop
  - Electrochemical Etch Stop
  - Isotropic Etching of Silicon
  - Deep Reactive Ion Etching (DRIE)
  - Wafer Bonding

2

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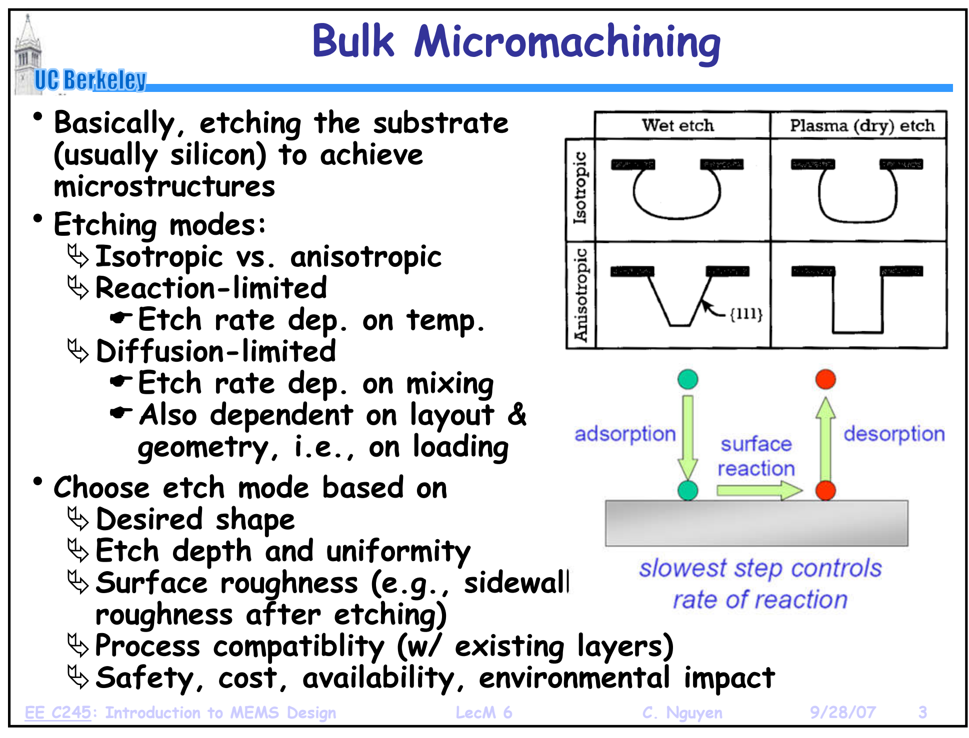

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Mechanical Properties of Silicon

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- Crystalline silicon is a hard and brittle material that deforms elastically until it reaches its yield strength, at which point it breaks.
  - Tensile yield strength = 7 GPa (~1500 lb suspended from 1 mm^2)
  - Young's Modulus near that of stainless steel
  - {100} = 130 GPa; {110} = 169 GPa; {111} = 188 GPa
  - Mechanical properties uniform, no intrinsic stress
  - Mechanical integrity up to 500°C
  - Good thermal conductor
  - Low thermal expansion coefficient
  - High piezoresistivity

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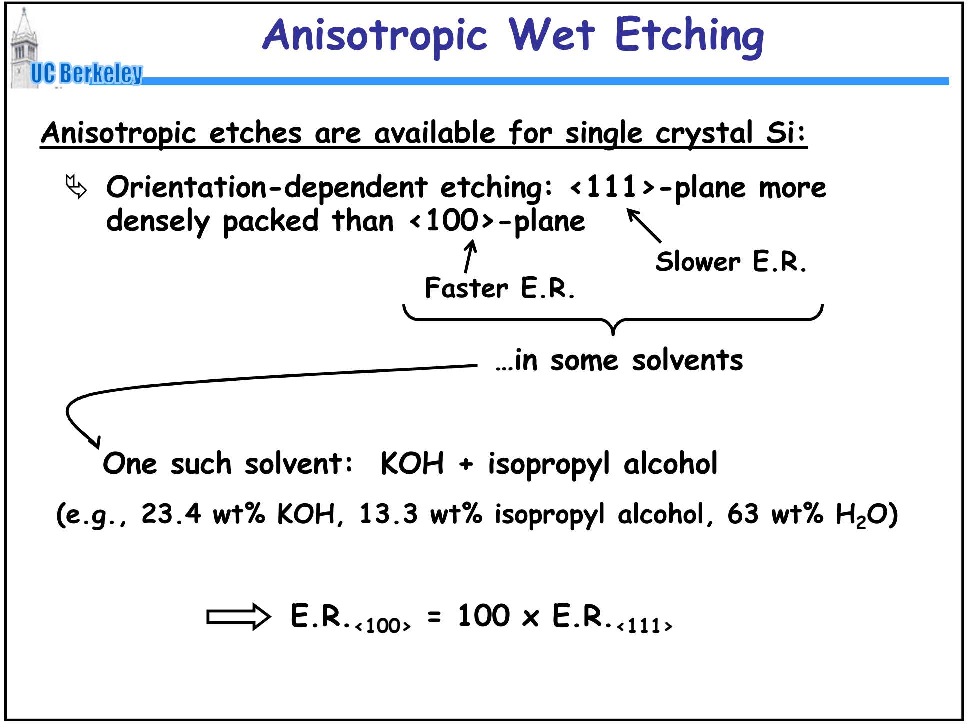

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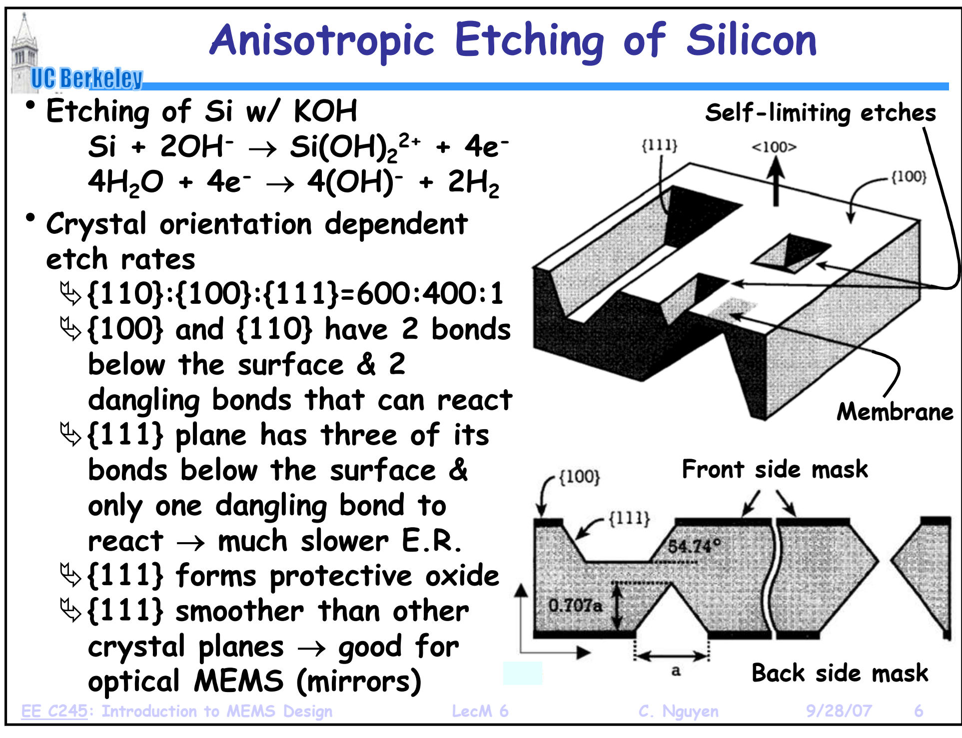

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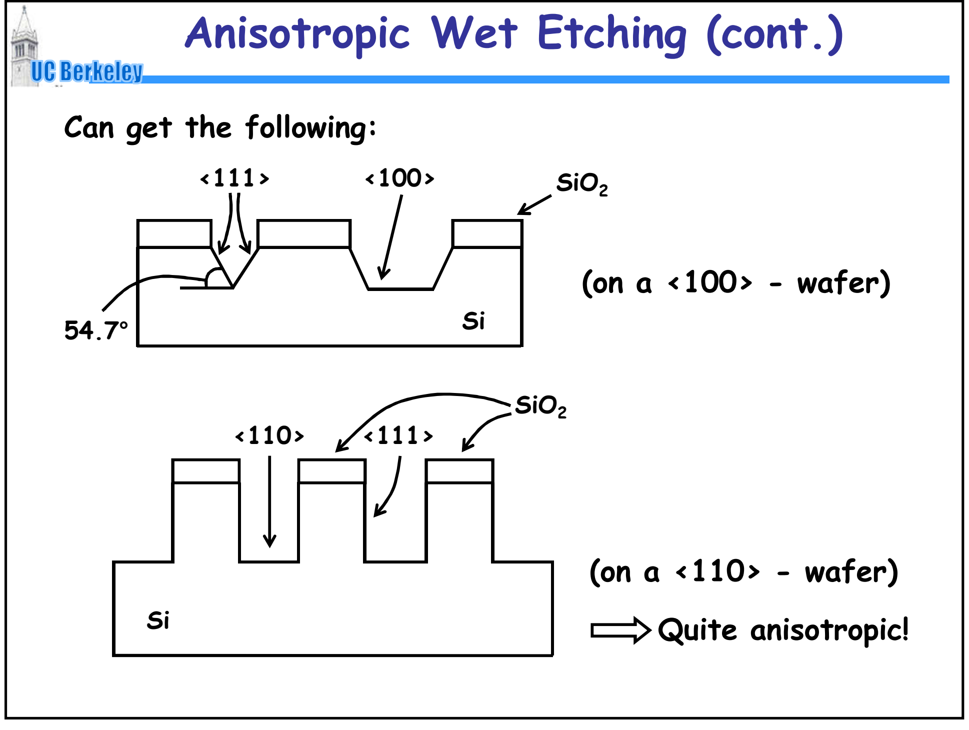

7

Anisotropic Etching of Silicon

Photoresist
Nitride Mask
Silicon Substrate
Opening to Silicon
Silicon Substrate
(100)
Silicon Substrate

- Deposit nitride:
  - Target = 100nm
  - 22 min. LPCVD @800°C
- Lithography to define areas of silicon to be etched
- Etch/pattern nitride mask
  - RIE using SF_6
  - Remove PR in PRS2000
- Etch the silicon
  - Use 1:2 KOH:H_2O (wt.), stirred bath @ 80°C
  - Etch Rates:
    - (100) Si → 1.4 μm/min
    - Si_3N_4 → ~ 0 nm/min
    - SiO_2 → 1-10 nm/min
    - Photoresist, Al → fast
- Micromasking by H_2 bubbles leads to roughness
  - Stir well to displace bubbles
  - Can also use oxidizer for (111) surfaces
  - Or surfactant additives to suppress bubble formation

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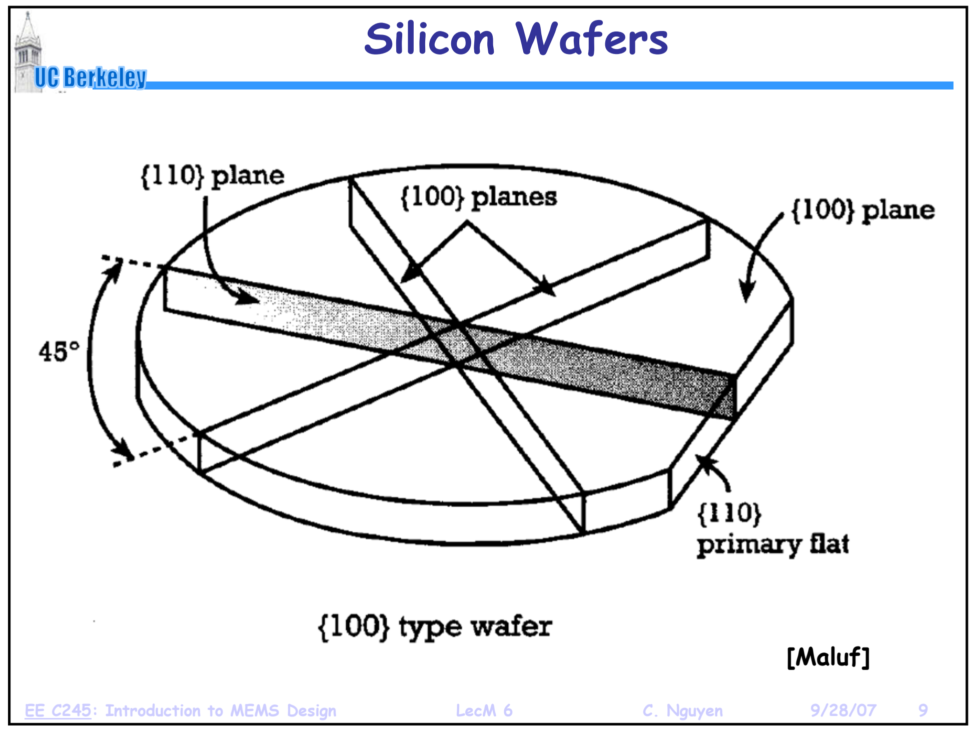

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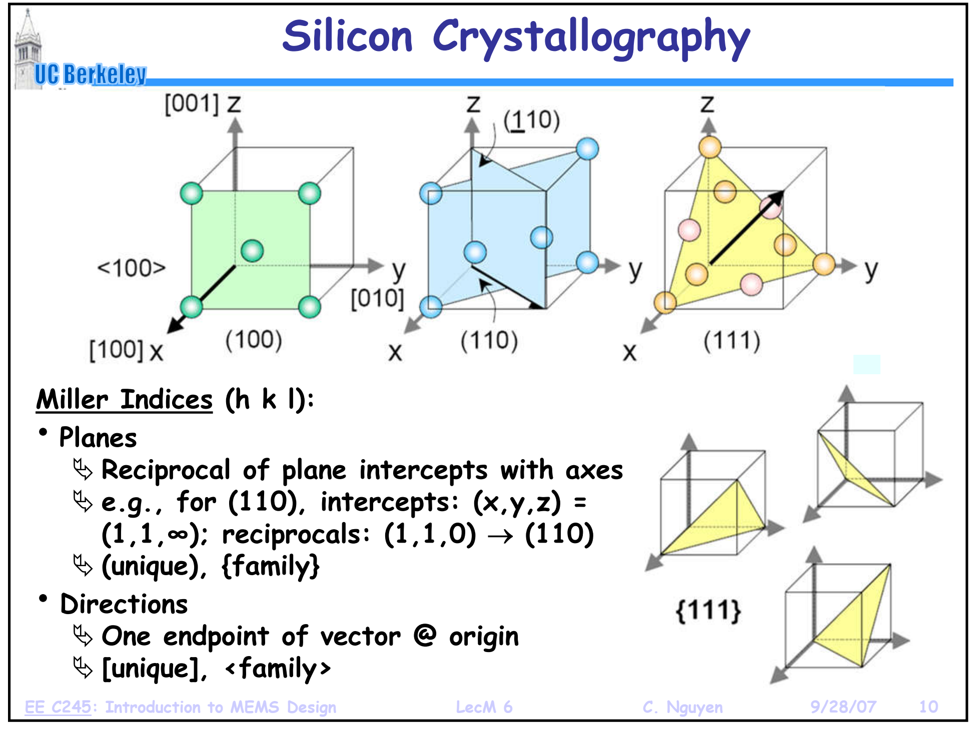

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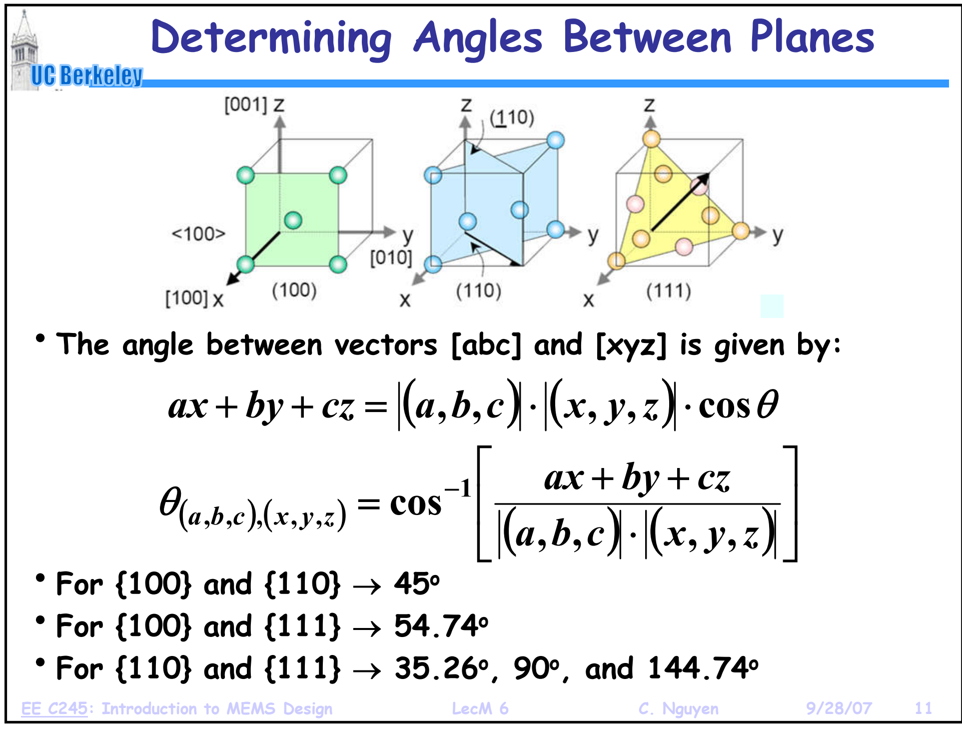

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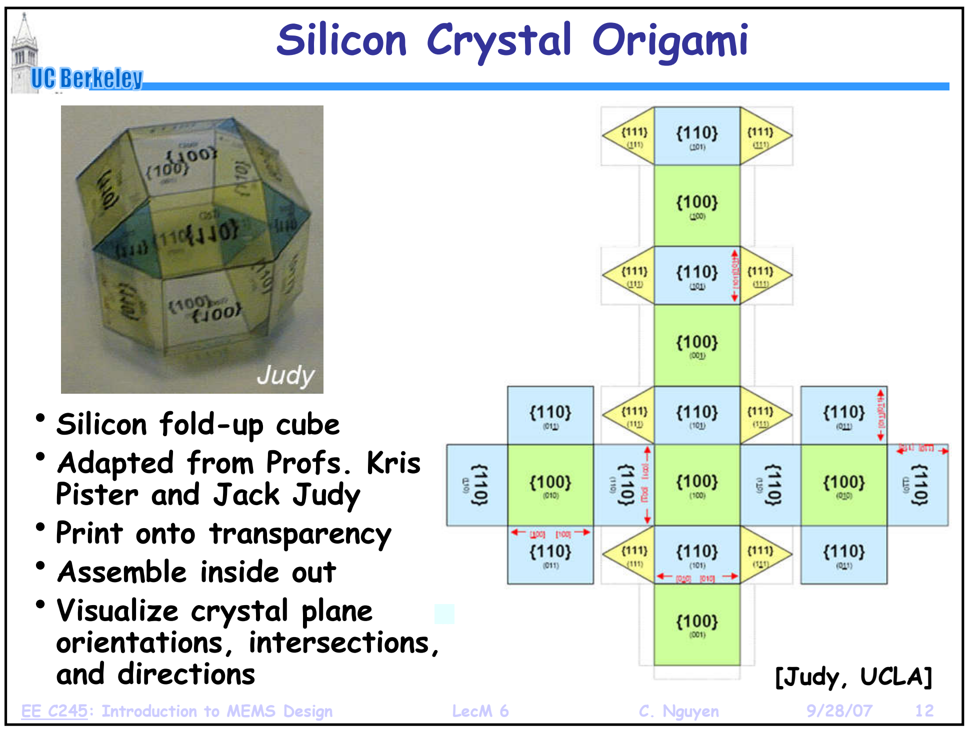

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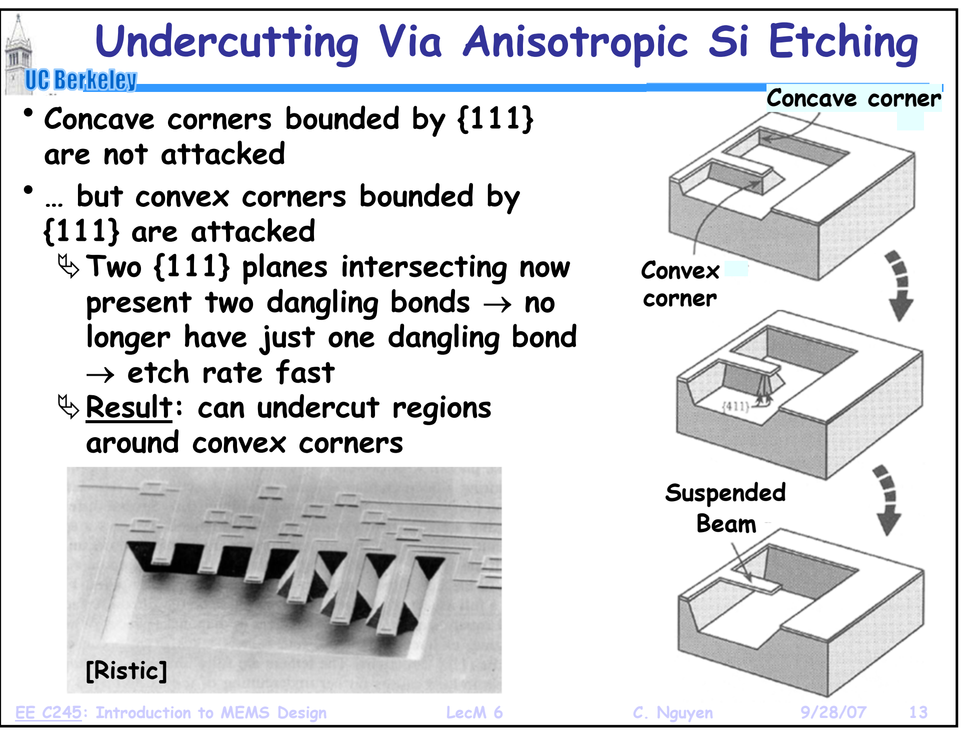

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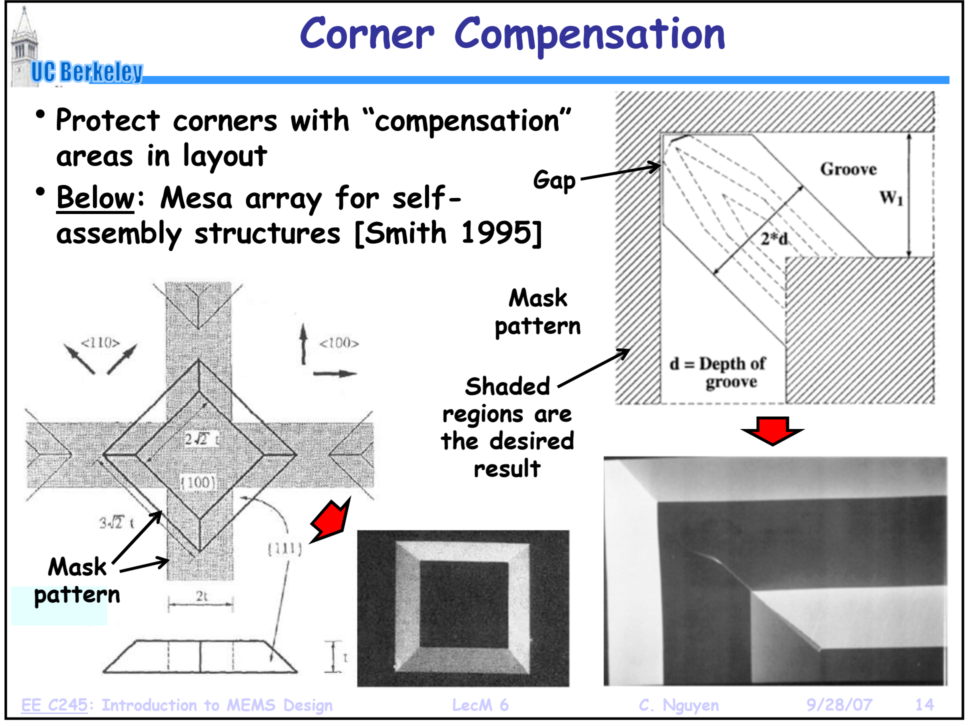

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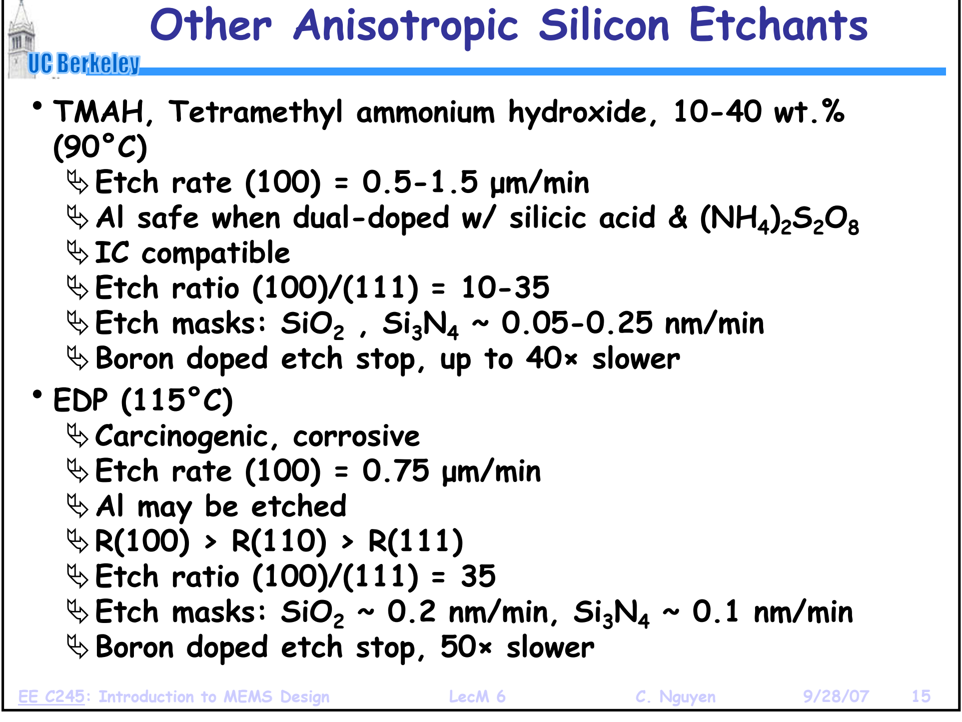

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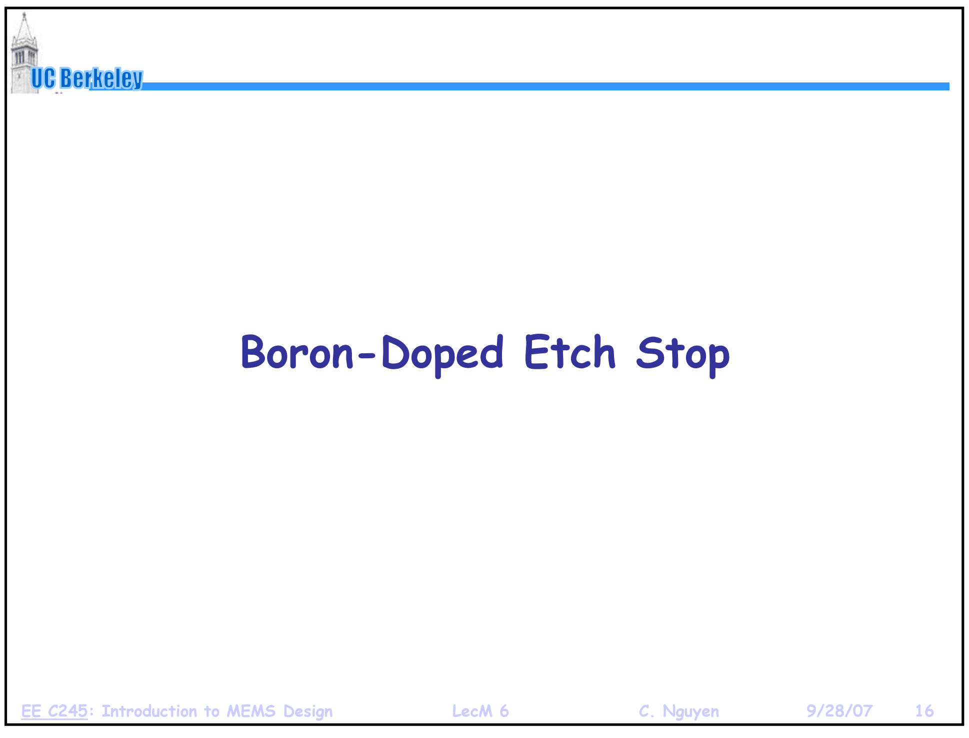

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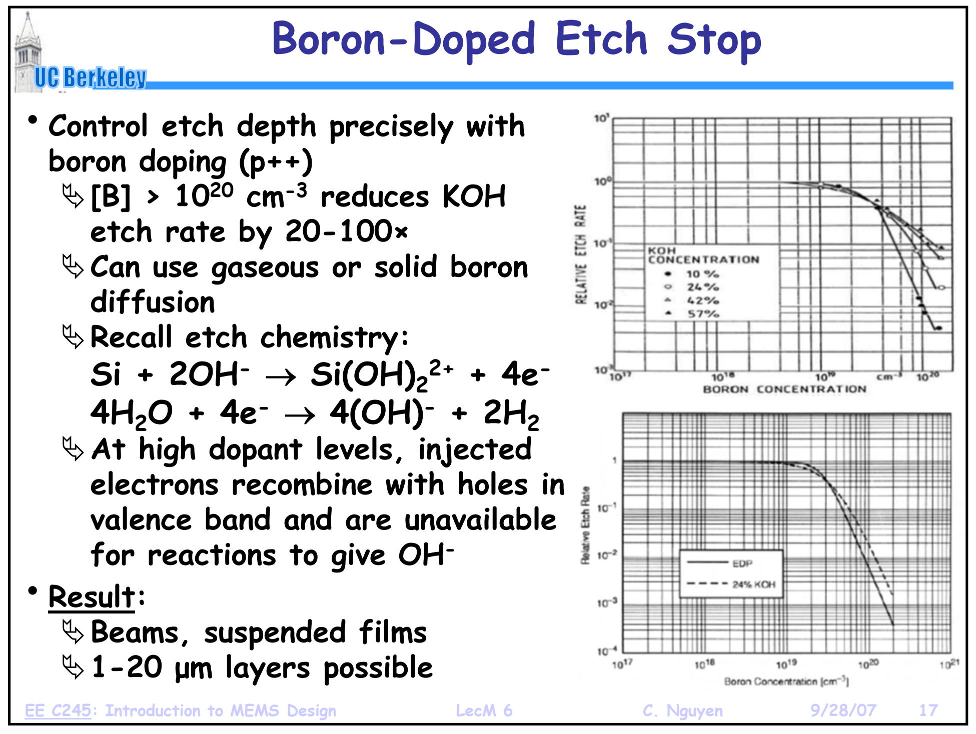

17

Ex: Micronozzle

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- Micronozzle using anisotropic etch-based fabrication
- Used for inkjet printer heads

Silicon frame
p++ silicon
Resist
p++ silicon
Silicon
1. Pattern mask
2. Etch circle in p++
Silicon nitride
3. Mask front side
4. Anisotropic etch

[Maluf]

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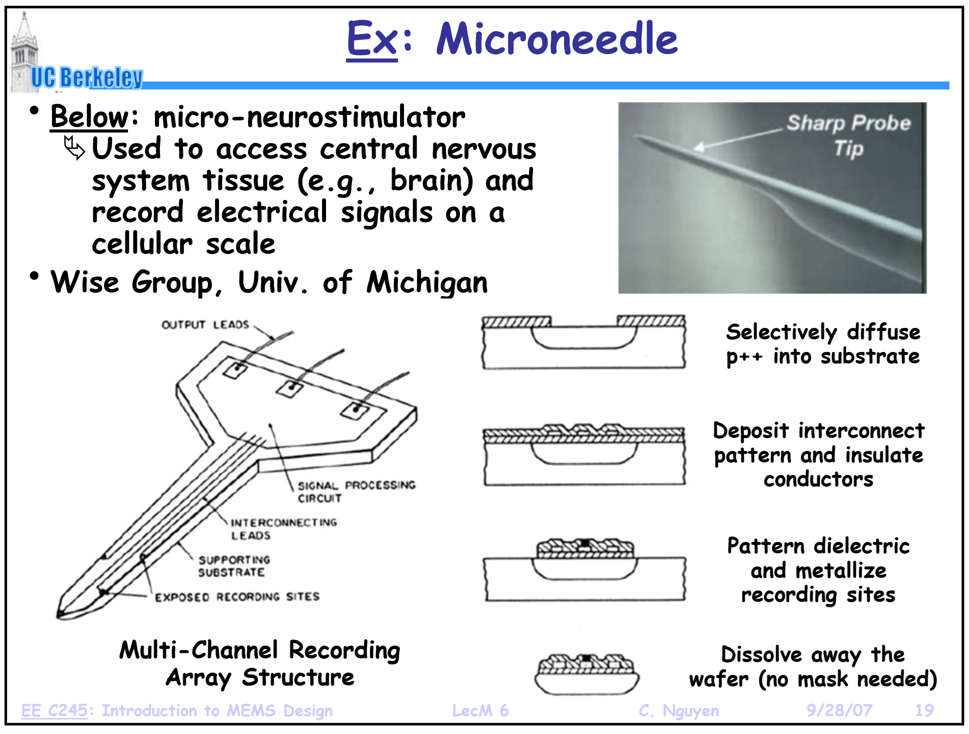
18



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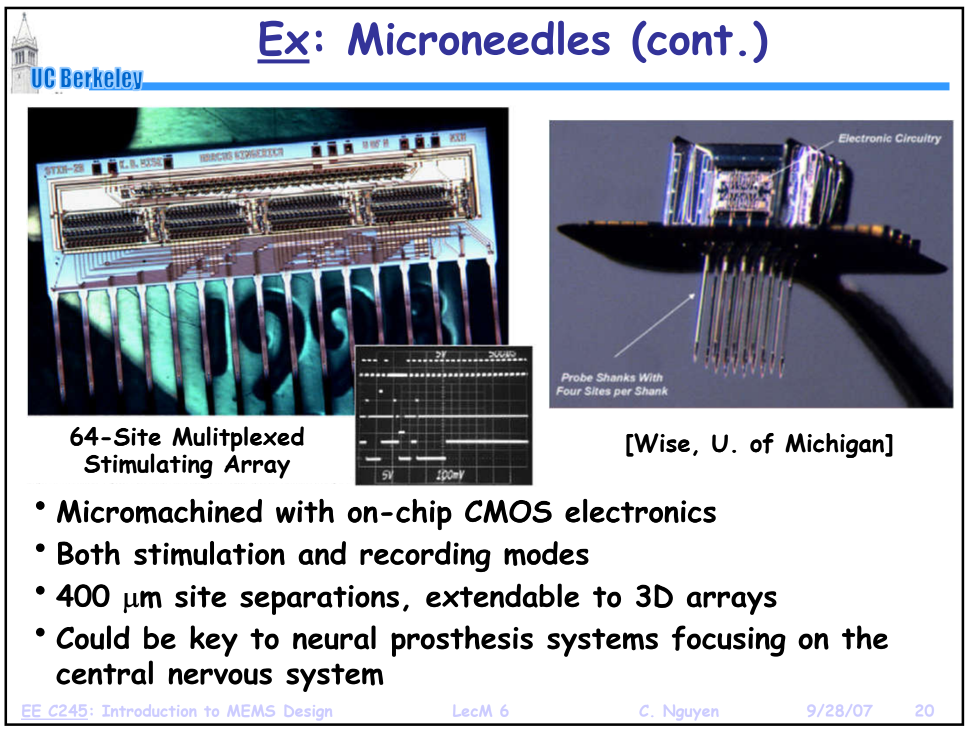

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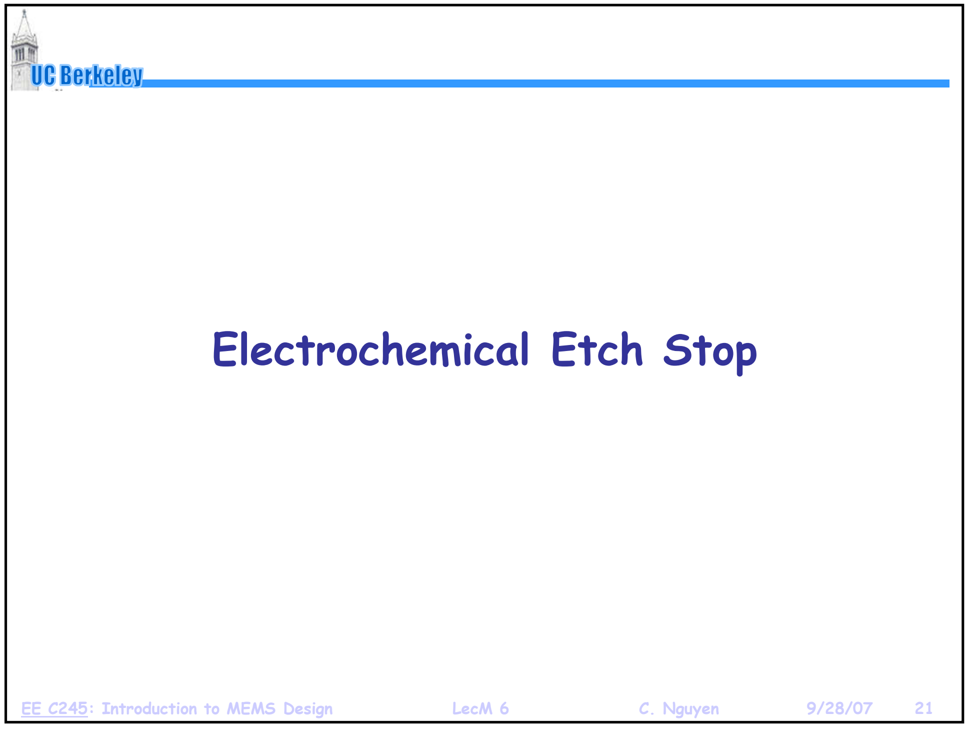

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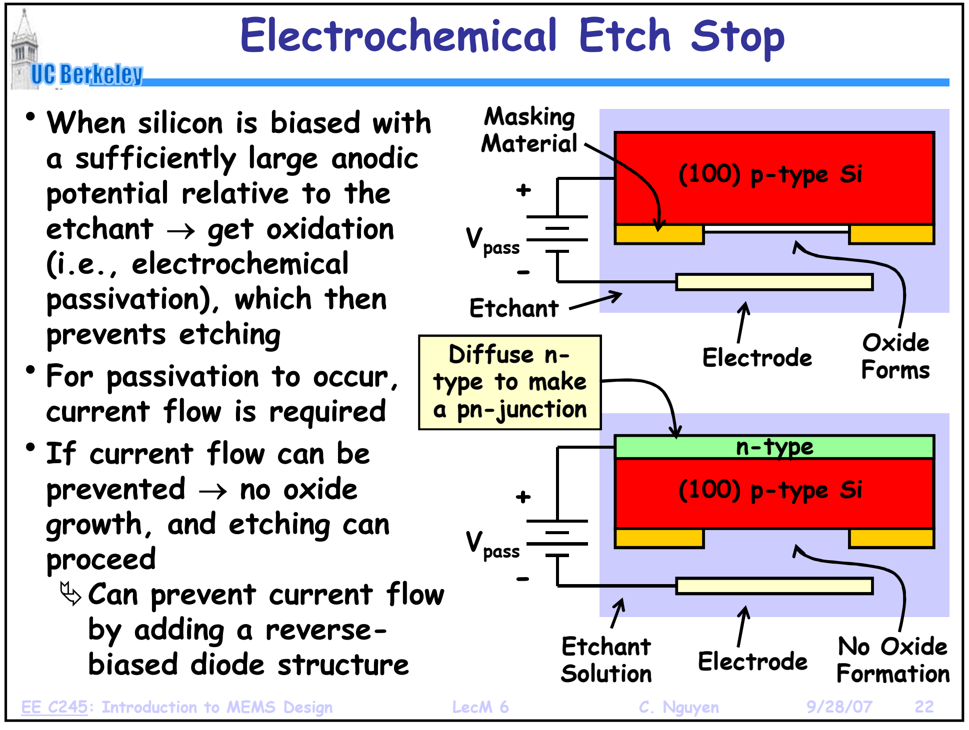

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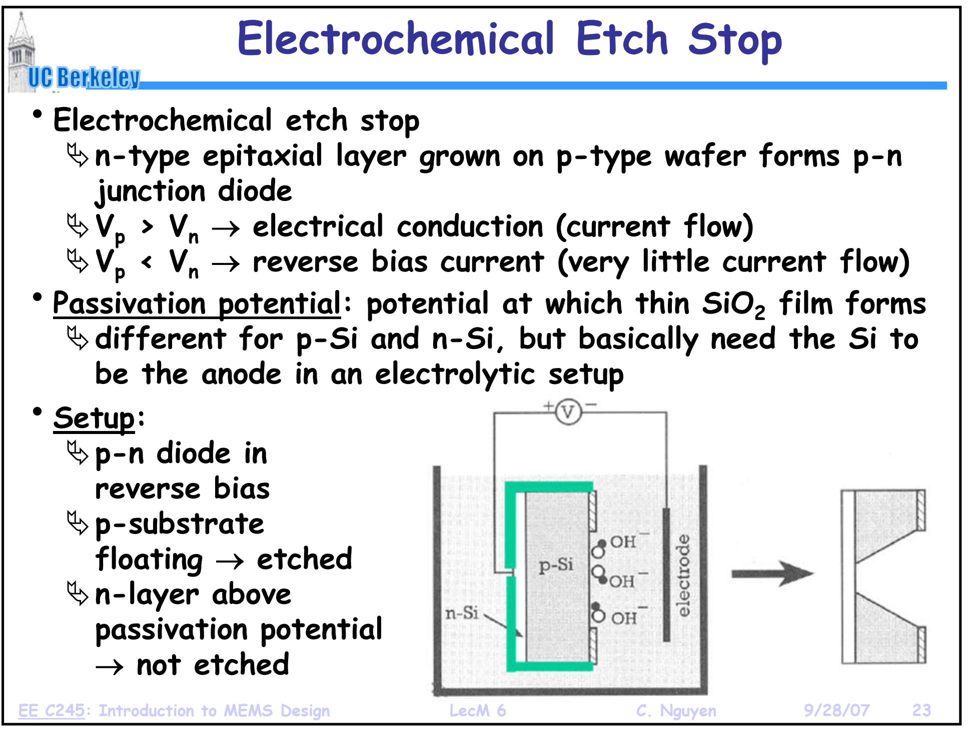

23

Electrochemical Etching of CMOS

- N-type Si well with circuits suspended f/ SiO_2 support beam
- Thermally and electrically isolated
- If use dual-doped TMAH etchant, Al bond pads safe

[Reay, et al. (1994)]
[Kovacs Group, Stanford]

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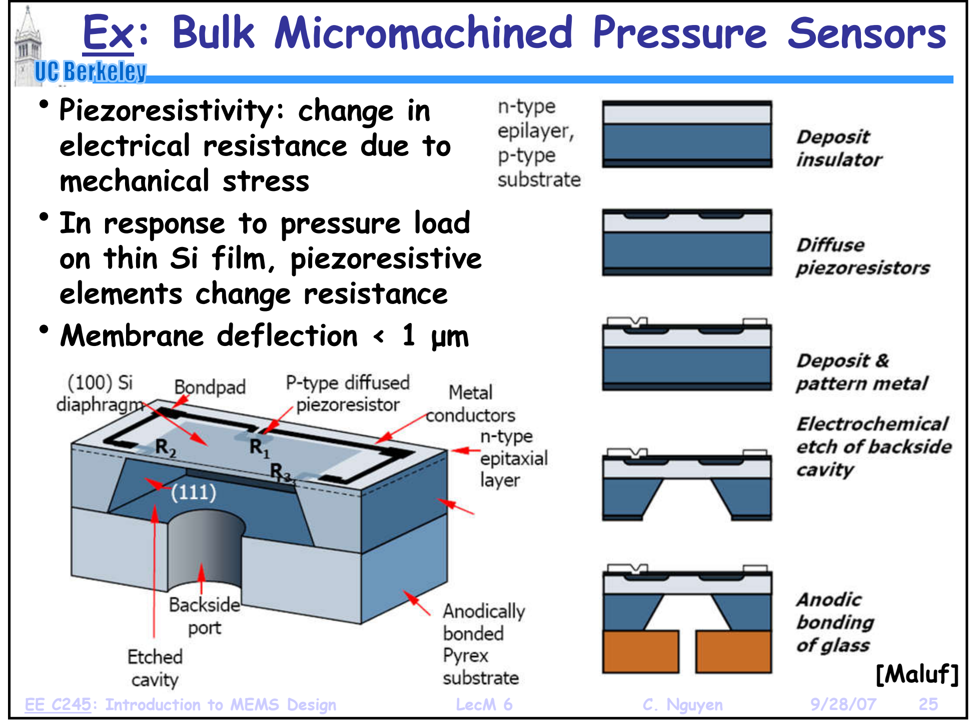

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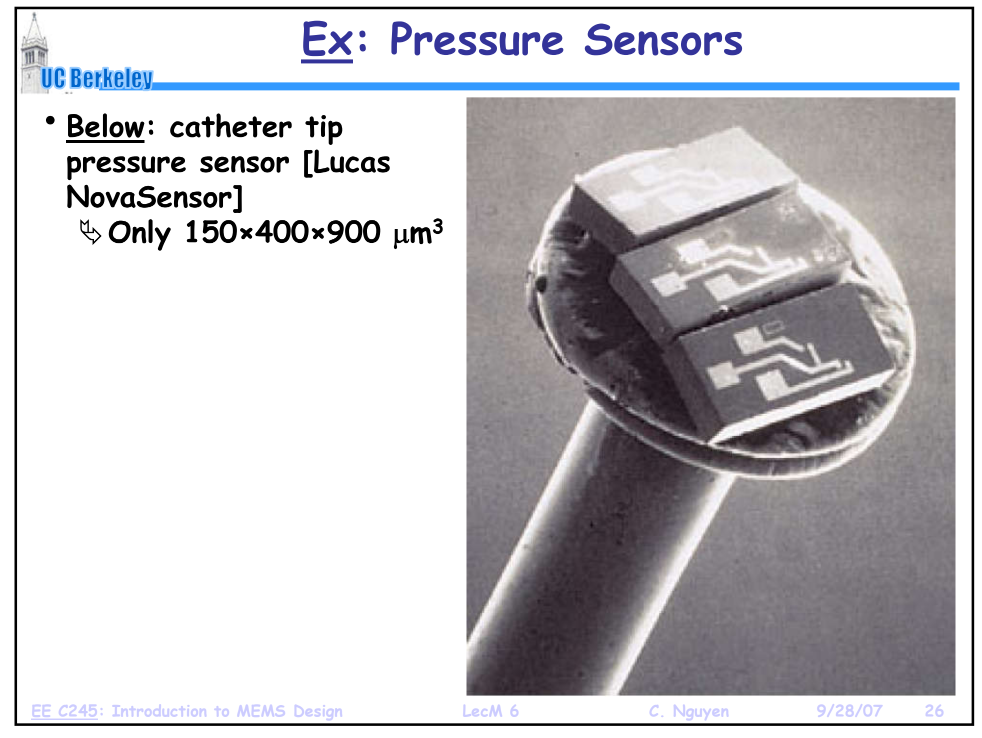

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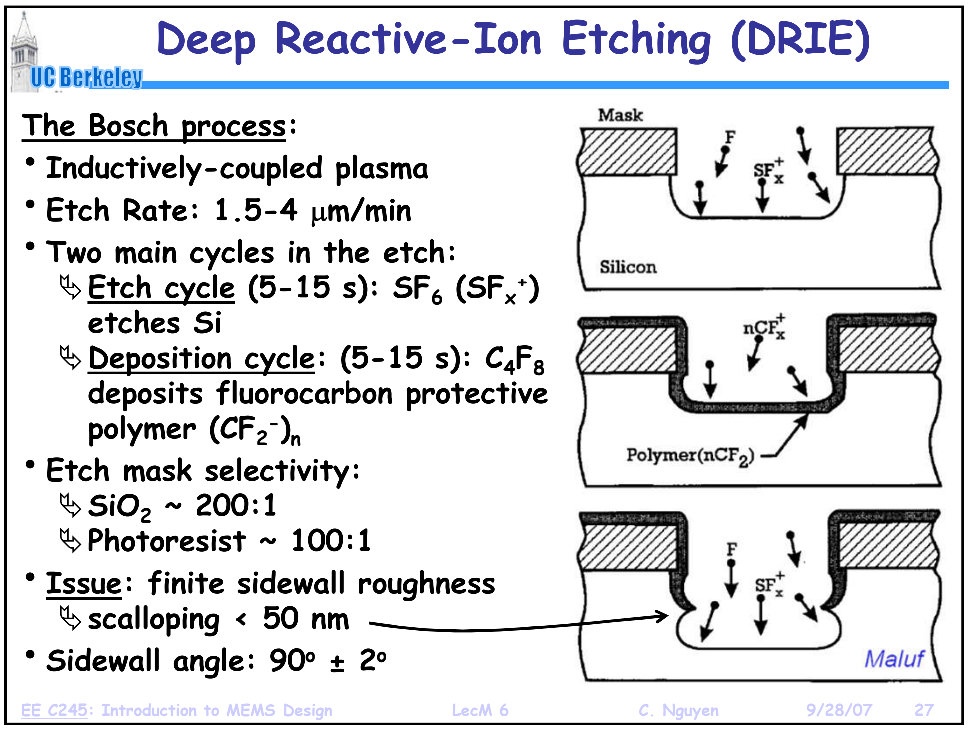

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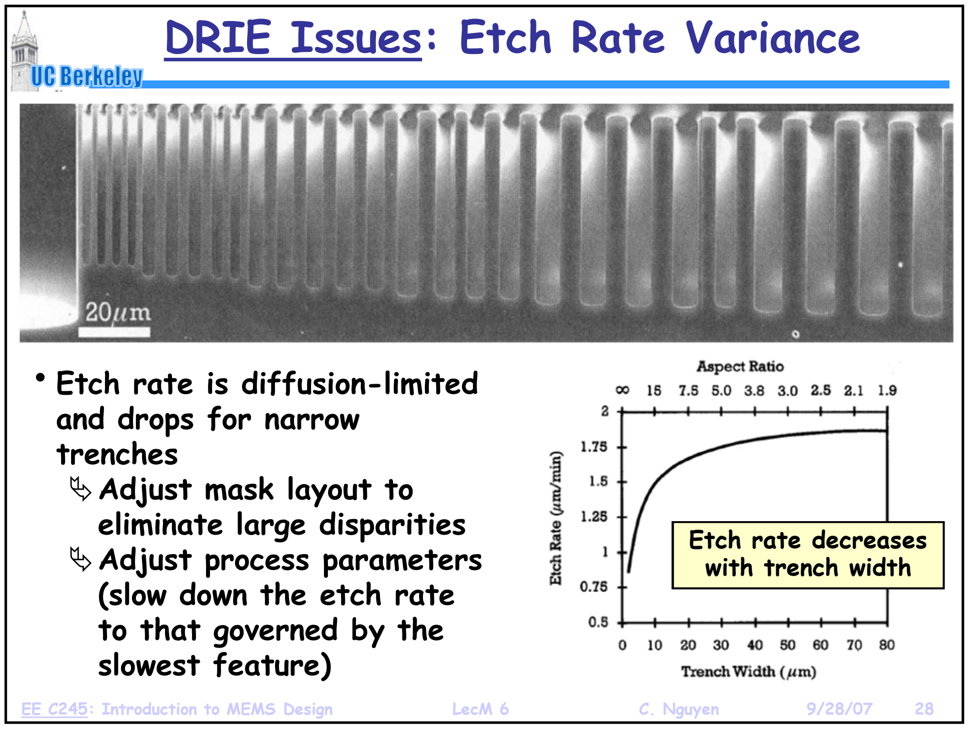

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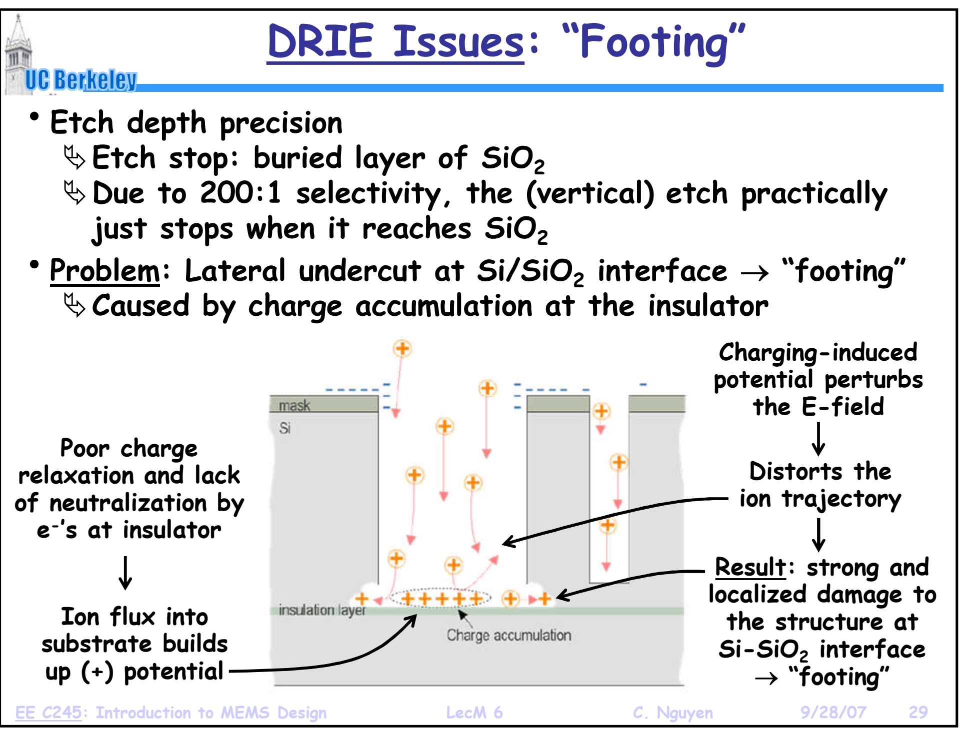

29

Recipe-Based Suppression of "Footing"

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- Use higher process pressure to reduce ion charging [Nozawa]
  - High operating pressure → concentration of (-) charge increases and can neutralize (+) surface charge
  - Issue: must introduce as a separate recipe when the etch reaches the Si-insulator interface, so must be able to very accurately predict the time needed for etching
- Adjust etch recipe to reduce overetching [Schmidt]
  - Change C_4F_8 flow rate, pressure, etc., to enhance passivation and reduce overetching
  - Issue: Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches
- Use lower frequency plasma to avoid surface charging [Morioka]
  - Low frequency → more ions with low directionality and kinetic energy → neutralizes (-) potential barrier at trench entrance
  - Allows e^-'s to reach the trench base and neutralize (+) charge → maintain charge balance inside the trench

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30

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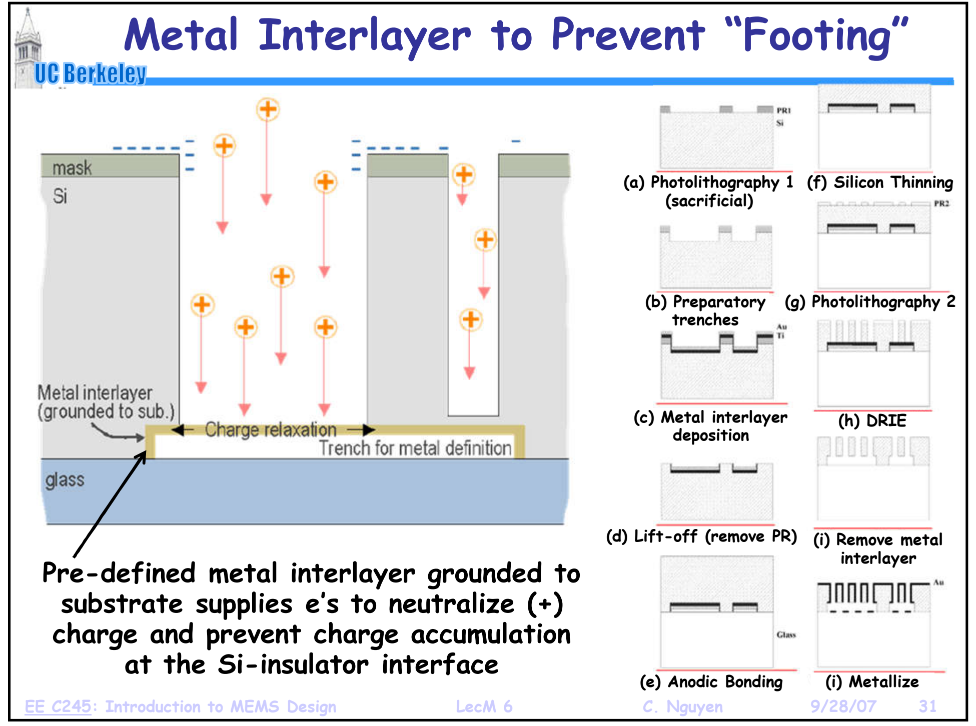

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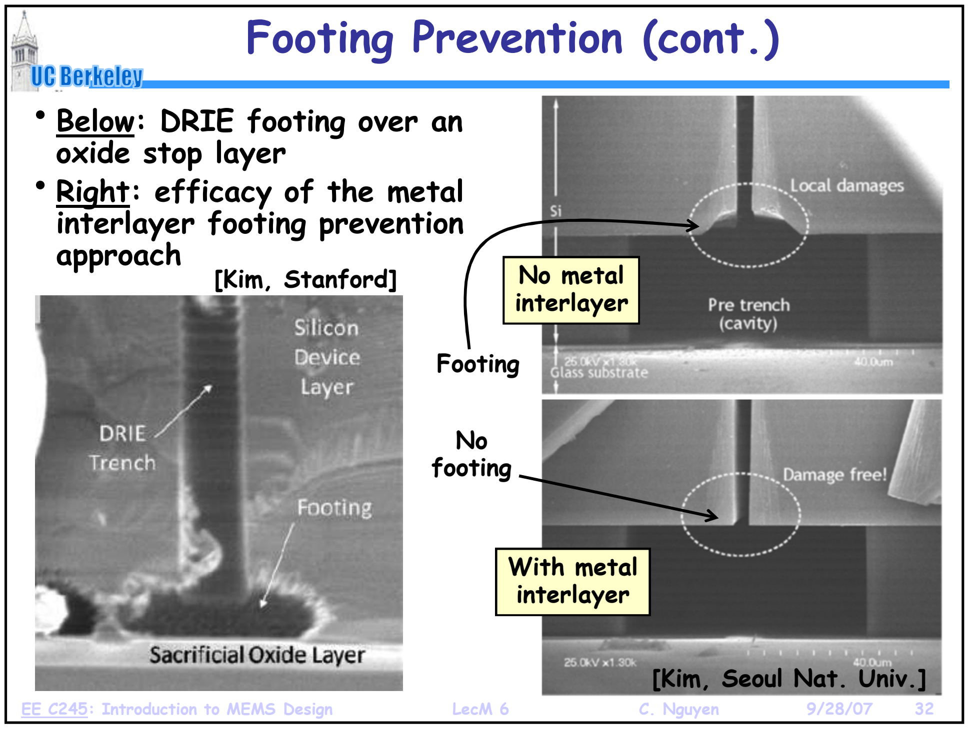

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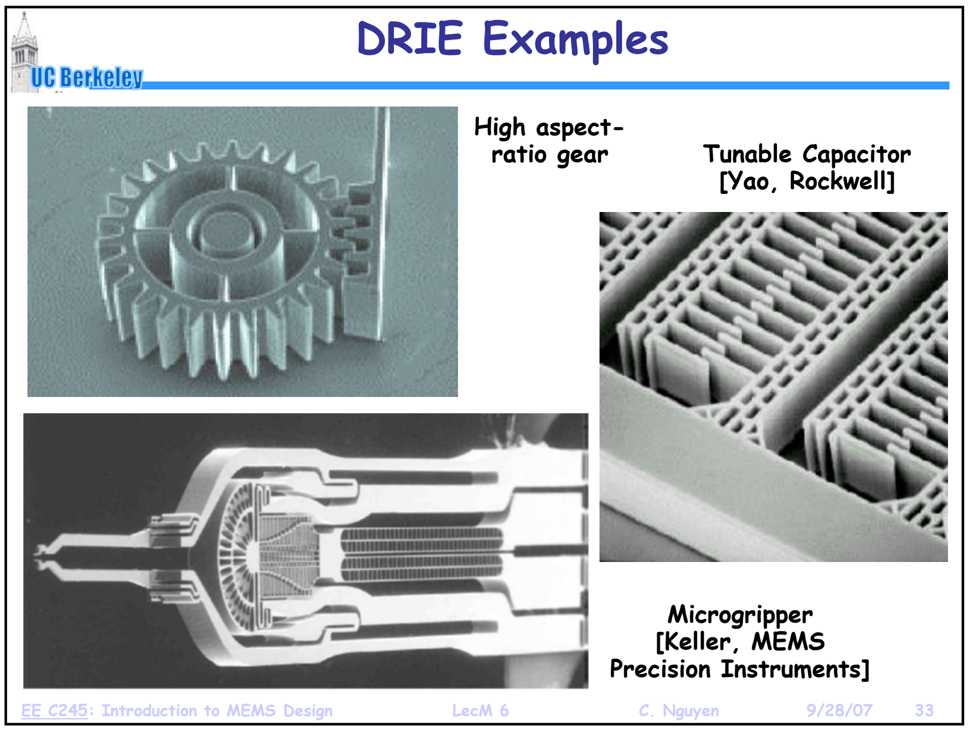

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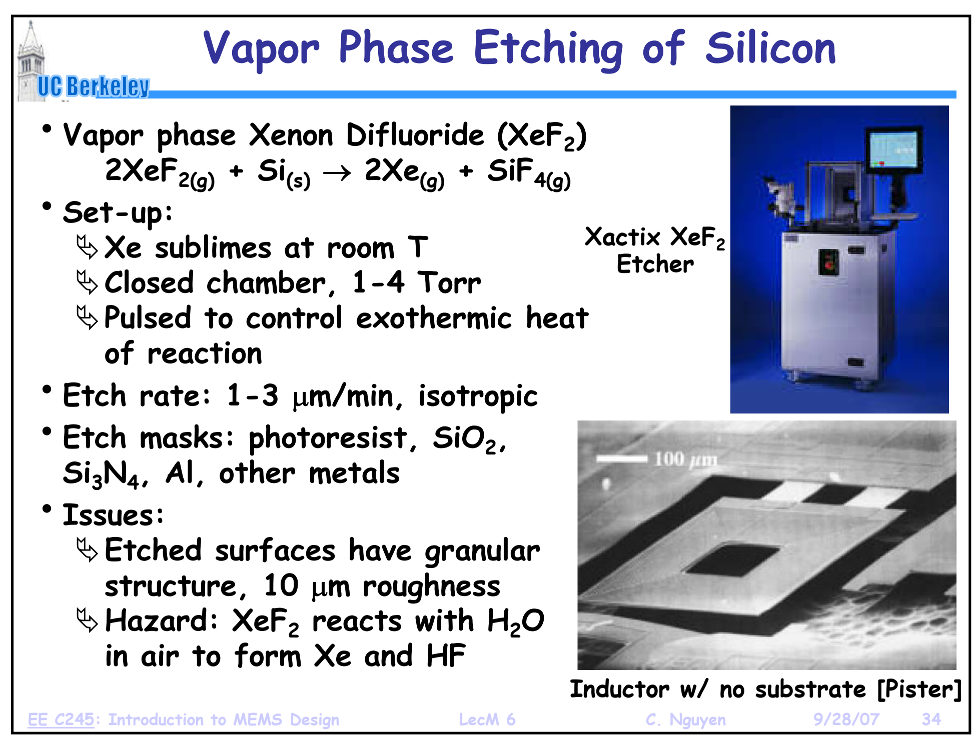

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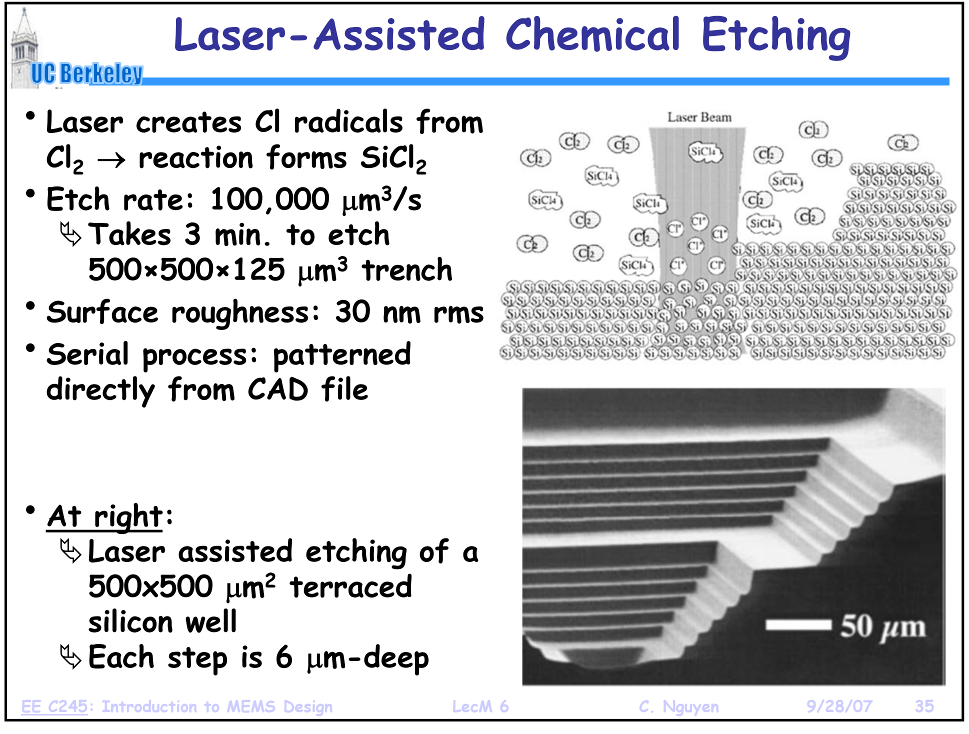

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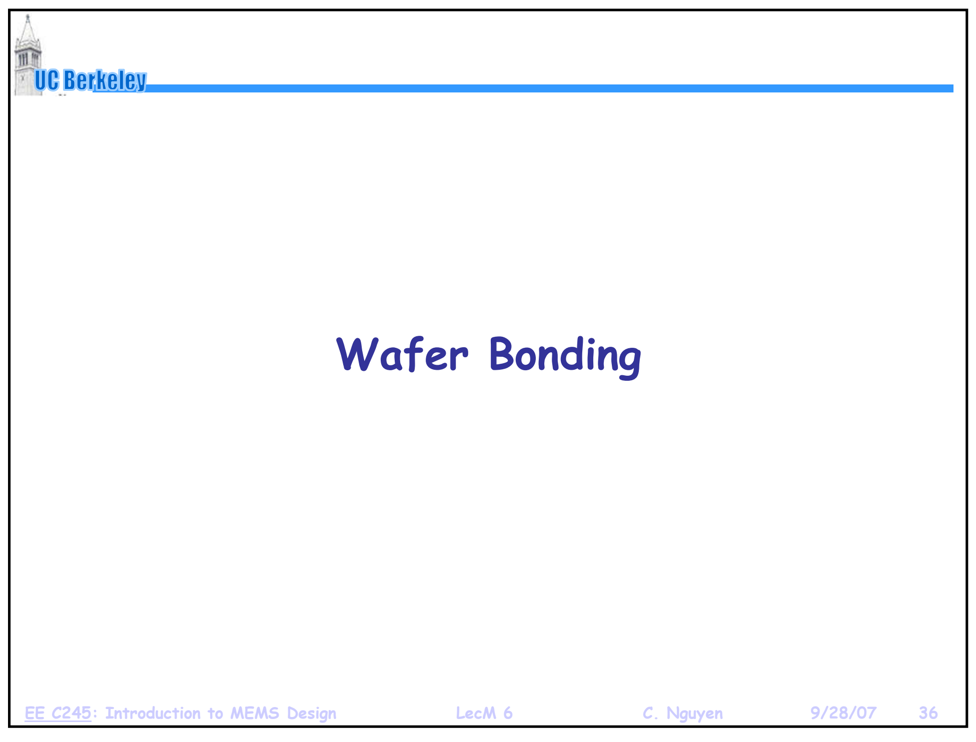

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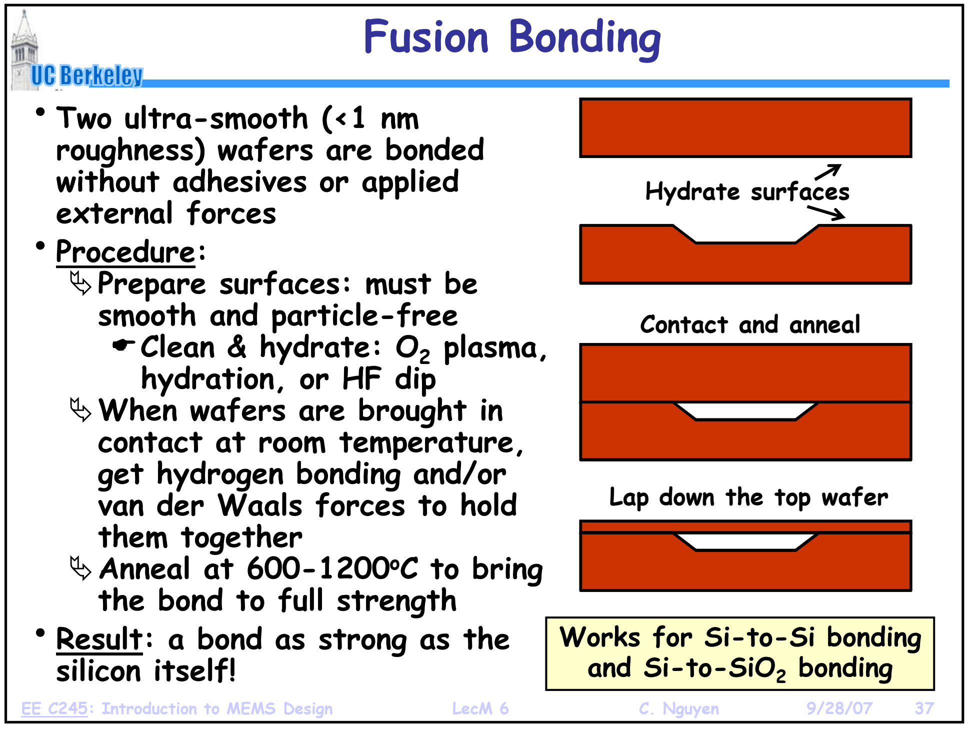

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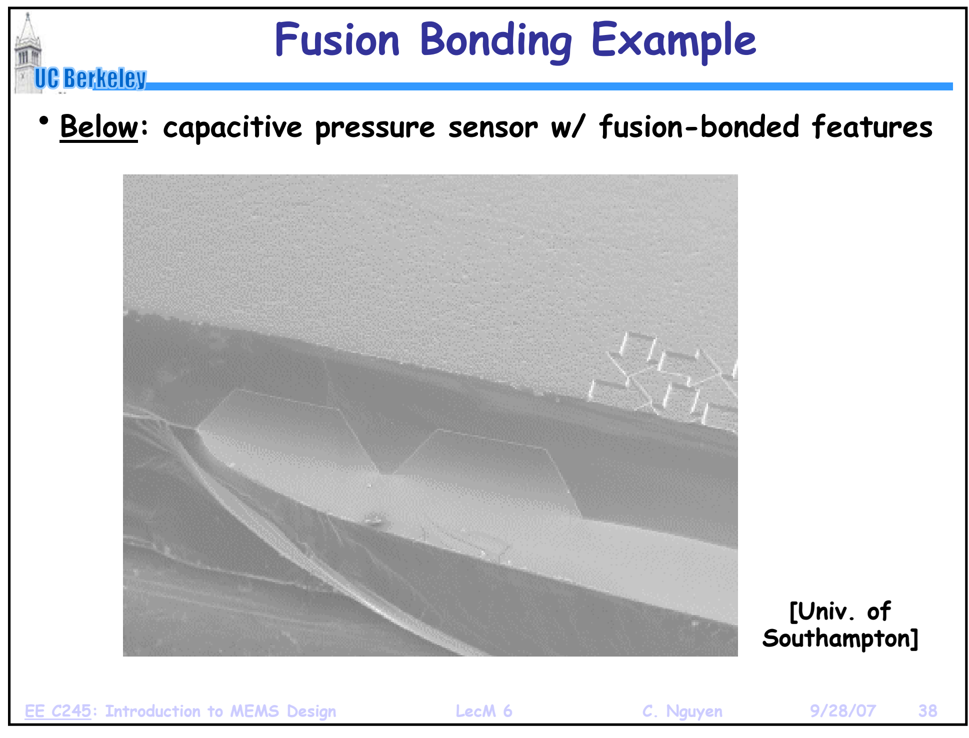

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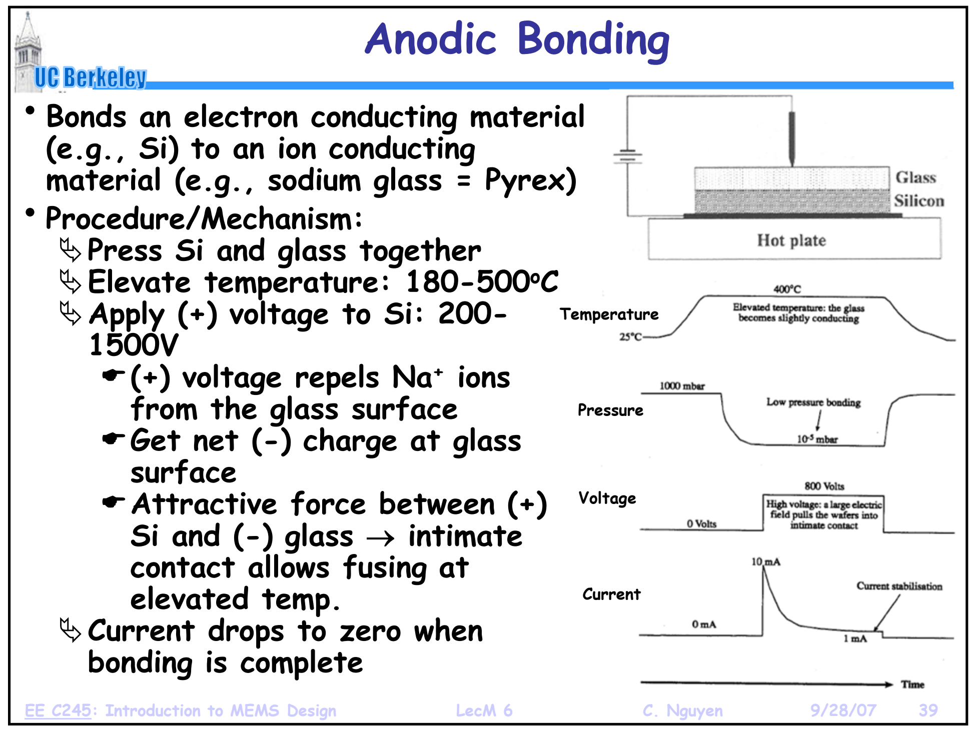

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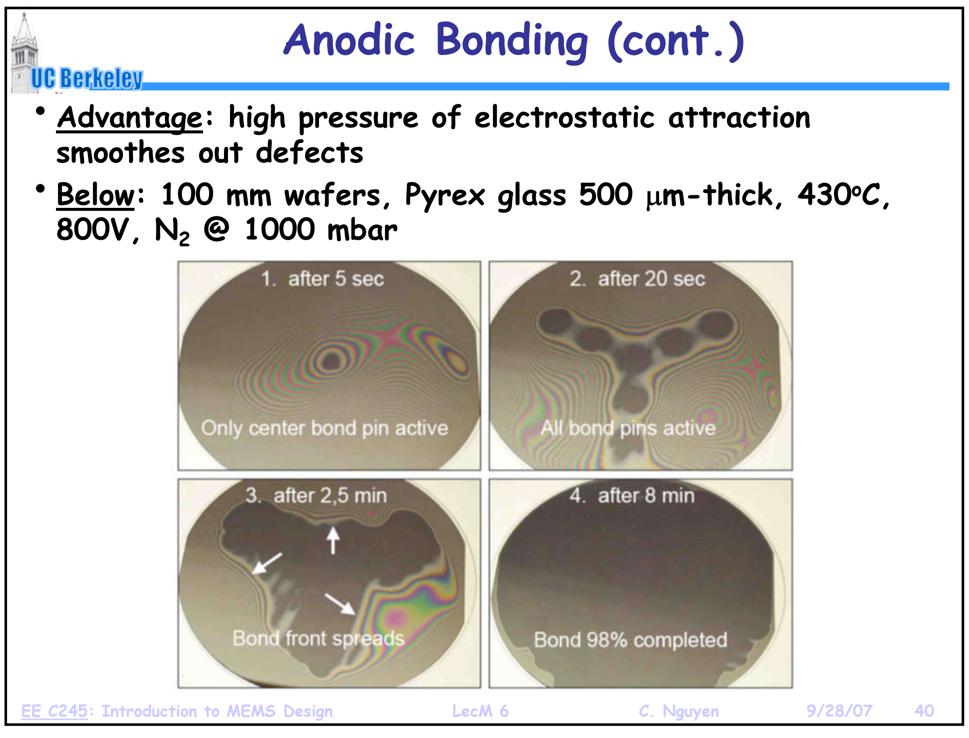

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Metal Layer Bonding

- Pattern seal rings and bond pads photolithographically
- Eutectic bonding
  - Uses eutectic point in metal-Si phase diagrams to form silicides
  - Au and Si have eutectic point at 363°C
  - Low temperature process
  - Can bond slightly rough surfaces
  - Issue: Au contamination of CMOS
- Solder bonding
  - PbSn (183°C), AuSn (280°C)
  - Lower-T process
  - Can bond very rough surfaces
  - Issue: outgassing (not good for encapsulation)
- Thermocompression
  - Commonly done with electroplated Au or other soft metals
  - Room temperature to 300°C
  - Lowest-T process
  - Can bond rough surfaces with topography

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41

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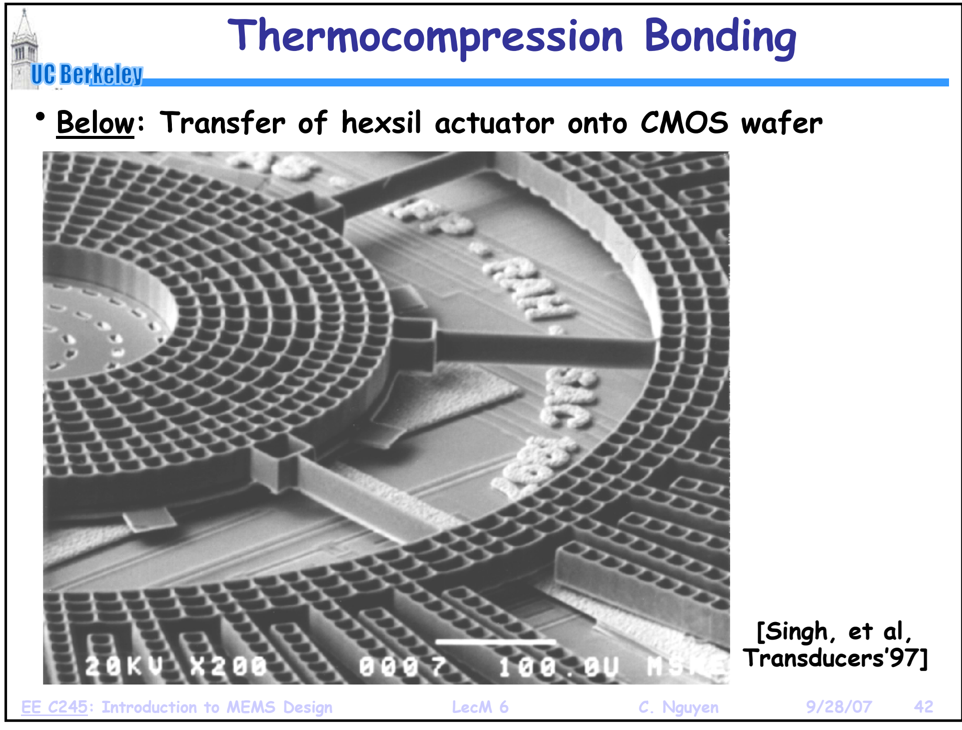
Thermocompression Bonding

- Below: Transfer of hexsil actuator onto CMOS wafer



[Singh, et al, Transducers'97]

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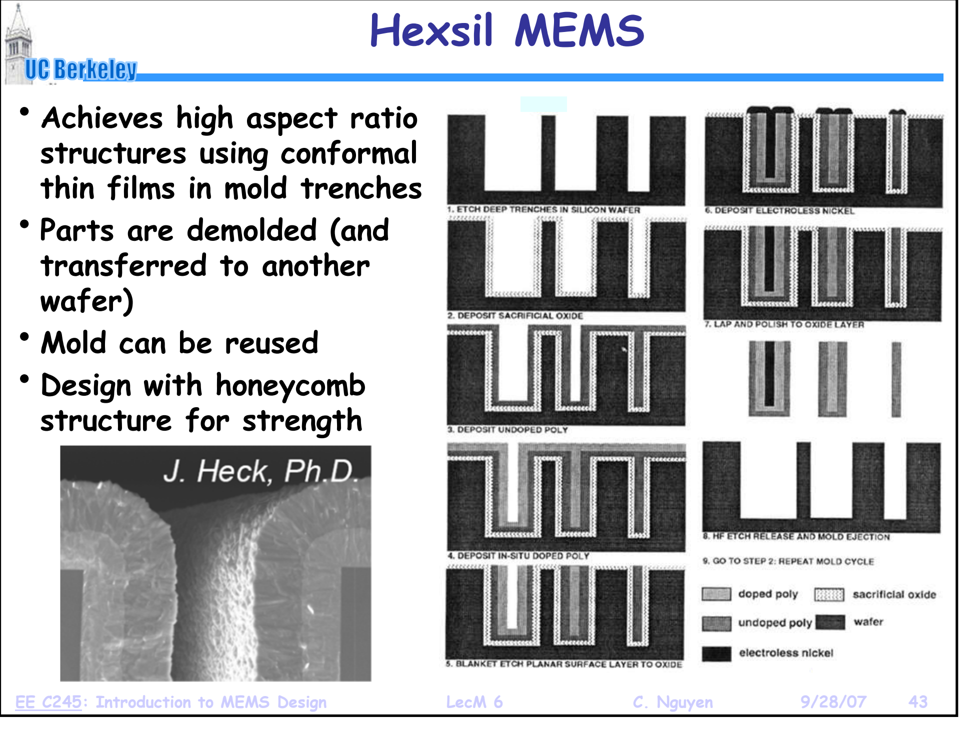

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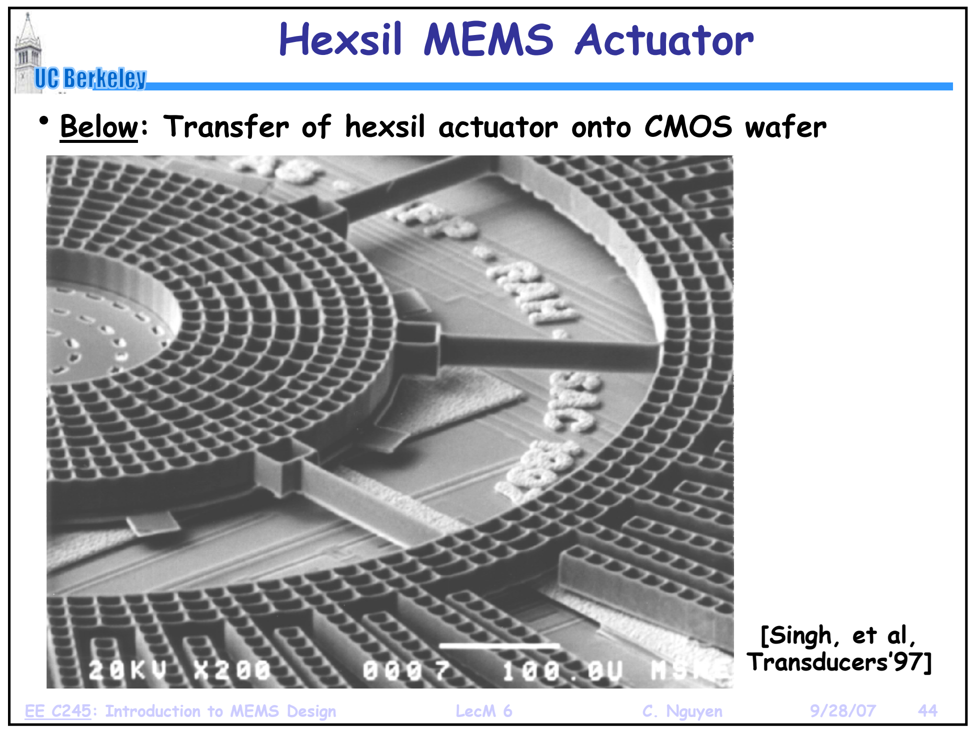

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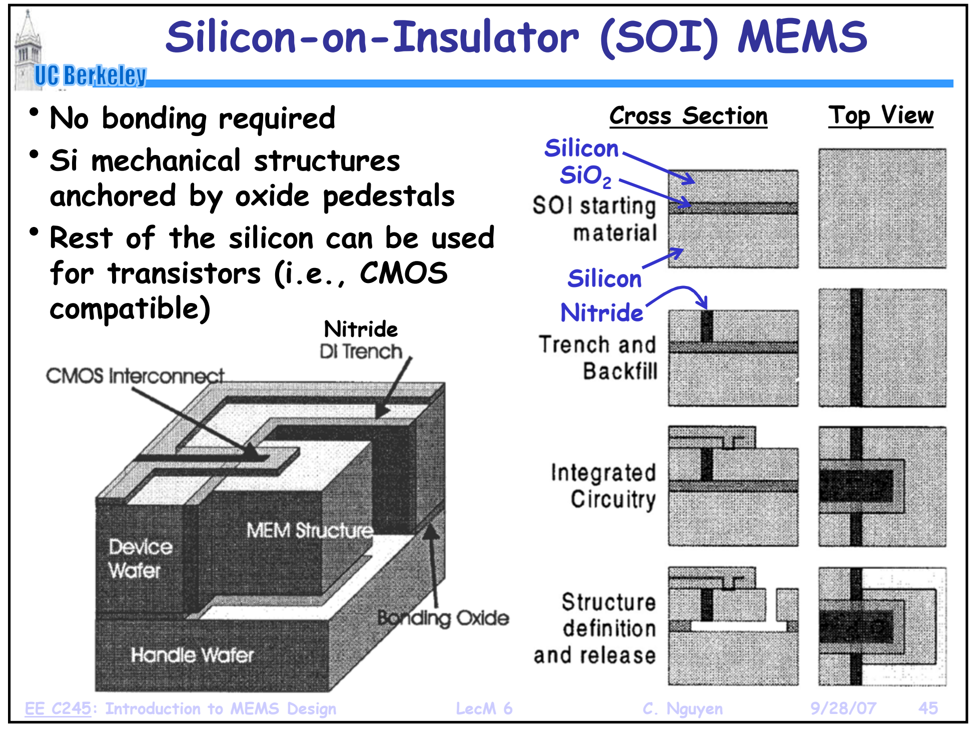

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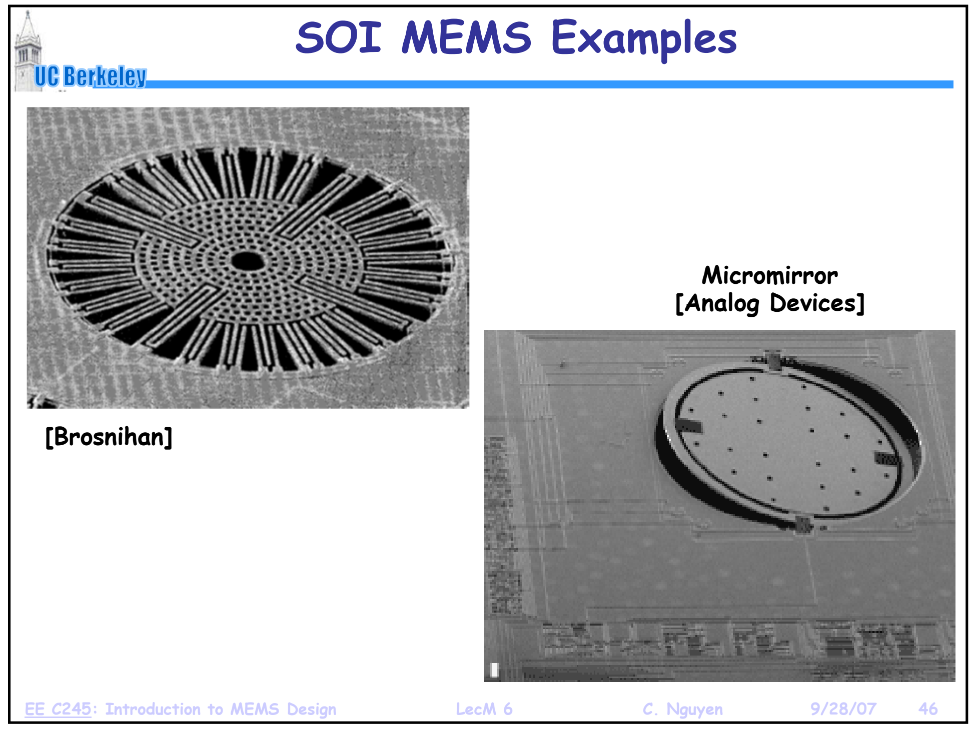

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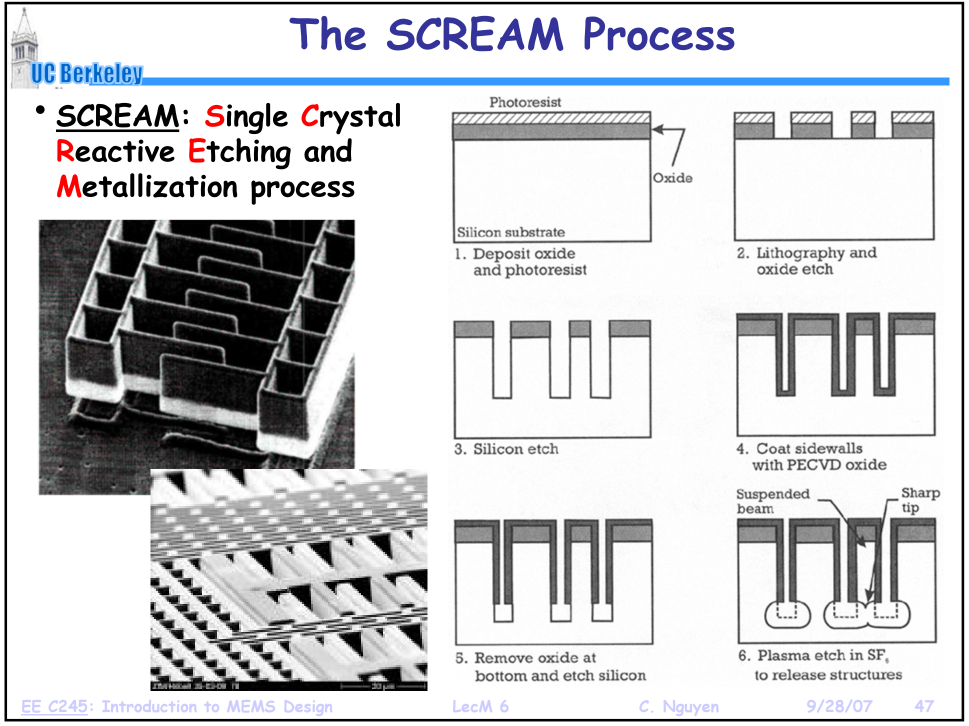

47