

---

**EE C247B - ME C218**  
**Introduction to MEMS Design**  
**Spring 2020**


**Prof. Clark T.-C. Nguyen**

Dept. of Electrical Engineering & Computer Sciences  
University of California at Berkeley  
Berkeley, CA 94720

**Lecture Module 6: Bulk Micromachining**

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    1

1




---

**Lecture Outline**

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handouts: "Bulk Micromachining of Silicon"
- Lecture Topics:
  - ↗ Bulk Micromachining
  - ↗ Anisotropic Etching of Silicon
  - ↗ Boron-Doped Etch Stop
  - ↗ Electrochemical Etch Stop
  - ↗ Isotropic Etching of Silicon
  - ↗ Deep Reactive Ion Etching (DRIE)
  - ↗ Wafer Bonding

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    2

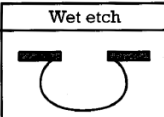
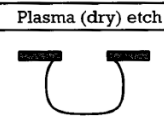
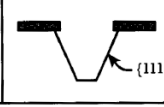
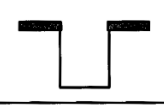
2

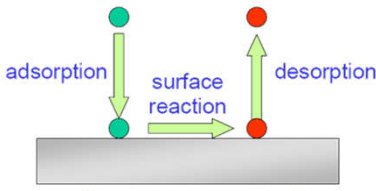


## Bulk Micromachining

---

- Basically, etching the substrate (usually silicon) to achieve microstructures
- Etching modes:
  - ↪ Isotropic vs. anisotropic
  - ↪ Reaction-limited
    - Etch rate dep. on temp.
  - ↪ Diffusion-limited
    - Etch rate dep. on mixing
    - Also dependent on layout & geometry, i.e., on loading
- Choose etch mode based on
  - ↪ Desired shape
  - ↪ Etch depth and uniformity
  - ↪ Surface roughness (e.g., sidewall roughness after etching)
  - ↪ Process compatibility (w/ existing layers)
  - ↪ Safety, cost, availability, environmental impact


	Wet etch	Plasma (dry) etch
Isotropic		
Anisotropic		



slowest step controls rate of reaction

EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
3

3



## Mechanical Properties of Silicon

---

- Crystalline silicon is a hard and brittle material that deforms elastically until it reaches its yield strength, at which point it breaks.
  - ↪ Tensile yield strength = 7 GPa (~1500 lb suspended from 1 mm<sup>2</sup>)
  - ↪ Young's Modulus near that of stainless steel
  - ↪ {100} = 130 GPa; {110} = 169 GPa; {111} = 188 GPa
  - ↪ Mechanical properties uniform, no intrinsic stress
  - ↪ Mechanical integrity up to 500°C
  - ↪ Good thermal conductor
  - ↪ Low thermal expansion coefficient
  - ↪ High piezoresistivity

EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
4

4

**Anisotropic Wet Etching**

UC Berkeley

**Anisotropic etches are available for single crystal Si:**

- ↪ Orientation-dependent etching:  $\langle 111 \rangle$ -plane more densely packed than  $\langle 100 \rangle$ -plane
  - ↖ Faster E.R.
  - ↗ Slower E.R.

...in some solvents

One such solvent: KOH + isopropyl alcohol  
 (e.g., 23.4 wt% KOH, 13.3 wt% isopropyl alcohol, 63 wt% H<sub>2</sub>O)

⇒ E.R. <sub>$\langle 100 \rangle$</sub>  = 100 × E.R. <sub>$\langle 111 \rangle$</sub>

5

**Anisotropic Etching of Silicon**

UC Berkeley

- Etching of Si w/ KOH
  - $\text{Si} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2^{2-} + 4e^-$
  - $4\text{H}_2\text{O} + 4e^- \rightarrow 4(\text{OH})^- + 2\text{H}_2$
- Crystal orientation dependent etch rates
  - ↪  $\{110\}:\{100\}:\{111\}=600:400:1$
  - ↪  $\{100\}$  and  $\{110\}$  have 2 bonds below the surface & 2 dangling bonds that can react
  - ↪  $\{111\}$  plane has three of its bonds below the surface & only one dangling bond to react → much slower E.R.
  - ↪  $\{111\}$  forms protective oxide
  - ↪  $\{111\}$  smoother than other crystal planes → good for optical MEMS (mirrors)

Self-limiting etches

Front side mask

Back side mask

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    6

6

**Anisotropic Wet Etching (cont.)**

UC Berkeley

Can get the following:

(on a  $\langle 100 \rangle$  - wafer)

(on a  $\langle 110 \rangle$  - wafer)

⇒ Quite anisotropic!

7

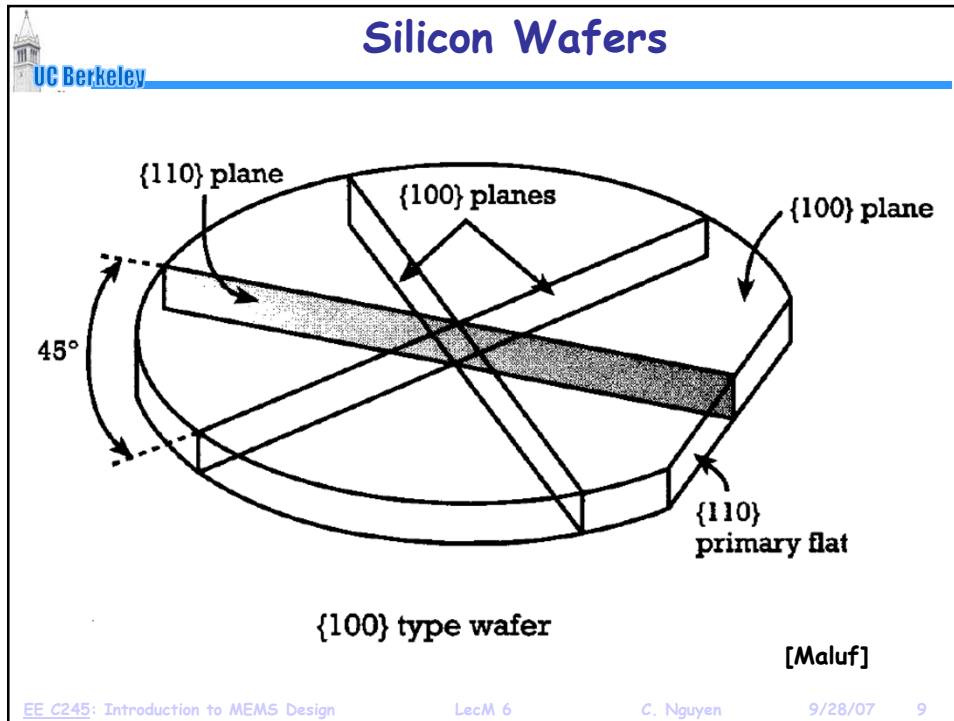
**Anisotropic Etching of Silicon**

UC Berkeley

- Deposit nitride:
  - ⊗ Target = 100nm
  - ⊗ 22 min. LPCVD @800°C
- Lithography to define areas of silicon to be etched
- Etch/pattern nitride mask
  - ⊗ RIE using  $\text{SF}_6$
  - ⊗ Remove PR in PRS2000
- Etch the silicon
  - ⊗ Use 1:2  $\text{KOH}:\text{H}_2\text{O}$  (wt.), stirred bath @ 80°C
  - ⊗ Etch Rates:
    - (100) Si → 1.4  $\mu\text{m}/\text{min}$
    - $\text{Si}_3\text{N}_4$  → ~ 0 nm/min
    - $\text{SiO}_2$  → 1-10 nm/min
    - Photoresist, Al → fast
- Micromasking by  $\text{H}_2$  bubbles leads to roughness
  - ⊗ Stir well to displace bubbles
  - ⊗ Can also use oxidizer for (111) surfaces
  - ⊗ Or surfactant additives to suppress bubble formation

EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      8

8



9

### Silicon Crystallography

**Miller Indices (h k l):**

- Planes
  - ↗ Reciprocal of plane intercepts with axes
  - ↗ e.g., for (110), intercepts: (x,y,z) = (1,1,∞); reciprocals: (1,1,0) → (110)
  - ↗ (unique), {family}
- Directions
  - ↗ One endpoint of vector @ origin
  - ↗ [unique], <family>

EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
10

10

**Determining Angles Between Planes**

UC Berkeley

- The angle between vectors  $[abc]$  and  $[xyz]$  is given by:
 
$$ax + by + cz = |(a, b, c)| \cdot |(x, y, z)| \cdot \cos \theta$$

$$\theta_{(a,b,c),(x,y,z)} = \cos^{-1} \left[ \frac{ax + by + cz}{|(a, b, c)| \cdot |(x, y, z)|} \right]$$
- For  $\{100\}$  and  $\{110\} \rightarrow 45^\circ$
- For  $\{100\}$  and  $\{111\} \rightarrow 54.74^\circ$
- For  $\{110\}$  and  $\{111\} \rightarrow 35.26^\circ, 90^\circ, \text{ and } 144.74^\circ$

EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      11

11

**Silicon Crystal Origami**

UC Berkeley

- Silicon fold-up cube
- Adapted from Profs. Kris Pister and Jack Judy
- Print onto transparency
- Assemble inside out
- Visualize crystal plane orientations, intersections, and directions

[Judy, UCLA]

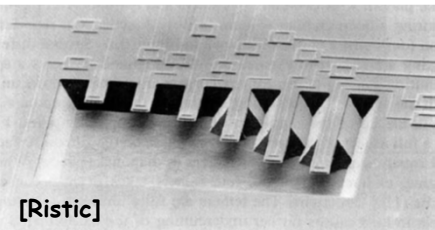
EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      12

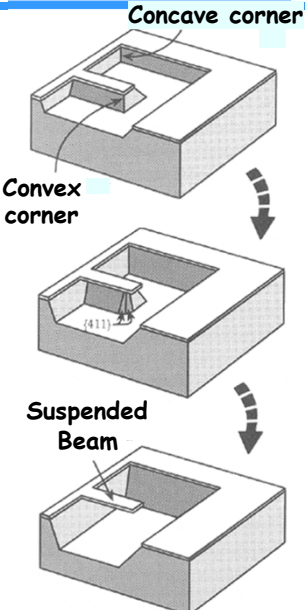
12

### Undercutting Via Anisotropic Si Etching

UC Berkeley

- Concave corners bounded by {111} are not attacked
- ... but convex corners bounded by {111} are attacked
  - ↳ Two {111} planes intersecting now present two dangling bonds → no longer have just one dangling bond → etch rate fast
  - ↳ **Result:** can undercut regions around convex corners





Concave corner

Convex corner

Suspended Beam

[Ristic]

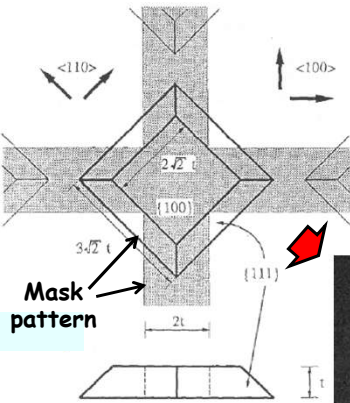
EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
13

13

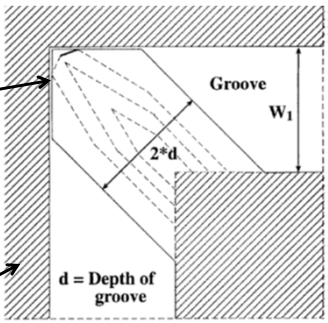
### Corner Compensation

UC Berkeley

- Protect corners with "compensation" areas in layout
- **Below:** Mesa array for self-assembly structures [Smith 1995]



Mask pattern



Gap

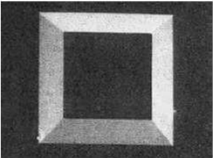
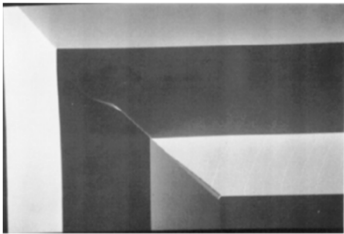
Groove  $W_1$

$2^{\circ}d$

$d = \text{Depth of groove}$


Mask pattern

Shaded regions are the desired result

EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
14

14

 **Other Anisotropic Silicon Etchants**

- TMAH, Tetramethyl ammonium hydroxide, 10-40 wt.% (90°C)
  - ↖ Etch rate (100) = 0.5-1.5  $\mu\text{m}/\text{min}$
  - ↖ Al safe when dual-doped w/ silicic acid &  $(\text{NH}_4)_2\text{S}_2\text{O}_8$
  - ↖ IC compatible
  - ↖ Etch ratio (100)/(111) = 10-35
  - ↖ Etch masks:  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$  ~ 0.05-0.25 nm/min
  - ↖ Boron doped etch stop, up to 40 $\times$  slower
- EDP (115°C)
  - ↖ Carcinogenic, corrosive
  - ↖ Etch rate (100) = 0.75  $\mu\text{m}/\text{min}$
  - ↖ Al may be etched
  - ↖  $R(100) > R(110) > R(111)$
  - ↖ Etch ratio (100)/(111) = 35
  - ↖ Etch masks:  $\text{SiO}_2$  ~ 0.2 nm/min,  $\text{Si}_3\text{N}_4$  ~ 0.1 nm/min
  - ↖ Boron doped etch stop, 50 $\times$  slower

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    15


15

 **Boron-Doped Etch Stop**

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    16

16

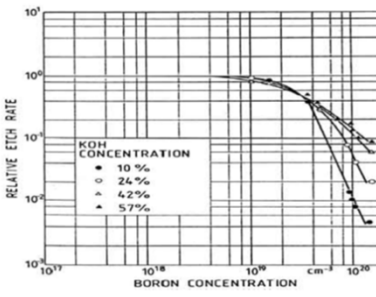
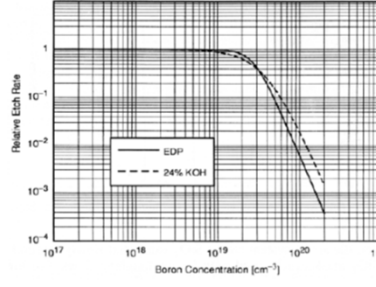




## Boron-Doped Etch Stop


- Control etch depth precisely with boron doping (p++)
  - ↳ [B] > 10<sup>20</sup> cm<sup>-3</sup> reduces KOH etch rate by 20-100x
  - ↳ Can use gaseous or solid boron diffusion
  - ↳ Recall etch chemistry:
 
$$\text{Si} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2^{2+} + 4\text{e}^-$$

$$4\text{H}_2\text{O} + 4\text{e}^- \rightarrow 4(\text{OH})^- + 2\text{H}_2$$
  - ↳ At high dopant levels, injected electrons recombine with holes in valence band and are unavailable for reactions to give OH<sup>-</sup>
- **Result:**
  - ↳ Beams, suspended films
  - ↳ 1-20 μm layers possible

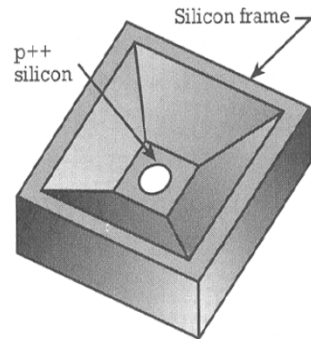
EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
17

17



## Ex: Micronozzle

- Micronozzle using anisotropic etch-based fabrication
- Used for inkjet printer heads



1. Pattern mask

2. Etch circle in p++

3. Mask front side

4. Anisotropic etch

**[Maluf]**

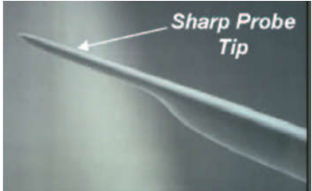
EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
18

18

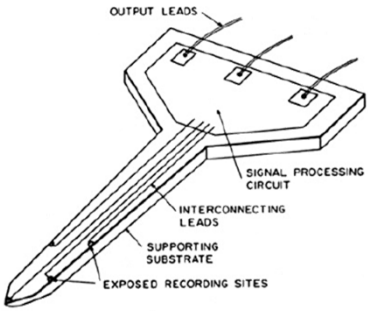
**Ex: Microneedle**

UC Berkeley

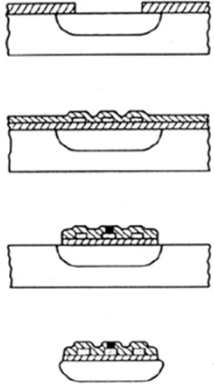
- Below: micro-neurostimulator
  - Used to access central nervous system tissue (e.g., brain) and record electrical signals on a cellular scale
- Wise Group, Univ. of Michigan



Sharp Probe Tip



Multi-Channel Recording Array Structure



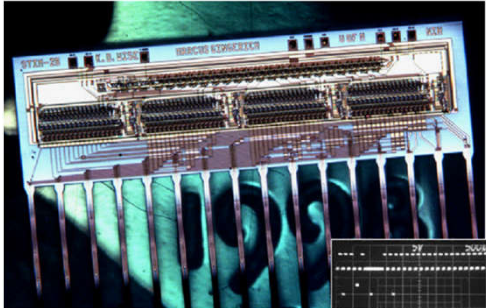
- Selectively diffuse p++ into substrate
- Deposit interconnect pattern and insulate conductors
- Pattern dielectric and metallize recording sites
- Dissolve away the wafer (no mask needed)

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    19

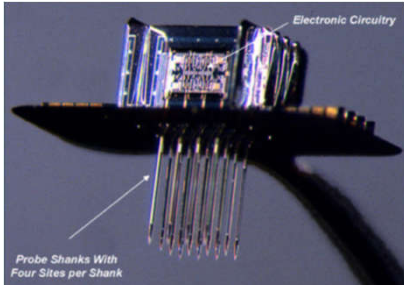
19

**Ex: Microneedles (cont.)**

UC Berkeley



64-Site Multiplexed Stimulating Array



Electronic Circuitry

Probe Shanks With Four Sites per Shank

[Wise, U. of Michigan]

- Micromachined with on-chip CMOS electronics
- Both stimulation and recording modes
- 400  $\mu\text{m}$  site separations, extendable to 3D arrays
- Could be key to neural prosthesis systems focusing on the central nervous system

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    20

20

UC Berkeley

## Electrochemical Etch Stop

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    21

21

UC Berkeley

## Electrochemical Etch Stop

- When silicon is biased with a sufficiently large anodic potential relative to the etchant → get oxidation (i.e., electrochemical passivation), which then prevents etching
- For passivation to occur, current flow is required
- If current flow can be prevented → no oxide growth, and etching can proceed
  - ↳ Can prevent current flow by adding a reverse-biased diode structure

Masking Material

(100) p-type Si

+

$V_{pass}$

-

Etchant

Electrode

Oxide Forms

Diffuse n-type to make a pn-junction

n-type

(100) p-type Si

+

$V_{pass}$

-


Etchant Solution

Electrode

No Oxide Formation

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    22

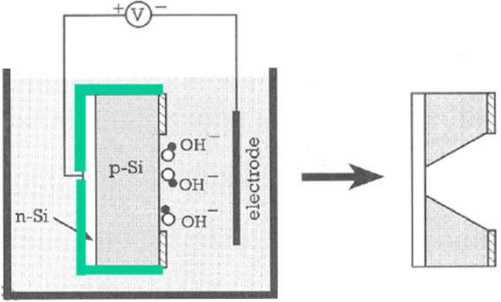
22



## Electrochemical Etch Stop


---

- **Electrochemical etch stop**
  - ↪ n-type epitaxial layer grown on p-type wafer forms p-n junction diode
  - ↪  $V_p > V_n \rightarrow$  electrical conduction (current flow)
  - ↪  $V_p < V_n \rightarrow$  reverse bias current (very little current flow)
- **Passivation potential:** potential at which thin  $\text{SiO}_2$  film forms
  - ↪ different for p-Si and n-Si, but basically need the Si to be the anode in an electrolytic setup
- **Setup:**
  - ↪ p-n diode in reverse bias
  - ↪ p-substrate floating  $\rightarrow$  etched
  - ↪ n-layer above passivation potential  $\rightarrow$  not etched



EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
23

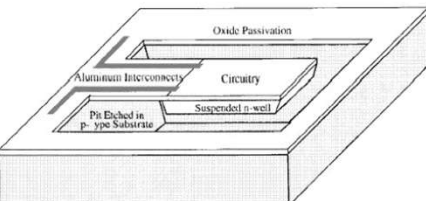
23

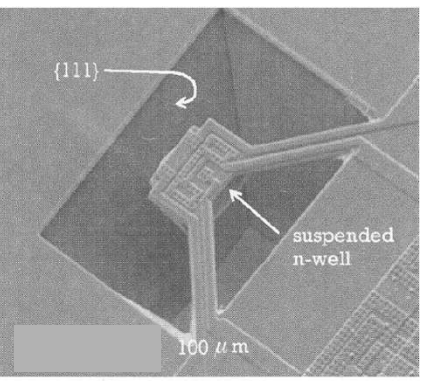


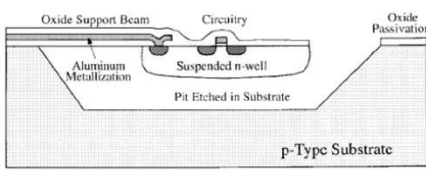
## Electrochemical Etching of CMOS

---

- N-type Si well with circuits suspended f/  $\text{SiO}_2$  support beam
- Thermally and electrically isolated
- If use dual-doped TMAH etchant, Al bond pads safe







[Reay, et al. (1994)]  
 [Kovacs Group, Stanford]

EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
24

24

**Ex: Bulk Micromachined Pressure Sensors**  
 UC Berkeley

- Piezoresistivity: change in electrical resistance due to mechanical stress
- In response to pressure load on thin Si film, piezoresistive elements change resistance
- Membrane deflection  $< 1 \mu\text{m}$

EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      25

25

**Ex: Pressure Sensors**  
 UC Berkeley

- Below: catheter tip pressure sensor [Lucas NovaSensor]  
 ↳ Only  $150 \times 400 \times 900 \mu\text{m}^3$

EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      26

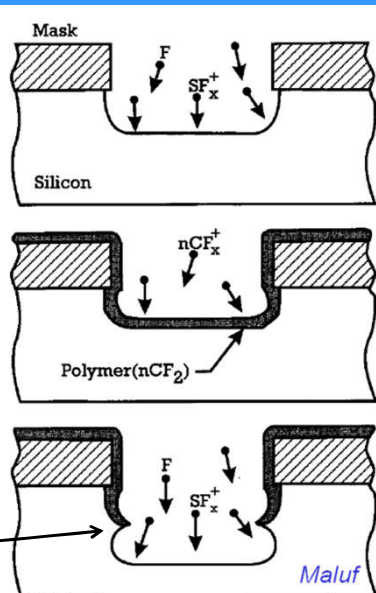
26

### Deep Reactive-Ion Etching (DRIE)

UC Berkeley

**The Bosch process:**

- Inductively-coupled plasma
- Etch Rate: 1.5-4  $\mu\text{m}/\text{min}$
- Two main cycles in the etch:
  - ↳ **Etch cycle** (5-15 s):  $\text{SF}_6$  ( $\text{SF}_x^+$ ) etches Si
  - ↳ **Deposition cycle**: (5-15 s):  $\text{C}_4\text{F}_8$  deposits fluorocarbon protective polymer  $(\text{CF}_2^-)_n$
- Etch mask selectivity:
  - ↳  $\text{SiO}_2 \sim 200:1$
  - ↳ Photoresist  $\sim 100:1$
- **Issue:** finite sidewall roughness
  - ↳ scalloping  $< 50 \text{ nm}$
- Sidewall angle:  $90^\circ \pm 2^\circ$



Mask

Silicon

Polymer( $n\text{CF}_2$ )<sub>n</sub>

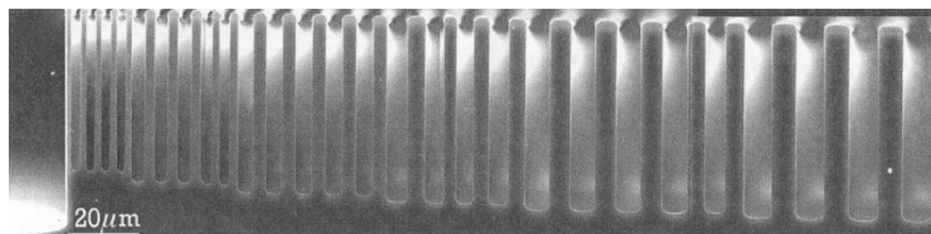
Maluf

EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
27

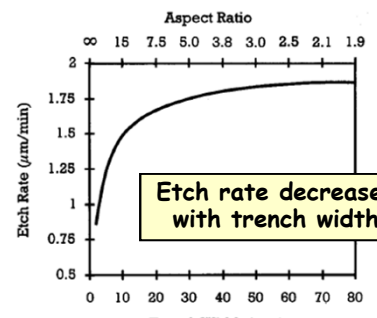
27

### DRIE Issues: Etch Rate Variance

UC Berkeley



- Etch rate is diffusion-limited and drops for narrow trenches
  - ↳ Adjust mask layout to eliminate large disparities
  - ↳ Adjust process parameters (slow down the etch rate to that governed by the slowest feature)



Aspect Ratio

∞ 15 7.5 5.0 3.8 3.0 2.5 2.1 1.9

Etch Rate ( $\mu\text{m}/\text{min}$ )

Trench Width ( $\mu\text{m}$ )

EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
28

28

**DRIE Issues: "Footing"**

UC Berkeley

- Etch depth precision
  - ↳ Etch stop: buried layer of  $\text{SiO}_2$
  - ↳ Due to 200:1 selectivity, the (vertical) etch practically just stops when it reaches  $\text{SiO}_2$
- **Problem:** Lateral undercut at  $\text{Si}/\text{SiO}_2$  interface → "footing"
  - ↳ Caused by charge accumulation at the insulator

Poor charge relaxation and lack of neutralization by  $e^-$ 's at insulator

Ion flux into substrate builds up (+) potential

Charging-induced potential perturbs the E-field

Distorts the ion trajectory

Result: strong and localized damage to the structure at  $\text{Si}-\text{SiO}_2$  interface → "footing"

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    29

29

**Recipe-Based Suppression of "Footing"**

UC Berkeley

- Use **higher process pressure** to reduce ion charging [Nozawa]
  - ↳ High operating pressure → concentration of (-) charge increases and can neutralize (+) surface charge
  - ↳ **Issue:** must introduce as a separate recipe when the etch reaches the  $\text{Si}$ -insulator interface, so must be able to very accurately predict the time needed for etching
- **Adjust etch recipe** to reduce overetching [Schmidt]
  - ↳ Change  $\text{C}_4\text{F}_8$  flow rate, pressure, etc., to enhance passivation and reduce overetching
  - ↳ **Issue:** Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches
- Use **lower frequency plasma** to avoid surface charging [Morioka]
  - ↳ Low frequency → more ions with low directionality and kinetic energy → neutralizes (-) potential barrier at trench entrance
  - ↳ Allows  $e^-$ 's to reach the trench base and neutralize (+) charge → maintain charge balance inside the trench

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    30

30

### Metal Interlayer to Prevent "Footing"

UC Berkeley

Pre-defined metal interlayer grounded to substrate supplies e's to neutralize (+) charge and prevent charge accumulation at the Si-insulator interface

(a) Photolithography 1 (sacrificial)

(b) Preparatory trenches

(c) Metal interlayer deposition

(d) Lift-off (remove PR)

(e) Anodic Bonding

(f) Silicon Thinning

(g) Photolithography 2

(h) DRIE

(i) Remove metal interlayer

(j) Metallize

EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      31

31

### Footing Prevention (cont.)

UC Berkeley

- **Below:** DRIE footing over an oxide stop layer
- **Right:** efficacy of the metal interlayer footing prevention approach

[Kim, Stanford]

[Kim, Seoul Nat. Univ.]

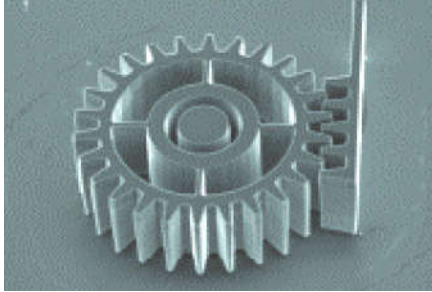
EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      32

32

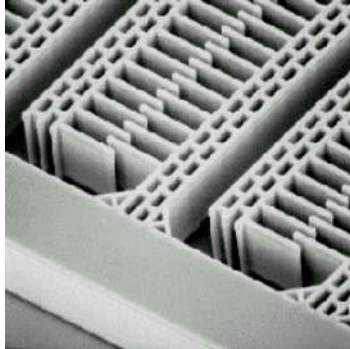


**DRIE Examples**

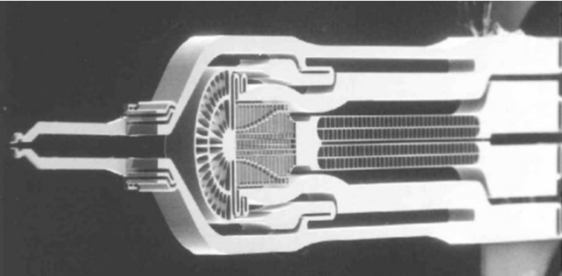
UC Berkeley



High aspect-ratio gear



Tunable Capacitor  
[Yao, Rockwell]



Microgripper  
[Keller, MEMS Precision Instruments]


EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    33

33

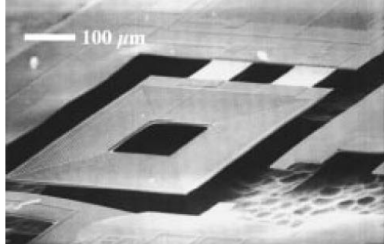
**Vapor Phase Etching of Silicon**

UC Berkeley

- Vapor phase Xenon Difluoride ( $XeF_2$ )  
 $2XeF_{2(g)} + Si_{(s)} \rightarrow 2Xe_{(g)} + SiF_{4(g)}$
- Set-up:
  - ↪ Xe sublimates at room T
  - ↪ Closed chamber, 1-4 Torr
  - ↪ Pulsed to control exothermic heat of reaction
- Etch rate: 1-3  $\mu\text{m}/\text{min}$ , isotropic
- Etch masks: photoresist,  $SiO_2$ ,  $Si_3N_4$ , Al, other metals
- Issues:
  - ↪ Etched surfaces have granular structure, 10  $\mu\text{m}$  roughness
  - ↪ Hazard:  $XeF_2$  reacts with  $H_2O$  in air to form Xe and HF




Xactix  $XeF_2$  Etcher



Inductor w/ no substrate [Pister]

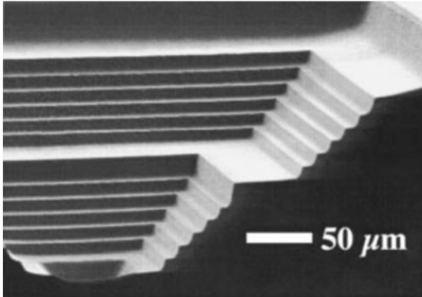
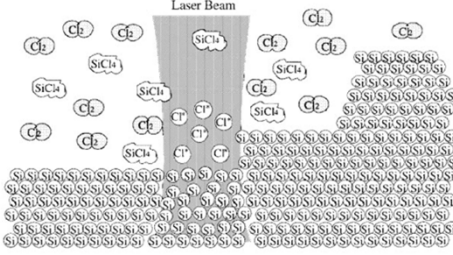
EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    34

34

 UC Berkeley

## Laser-Assisted Chemical Etching

- Laser creates Cl radicals from  $\text{Cl}_2 \rightarrow$  reaction forms  $\text{SiCl}_4$
- Etch rate:  $100,000 \mu\text{m}^3/\text{s}$ 
  - ↳ Takes 3 min. to etch  $500 \times 500 \times 125 \mu\text{m}^3$  trench
- Surface roughness: 30 nm rms
- Serial process: patterned directly from CAD file
- At right:
  - ↳ Laser assisted etching of a  $500 \times 500 \mu\text{m}^2$  terraced silicon well
  - ↳ Each step is  $6 \mu\text{m}$ -deep



EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    35


35

 UC Berkeley

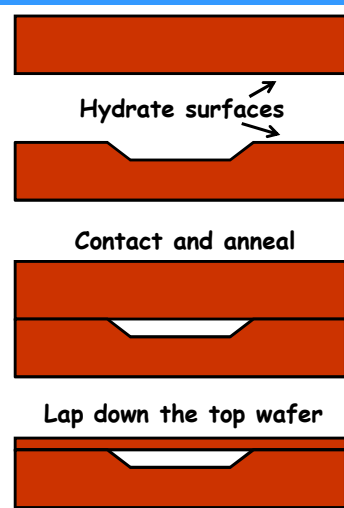
## Wafer Bonding

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    36

36

 **Fusion Bonding**


- Two ultra-smooth (<1 nm roughness) wafers are bonded without adhesives or applied external forces
- **Procedure:**
  - ↳ Prepare surfaces: must be smooth and particle-free
    - ↳ Clean & hydrate: O<sub>2</sub> plasma, hydration, or HF dip
  - ↳ When wafers are brought in contact at room temperature, get hydrogen bonding and/or van der Waals forces to hold them together
  - ↳ Anneal at 600-1200°C to bring the bond to full strength
- **Result:** a bond as strong as the silicon itself!



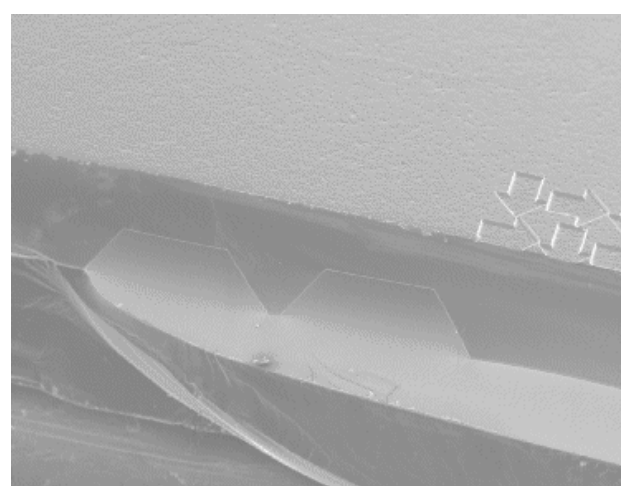
Works for Si-to-Si bonding and Si-to-SiO<sub>2</sub> bonding

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    37

37

 **Fusion Bonding Example**

- **Below:** capacitive pressure sensor w/ fusion-bonded features



[Univ. of Southampton]

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    38

38

**Anodic Bonding**

UC Berkeley

- Bonds an electron conducting material (e.g., Si) to an ion conducting material (e.g., sodium glass = Pyrex)
- Procedure/Mechanism:
  - ↪ Press Si and glass together
  - ↪ Elevate temperature: 180-500°C
  - ↪ Apply (+) voltage to Si: 200-1500V
    - (+) voltage repels Na<sup>+</sup> ions from the glass surface
    - Get net (-) charge at glass surface
    - Attractive force between (+) Si and (-) glass → intimate contact allows fusing at elevated temp.
  - ↪ Current drops to zero when bonding is complete

The schematic shows a Silicon (Si) wafer on top of a Glass wafer, both on a Hot plate. A positive voltage is applied to the Si wafer. The graphs show:
 

- Temperature:** Starts at 25°C, rises to 400°C. Note: 'Elevated temperature: the glass becomes slightly conducting'.
- Pressure:** Starts at 1000 mbar, drops to 10<sup>-3</sup> mbar for 'Low pressure bonding', then returns to 1000 mbar.
- Voltage:** Starts at 0 Volts, rises to 800 Volts. Note: 'High voltage: a large electric field pulls the wafers into intimate contact'.
- Current:** Starts at 0 mA, rises to 10 mA, then drops to 1 mA for 'Current stabilisation'.

EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      39

39

**Anodic Bonding (cont.)**

UC Berkeley


- **Advantage:** high pressure of electrostatic attraction smoothes out defects
- **Below:** 100 mm wafers, Pyrex glass 500 μm-thick, 430°C, 800V, N<sub>2</sub> @ 1000 mbar

The images show the progression of anodic bonding on a wafer:
 

1. after 5 sec: Only center bond pin active
2. after 20 sec: All bond pins active
3. after 2,5 min: Bond front spreads
4. after 8 min: Bond 98% completed

EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      40


40

 **Metal Layer Bonding**

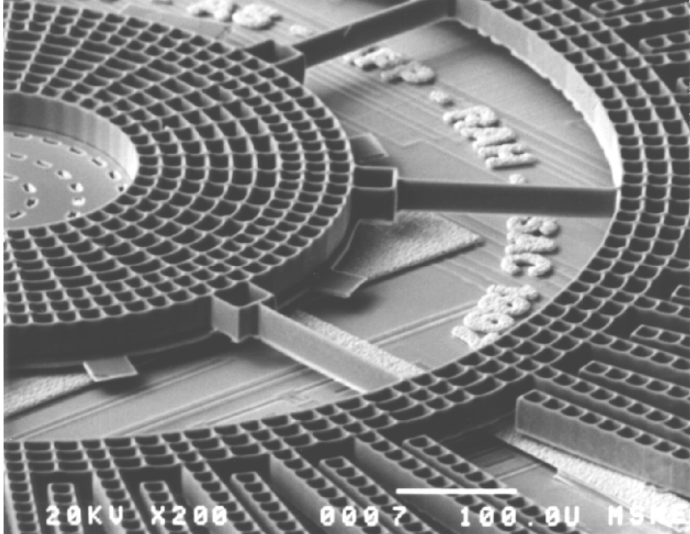
- Pattern seal rings and bond pads photolithographically
- **Eutectic bonding**
  - ↗ Uses eutectic point in metal-Si phase diagrams to form silicides
  - ↗ Au and Si have eutectic point at 363°C
  - ↗ Low temperature process
  - ↗ Can bond slightly rough surfaces
  - ↗ Issue: Au contamination of CMOS
- **Solder bonding**
  - ↗ PbSn (183°C), AuSn (280°C)
  - ↗ Lower-T process
  - ↗ Can bond very rough surfaces
  - ↗ Issue: outgassing (not good for encapsulation)
- **Thermocompression**
  - ↗ Commonly done with electroplated Au or other soft metals
  - ↗ Room temperature to 300°C
  - ↗ Lowest-T process
  - ↗ Can bond rough surfaces with topography

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    41

41

 **Thermocompression Bonding**


- Below: Transfer of hexsil actuator onto CMOS wafer



[Singh, et al, Transducers'97]

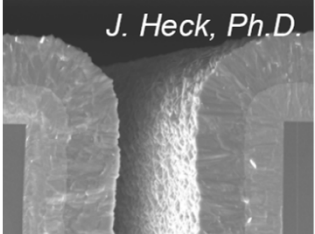
EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    42

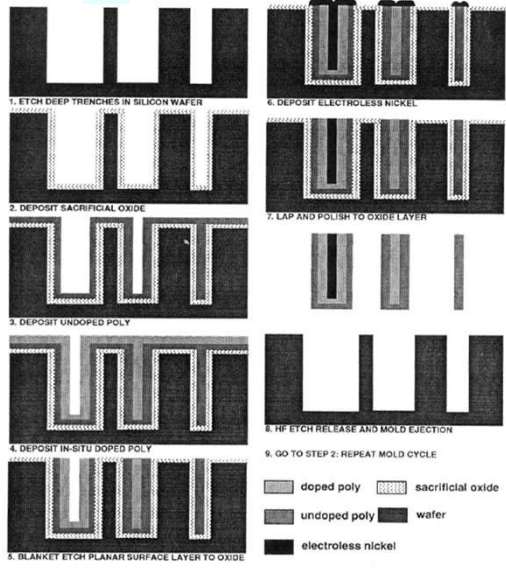
42



## Hexsil MEMS


- Achieves high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Design with honeycomb structure for strength





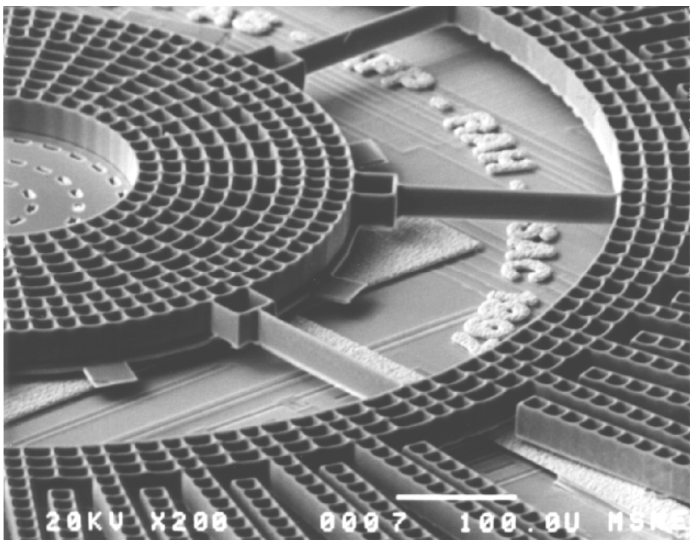
EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
43

43



## Hexsil MEMS Actuator

- Below: Transfer of hexsil actuator onto CMOS wafer



[Singh, et al, Transducers'97]

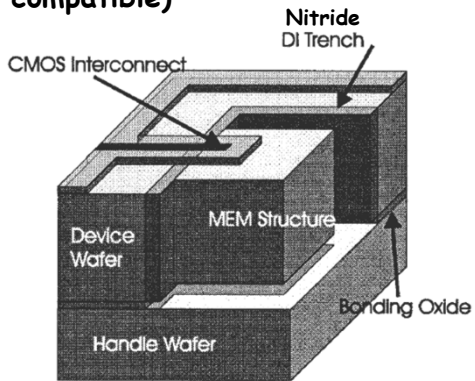
EE C245: Introduction to MEMS Design
LecM 6
C. Nguyen
9/28/07
44

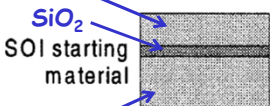
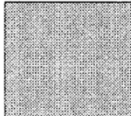
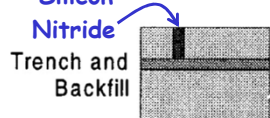
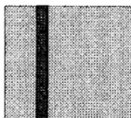

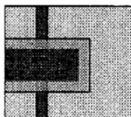
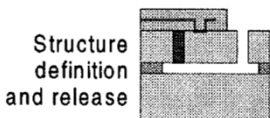
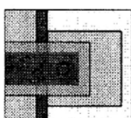
44

**Silicon-on-Insulator (SOI) MEMS**

UC Berkeley

- No bonding required
- Si mechanical structures anchored by oxide pedestals
- Rest of the silicon can be used for transistors (i.e., CMOS compatible)



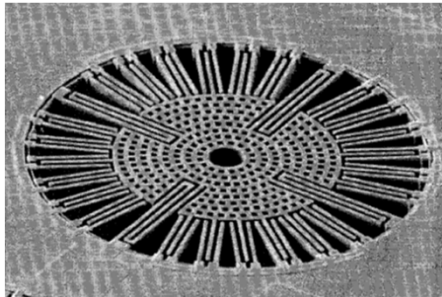
	Cross Section	Top View
SOI starting material		
Trench and Backfill		
Integrated Circuitry		
Structure definition and release		

EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      45

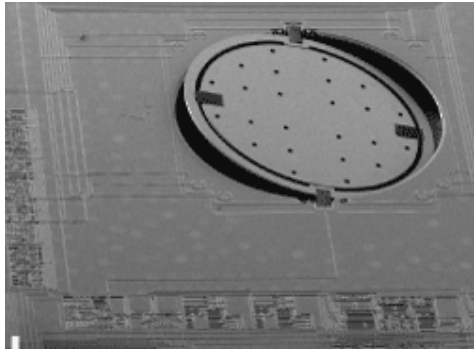
45

**SOI MEMS Examples**

UC Berkeley



[Brosnihan]



Micromirror  
[Analog Devices]

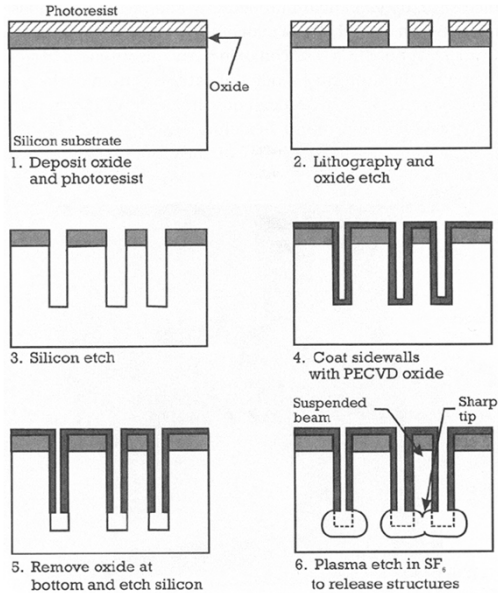
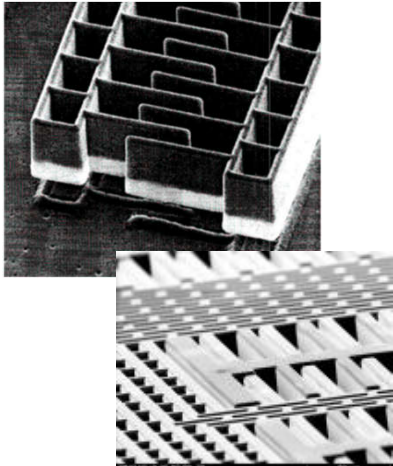
EE C245: Introduction to MEMS Design      LecM 6      C. Nguyen      9/28/07      46

46

### The SCREAM Process

**UC Berkeley**

- **SCREAM: Single Crystal Reactive Etching and Metallization process**



The diagram illustrates the SCREAM process in six steps:

1. Deposit oxide and photoresist
2. Lithography and oxide etch
3. Silicon etch
4. Coat sidewalls with PECVD oxide
5. Remove oxide at bottom and etch silicon
6. Plasma etch in  $\text{SF}_6$  to release structures

Labels in the diagram include: Photoresist, Oxide, Silicon substrate, Suspended beam, and Sharp tip.

EE C245: Introduction to MEMS Design    LecM 6    C. Nguyen    9/28/07    47

47