Non-Ideal Operational Amplifiers

Actual Op Amps Are Not Ideal

- Actual op amps, of course, are not ideal; rather, they...
  - Generate noise
  - Have finite gain, $A_o$
  - Have finite bandwidth, $\omega_b$
  - Have finite input resistance, $R_i$
  - Have finite input capacitance, $C_i$
  - Have finite output resistance, $R_o$
  - Have an offset voltage $V_{OS}$ between their (+) and (-) terminals
  - Have input bias currents
  - Have an offset $I_{OS}$ between the bias currents into the (+) and (-) terminals
  - Have finite slew rate
  - Have finite output swing (governed by the supply voltage used, $-V$ to $+V$)
- And what's worse: All of the above can be temperature (or otherwise environmentally) dependent!

Finite Op Amp Gain and Bandwidth

- For an ideal op amp: $A = \infty$
- In reality, the gain is given by: $A(s) = \frac{A_0}{s + \omega_b}$
- For $\omega >> \omega_b$:
  - $A(s) \approx \frac{A_0}{\omega_b}$
  - $\omega >> \omega_b$ Integrator w/ time const. $1/\omega_b$
  - $A(s) \approx \frac{A_0}{s + \omega_b}$ Open-loop response of the amplifier.
  - $\omega >> \omega_b$
  - $A(s) \approx \frac{A_0}{s}$
  - $\omega >> \omega_b$ Integrator w/ time const. $1/\omega_b$
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Op Amp Non-Idealities

Op Amp Non-Idealities → $R_i$ & $R_0$

Input resistance $R_i$ and Output Resistance $R_0$:
With finite $R_i$ and $R_0$, and finite gain and BW, the op amp equivalent circuit becomes:

- $R_i$ and $R_0$:
- Add an output $C_0$ to model a single pole response, where

\[
 w_0 = \frac{1}{R_0 C_0}
\]

Op Amp Non-Idealities

Input Offset Voltage $V_{0S}$

Ideal case: $v_0 = 0$
Reality: $v_0 \neq 0$ (usually, $v_0 = L^+$ or $L^-$: it rails out!)

Why? Internal mismatches within the op amp → cause a dc offset. Model this with an equivalent input offset voltage $V_{0S}$.

Typically, $V_{0S} = 1 \text{mV} - 5 \text{mV}$

Effect of $V_{0S}$ on Op Amp Circuits

Example: Non-Inverting Amplifier

\[
 V_0 = V_{0S} \left(1 + \frac{R_2}{R_1}\right)
\]

e.g., $\frac{R_2}{R_1} = 9$, $V_{0S} = 5 \text{mV} \rightarrow V_0 = 50 \text{mV}$

(not so bad ...)

Effect of $V_{0S}$ on Op Amp Circuits (cont.)

Example: Integrator

To fix this, place a resistor in shunt with the $C$ → then:

\[
 v_0 = V_{0S} + \frac{1}{C R} \int v_{0S} dt
\]

\[
 = V_{0S} + \frac{1}{C R} \int v_{0S} dt
\]

\[
 = V_{0S} \left(1 + \frac{t}{RC}\right) + v_C|_{t=0}
\]

Will continue to increase until op amp saturates
Integrator-Based Diff. Position Sensing

\[ i_0 \approx \frac{N_f(C_F) - N_f(C_p)}{C_p} \]

Buffer-Bootstrapped Position Sensing

\[ C_p \approx \frac{C_p}{C_p} \]

Unity Gain Buffer

\[ \begin{align*}
    &C_p \approx \frac{C_p}{C_p} \\
    &V_0 \approx \frac{V_0}{V_0} \\
    &C_{pd} = \text{gate-to-drain capacitance of the input MOS transistor}
\end{align*} \]

Bootstrap the ground lines around the interconnect and bond pads

\[ \text{No voltage across } C_p \]

\[ \text{It's effectively not there!} \]

Effect of Finite Op Amp Gain

\[ \text{Total ADXL-50 Sense } C \approx 100 \text{ff} \]

Integration of MEMS and Transistors
Integrate or Not?

* Benefits:
  - Lower parasitic capacitance and resistance → improved sensitivity and resolution, higher operation frequency
  - Better reliability
  - Reduced size → lower cost?
  - Reduced packaging complexity → integration is a form of packaging → lower cost?
  - Higher integration density supports greater functionality

* Challenges:
  - Temperature ceilings imposed by the transistors or MEMS
  - Protecting one process from the other
  - Surface topography of MEMS
  - Material incompatibilities
  - Multiplication of yield losses (versus non-integrated)
  - Acceptance by transistor foundries

Merged MEMS/Transistor Technologies (Process Philosophy)

MEMS-Last:
- Circuits → Pass/Prot. → μMechanics
- Fully Integrated μMechanical Resonator Oscillator

MEMS-First:
- μMechanics → Pass/Prot. → Circuits

Mixed:
- Circuits → Pass/Prot. → μMechanics → Pass/Prot.

* Mixed:
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product

* MEMS-first or MEMS-last:
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

Analog Devices BiMEMS Process

* Interleaved MEMS and 4 μm BiMOS processes (28 masks)
* Diffused n+ runners used to interconnect MEMS & CMOS
* Relatively deep junctions allow for MEMS poly stress anneal
* Used to manufacture the ADXL-50 accelerometer and Analog Devices family of accelerometers
Analog Devices BiMEMS Process (cont)

* Examples:

Old \[\rightarrow\] New

Analog Devices ADXL 78

Analog Devices ADXL-202 Multi-Axis Accelerometer

* Can you list the advances in the process from old to new?

MEMS-First Integration

- Modular technology minimizes product updating effort
  - Module 1: micromachining process (planar technology)
  - Module 2: transistor process (planar IC technology)
- Adv.: (ideally) no changes needed to the transistor process
- Adv.: high temperature ceiling for some MEMS materials
- Challenges:
  - Reducing topography after MEMS processing so transistors can be processed
  - Maximizing the set of permissible MEMS materials: the materials must be able to withstand transistor processing temperatures
  - Getting transistor foundries to accept pre-processed wafers

Merged MEMS/Transistor Technologies (Process Philosophy)

Post-Circuits: Circuits \[\rightarrow\] Pass/Prot. \[\rightarrow\] Mechanics

Mixed: Circuits \[\rightarrow\] Pass/Prot. \[\rightarrow\] Mechanics \[\rightarrow\] Pass/Prot.

Pre-Circuits: Mechanics \[\rightarrow\] Pass/Prot. \[\rightarrow\] Circuits

* Mixed:
  - problem: multiple passivation/protection steps \[\Rightarrow\] large number of masks required
  - problem: custom process for each product

MEMS-first or MEMS-last:
  - Adv.: modularity \[\Rightarrow\] flexibility \[\Rightarrow\] less development time
  - Adv.: low pass./protection complexity \[\Rightarrow\] fewer masks

MEMS-First Integration

- Problem: structural topography interferes with lithography
  - difficult to apply photoresist for submicron circuits

- Soln.: build micromechanics in a trench, then planarize before circuit processing [Smith et al, IEDM'95]
MEMS-First Ex: Sandia’s iMEMS

* Used to demonstrate functional fully integrated oscillators

* Issues:
  - lithography and etching may be difficult in trench $\Rightarrow$ may limit dimensions (not good for RF MEMS)
  - $\mu$m-scale mechanical material must stand up to IC temperatures ($>1000^\circ$C) $\Rightarrow$ problem for some metal materials
  - might be contamination issues for foundry ICs

[Smith et al, IEDM’95]

Bosch/Stanford MEMS-First Process

* Single-crystal silicon microstructures sealed under epi-poly encapsulation covers

* Many masking steps needed, but very stable structures

Problems With MEMS-First

* Many masking steps needed, plus CMP required $\Rightarrow$ cost can grow if you’re not careful

* Processes using trenches sacrifice lithographic resolution in microstructures

* MEMS must withstand transistor processing temperatures
  - Precludes the use of structural materials with low temperature req’mts: metals, polymers, etc.

* Exotic MEMS (e.g., ZnO) that can contaminate transistors during their processing are not permissible
  - thus, not truly modular

* Foundry acceptance not guaranteed and might be rare

Foundry Acceptance of MEMS-First?

* Is a CMP’ed silicon surface sufficiently pure for fabrication of aggressively scaled transistors? How about if an oxide is grown over the CMP’ed surface and removed via a wet etch to yield a “pristine” surface?

* Is epi silicon grown as part of a sealing process sufficiently pure for fabrication of aggressively scaled transistors?

* CMOS is many times more difficult to run than MEMS
  - Feature sizes on the nm scale for billions of devices
  - Contamination a big issue: many foundries may not accept pre-processed wafers for contamination reasons
  - Many foundries will not accept any pre-processed wafers, MEMS or not $\Rightarrow$ just can’t guarantee working transistor circuits with unknowns in starting silicon

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Merged MEMS/Transistor Technologies (Process Philosophy)

Pre-Circuits: μMechanics
Pass/Prot.
Mixed:
Circuits → μMechanics → Pass/Prot.

Post-Circuits: Circuits → Pass/Prot. → μMechanics

* Mixed:
- Problem: multiple passivation/protection steps ⇒ large number of masks required
- Problem: custom process for each product

* MEMS-first or MEMS-last:
  - Adv.: modularity ⇒ flexibility ⇒ less development time
  - Adv.: low pass./protection complexity ⇒ fewer masks

MEMS-Last Integration

* Modular technology minimizes product updating effort
  - Module 1: transistor process (planar IC technology)
  - Module 2: micromachining process (planar technology)

* Adv.: foundry friendly
  - Virtually any foundry can be used ⇒ can use the lowest cost transistor circuits (big advantage)

* Adv.: topography after circuit fabrication is quite small, especially given the use of CMP to planarize the metallization layers

* Issue: limited thermal budget ⇒ limits the set of usable structural materials
  - Metallization goes bad if temperature gets too high
  - Aluminum grows hillocks and spikes junctions if T > 500°C
  - Copper diffusion can be an issue at high temperature
  - Low-k dielectrics used around metals may soon lower the temperature ceiling to only 320°C

Berkeley Polysilicon MICS Process

* Uses surface-micromachined polysilicon microstructures with silicon nitride layer between transistors & MEMS
  - Polysilicon dep. T ~ 600°C, nitride dep. T ~ 835°C
  - 1100°C RTA stress anneal for 1 min.
  - Metal and junctions must withstand temperatures ~ 835°C
  - Tungsten metallization used with TiSi2 contact barriers
  - In situ doped structural polySi: rapid thermal annealing

Surface Micromachining

* Fabrication steps compatible with planar IC processing
Single-Chip Ckt/MEMS Integration

- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)

To allow the use of >600°C processing temperatures, tungsten (instead of aluminum) is used for metallization

[Nguyen, Howe 1993]

Usable MEMS-Last Integration

- Problem: tungsten is not an accepted primary interconnect metal
- Challenge: retain conventional metallization
  - minimize post-CMOS processing temperatures
  - explore alternative structural materials (e.g., plated nickel, SiGe [Franke, Howe et al, MEMS'99])
  - Limited set of usable structural materials → not the best situation, but workable

Poly-SiGe MICS Process

- MICS = "Modular Integration of Circuits and Structures"
- MEMS-last process, where SiGe micromechanics are planar processed directly above conventional foundry circuits
  - enabled by lower deposition temperature of SiGe ~450°C
  - Adv.: alleviates contamination issues of pre-circuit processes, allowing a wider choice of IC technologies

Polysilicon Germanium

- Deposition
  - LPCVD thermal decomposition of GeH₄ and SiH₄ or Si₂H₆
  - Rate >50 Å/min, T < 475°C, P = 300-600 mT
  - At higher [Ge]: rate ↑, T ↓
  - In-situ doping, ion implantation

- Dry Etching
  - Similar to poly-Si, use F, Cl, and Br containing plasmas
  - Rate ~0.4 μm/min

- Wet Etching
  - H₂O₂ @ 90°C: can get 4 orders of magnitude selectivity between >80% and <50% Ge content
  - Good release etchant
**Poly-SiGe Mechanical Properties**

- Conformal deposition
- Low as-deposited stress (when its done right)
- Young's modulus ~ 146 GPa (for poly-Si$_{0.35}$Ge$_{0.65}$)
- Density ~4280 kg/m$^3$
- Acoustic velocity ~5840 m/s (25% lower than polysilicon)
- Harder to achieve high frequency devices
- Fracture strain 1.7% (compared to 1.5% for MUMPs polySi)
- Q=30,000 for n-type poly-Ge in vacuum

**UCB Poly-SiGe MICS Process**

- 2 µm standard CMOS process w/ Al metallization
- P-type poly-Si$_{0.35}$Ge$_{0.65}$ structural material; poly-Ge sacrificial material
- Process:
  - Passivate CMOS w/ LTO @ 400°C
  - Open vias to interconnect runners
  - Deposit & pattern ground plane
  - RTA anneal to lower resistivity (550°C, 30s)

**ASIMPS Ckt/MEMS Integration Process**

- MEMS constructed from metal/insulator laminates of foundry CMOS
- Top metal layer used as etch mask for CHF$_3$/O$_2$ oxide etch
- Structures released via a final SF$_6$ isotropic dry etch
- Independent electrostatic actuation possible due to multiple insulated metal layers
- Stress issues can be tricky
- Must design defensively against warping

**ASIMPS Ckt/MEMS Integration Process**

- Direct integration of Al/oxide MEMS structure with silicon CMOS or SiGe BiCMOS circuits
- Multiple electrodes within structures
- Derivatives for bulk silicon structures
Effect of Finite Op Amp Gain

Total ADXL-50 Sense $C \sim 100fF$

Unity Gain Buffer

\[ \frac{N_o}{N_i} = \frac{A_o(N_i - N_p)}{A_o(N_i - N_p) + N_o} \rightarrow \frac{N_o}{N_i} \approx \frac{A_o}{1 + A_o} \]

\[ C_{\text{eff}} = \frac{C_p}{1 + A_o} \]

Ex: $A_o \approx 10^3$, $C_p \approx 2pF$

\[ C_{\text{eff}} = \frac{2pF}{10^3} = 20fF \]

\[ C_{\text{eff}} \approx 0 \text{ not negligibly small compared with ADXL so } \text{distortion} \approx 0 \text{ pF}! \]