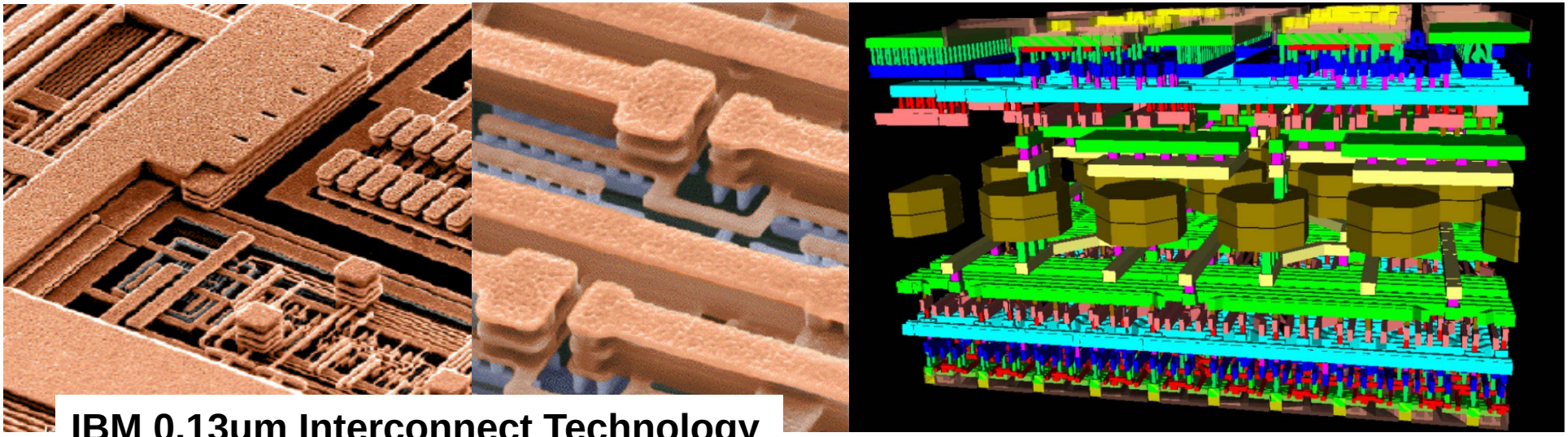


IBM 0.13um Interconnect Technology

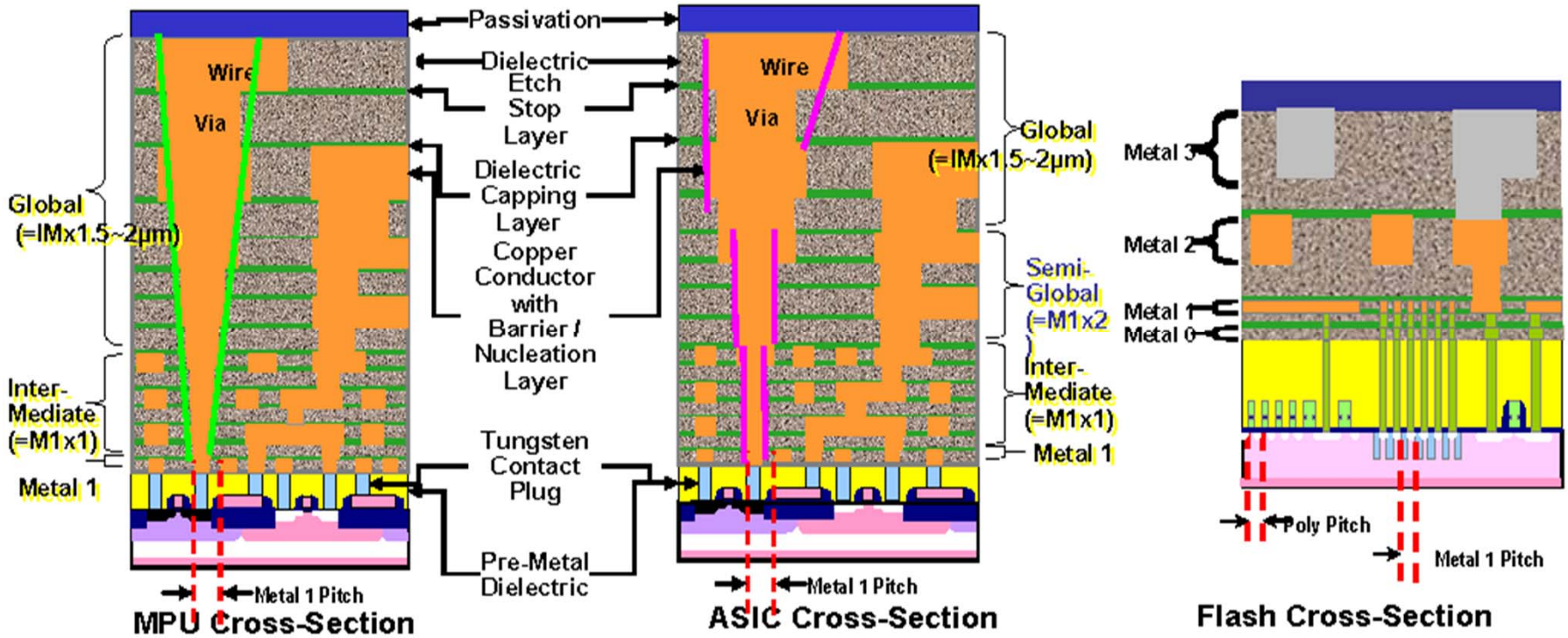
Lecture 17

- **BEOL and 3-D Integration**
  - Back-End-of-Line Technology
  - 3-D Integration Approaches

Reading: multiple research articles (reference list at the end of this lecture)

Back-End-of-Line (BEOL) Technology

Source: ITRS (2011)



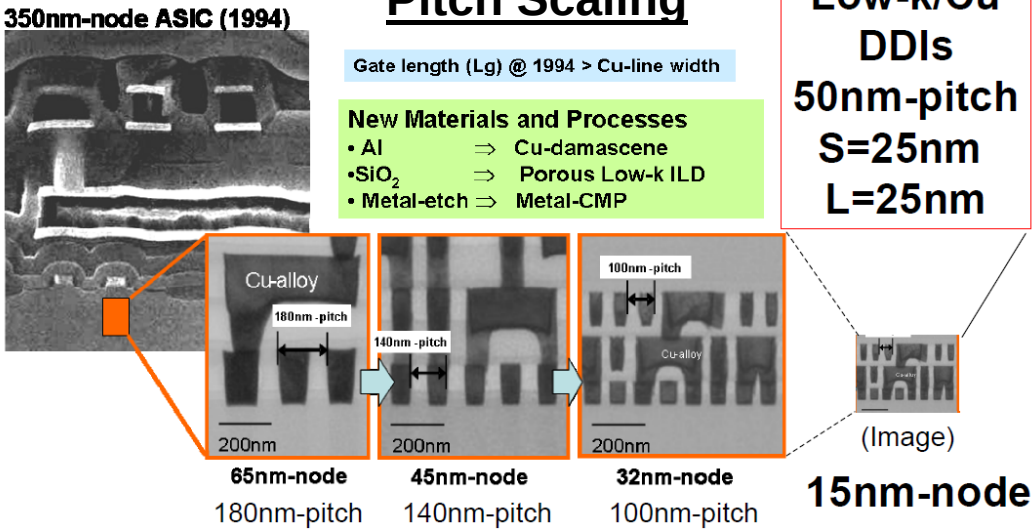
Hierarchy Wiring
(high # of metal layers and devices)

4-Pitches Wiring

Simple Wiring

BEOL Metal

Pitch Scaling

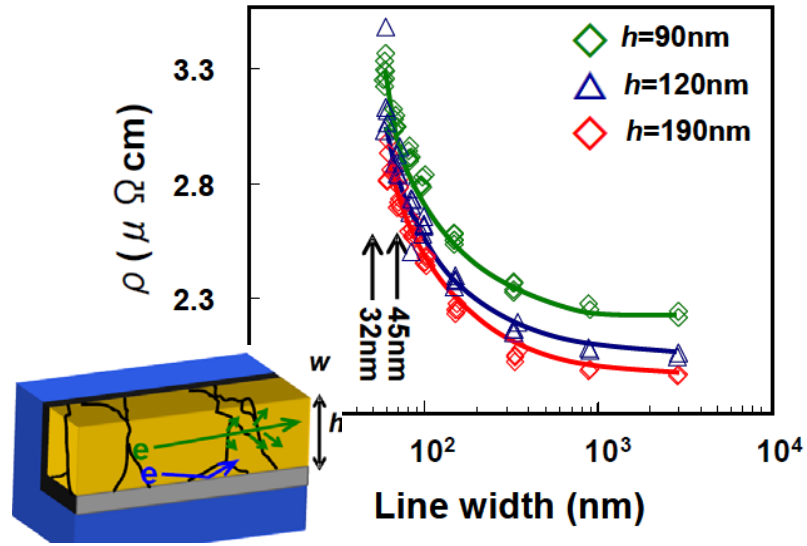


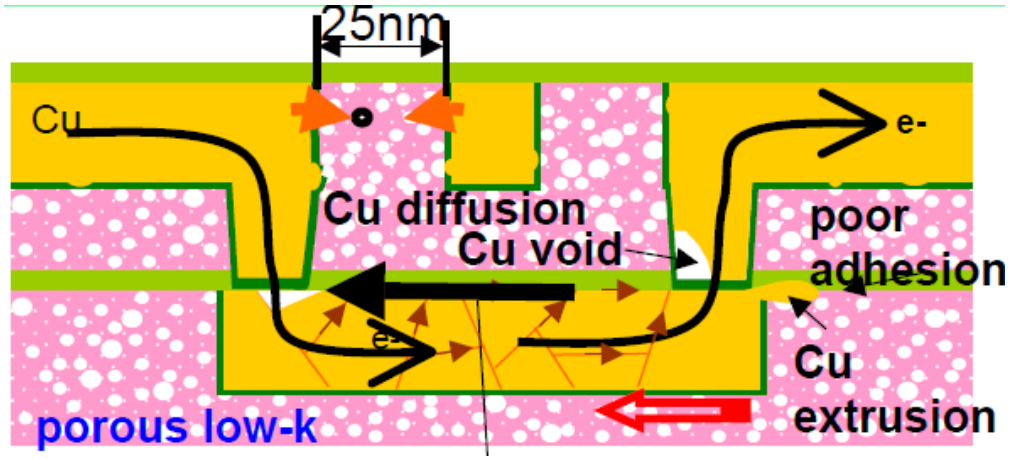
Gate length (Lg) @ 1994 > Cu-line width

New Materials and Processes
- Al ⇒ Cu-damascene
- SiO_2 ⇒ Porous Low-k ILD
- Metal-etch ⇒ Metal-CMP

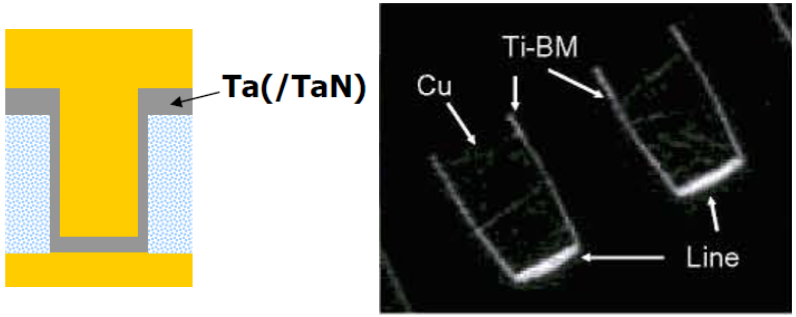
Low-k/Cu DDIs
50nm-pitch
S=25nm
L=25nm

Cu Resistivity *vs*. Geometry



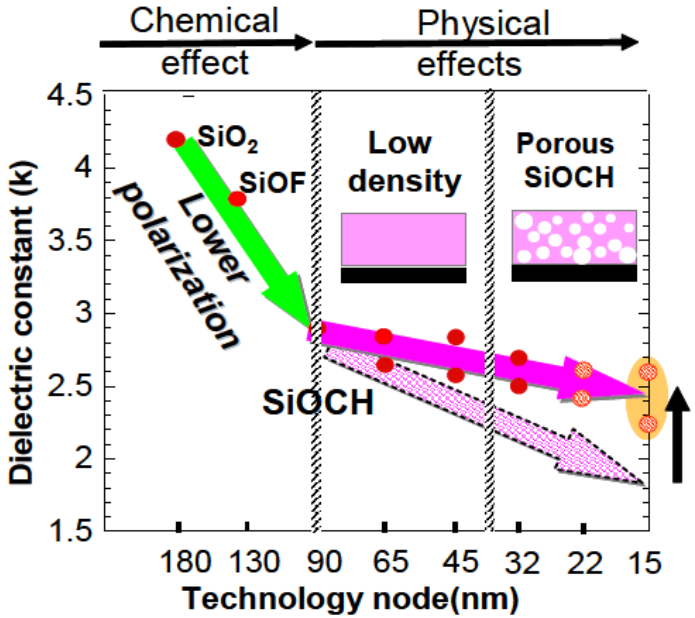


Barrier Layer to avoid Cu Diffusions

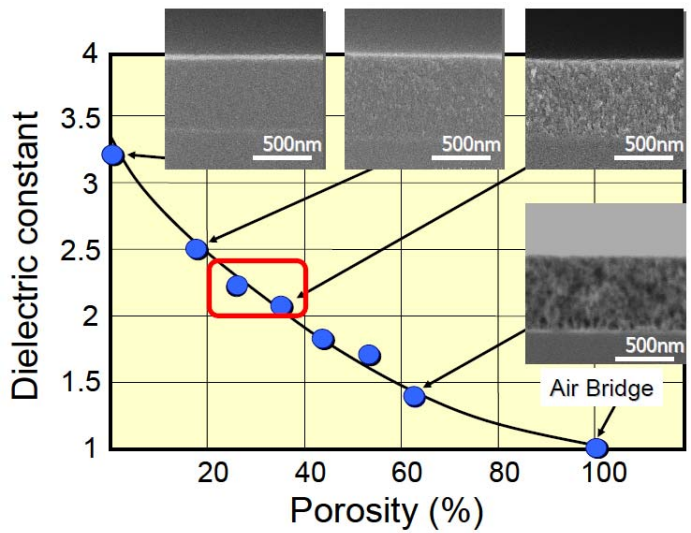


A. Tsukune, VLSI sc (2007)
Y. Hayashi, IEDM sc (2010)

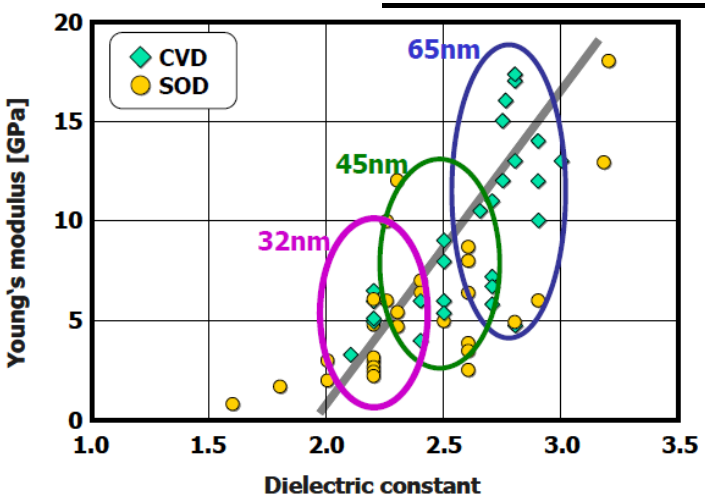
BEOL Dielectrics

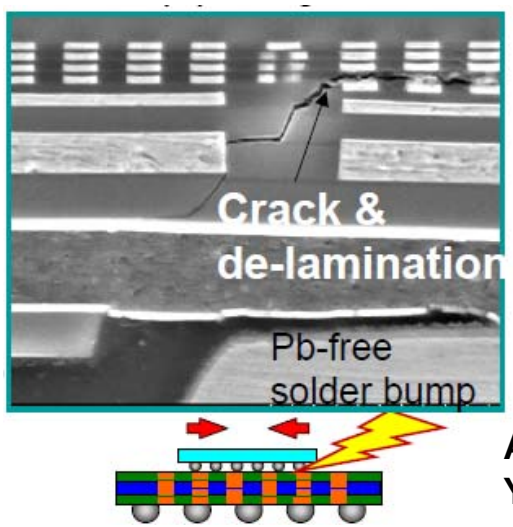


Porous Low-K Dielectric

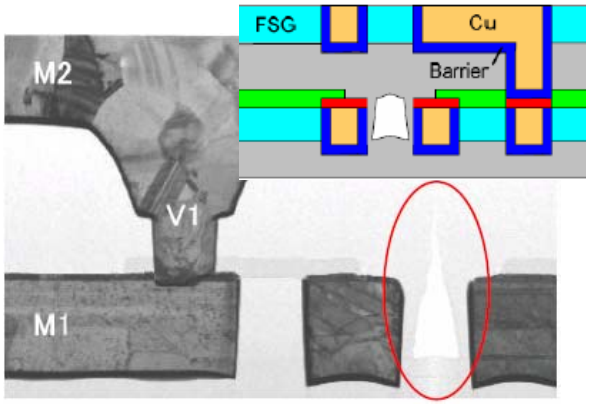


Mechanical Weakness



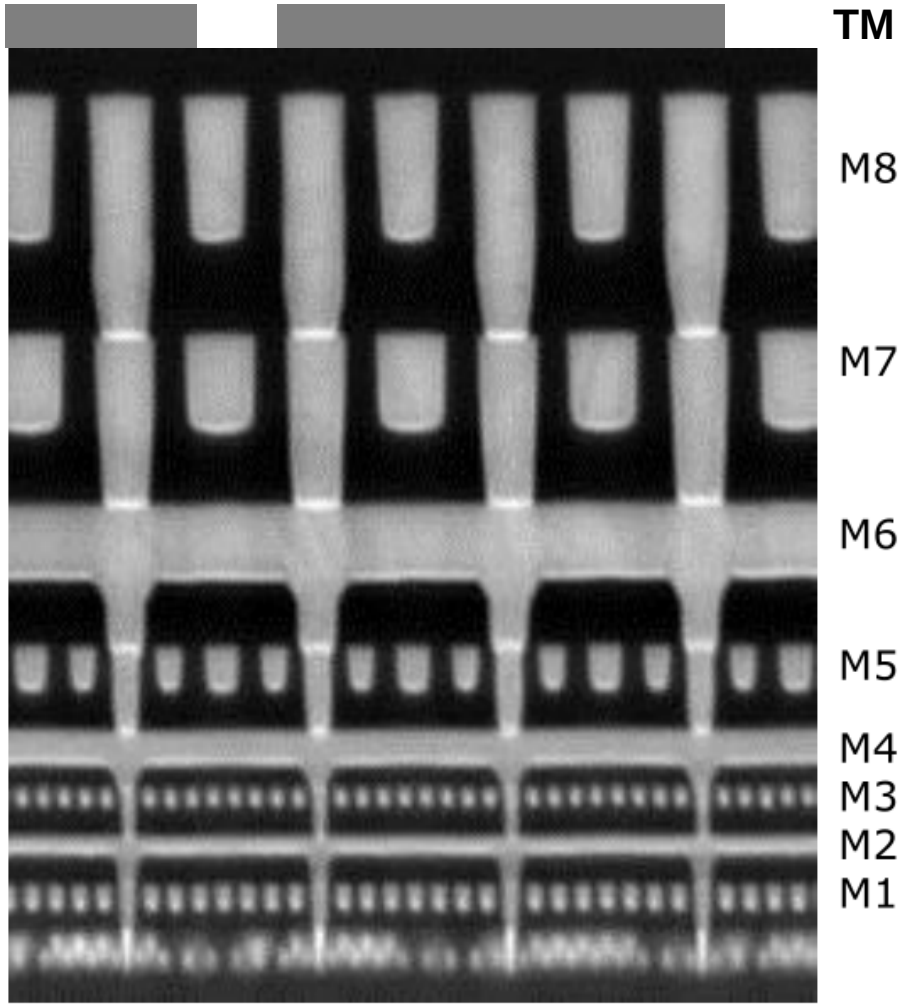


Air-gap Spacer



A. Tsukune, VLSI sc (2007)
Y. Hayashi, IEDM sc (2010)

BEOL Technology at 22nm



Layer	A	B	C	
TM	14	14	14	um
M10	-	-	360	nm
M9	-	360	360	nm
M8	360	240	160	nm
M7	240	160	108	nm
M6	160	108	80	nm
M5	108	80	80	nm
M4	80	80	80	nm
M3	80	80	80	nm
M2	80	80	80	nm
M1	90	90	90	nm

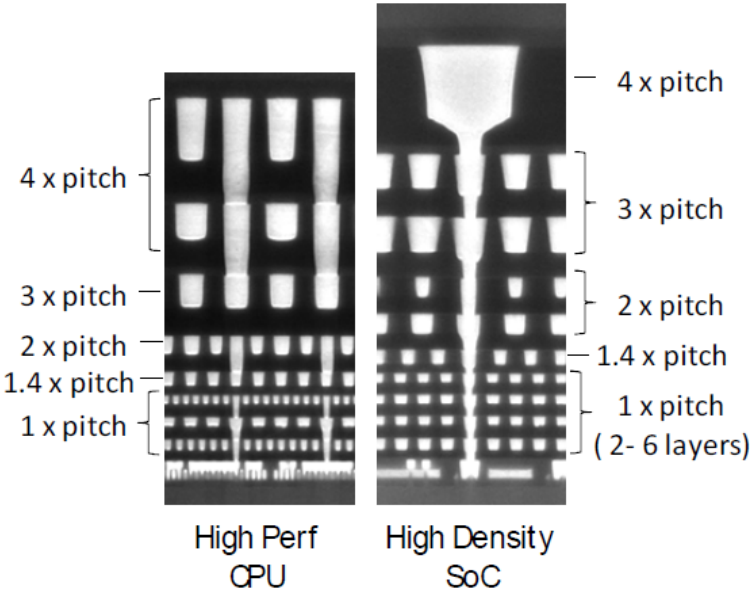
- **M1 requires double patterning.**
- **All other MLs use single patterning.**

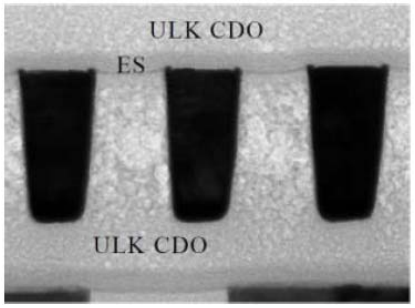
M. Bohr, Intel DF(2012)

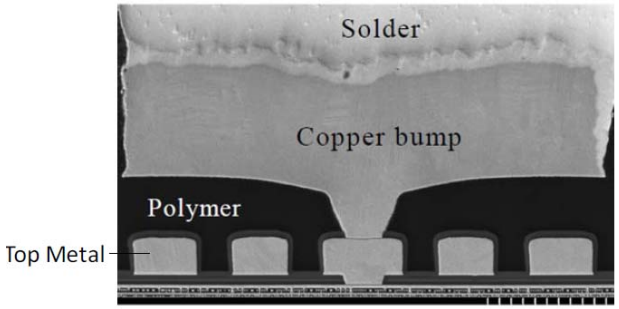
BEOL Technology at 22nm (Cont'd)

Table 2. 22 nm interconnect pitches

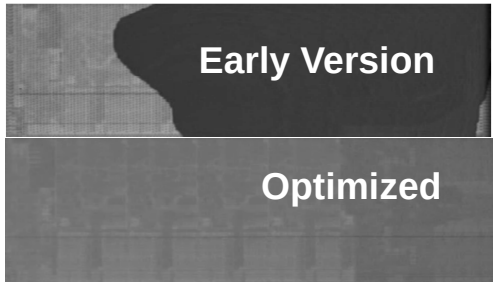
Layer	Pitch (nm)	Process	Dielectric Materials	CPU	SoC
Fin	60	-	-	Fin	Fin
Contact	90	SAC	-	Contact	Contact
M1	90	SAV	ULK CDO	M1	M1
MT - 1X	80	SAV	ULK CDO	M2/M3	2-6 layers
MT – 1.4x	112	SAV	ULK CDO	M4	Semi-global
MT – 2x	160	SAV	ULK CDO	M5	Semi-global
MT – 3x	240	SAV	ULK CDO	M6	Global Routing
MT – 4x	320 360	Via First	LK CDO	M7/8	Global Routing
MT - TOP	14 um	Plate Up	Polymer	M9	Top Metal







suppression of de-lamination under thermal stress



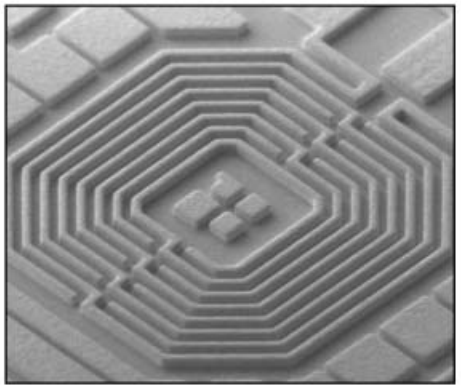
Technology Features:

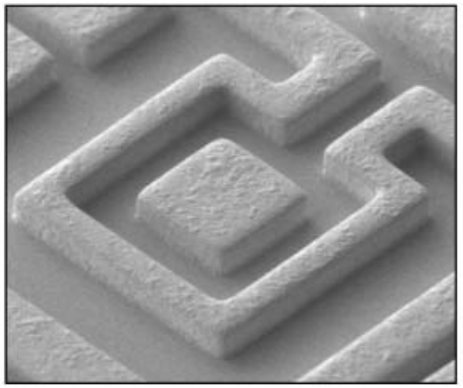
- **Carbon doped oxides (CDO) as ULK dielectrics**
- **Self-aligned via (SAV) process**

C.-H. Jan, IEDM (2012)
D. Ingerly, IITC (2012)

BEOL Passive Devices

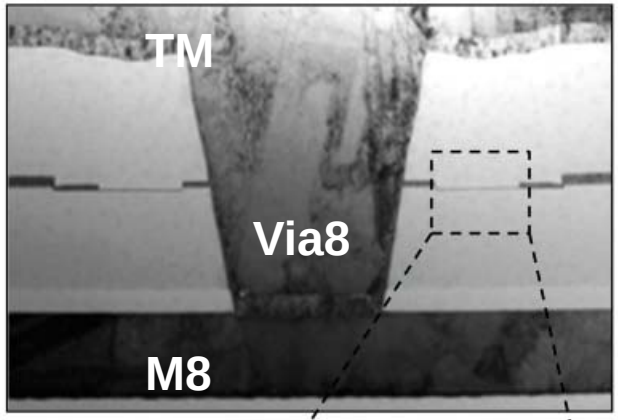
Inductor

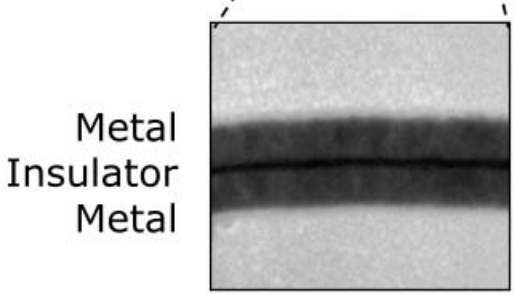




TM

MIM Capacitor





M8 – TM

M. Bohr, Intel DF(2012)
R. Brain, VLSI-T (2013)

Inductor technologies:

- Spiral coils in single Al- or Cu-metal levels are most common types
- Usually on top metal, for sufficient separation with substrate
- Low-k dielectrics is also preferred

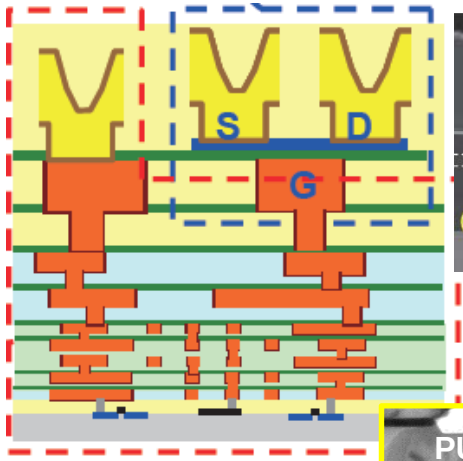
Capacitor technologies:

- Poly-Si/insulator/poly-Si (PIP)
  FEOL process → perform. degradation
  additional steps → added cost
- Metal/insulator/metal (MIM)
  BEOL process:
  LPCVD SiO_2: 1 fF/um^2
  PECVD SiO_2: 2 fF/um^2
  Ta_2O_5 + Al_2O_3: 10 fF/um^2

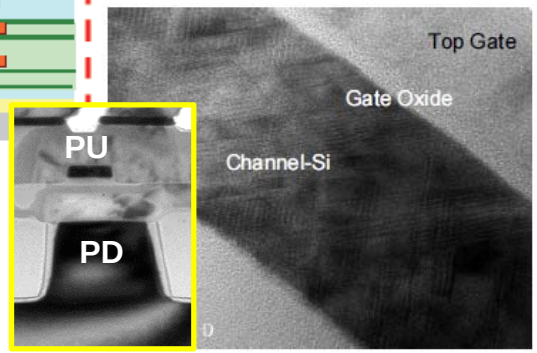
BEOL Active Devices

Thin-Film Transistors (TFT)

I/O Devices

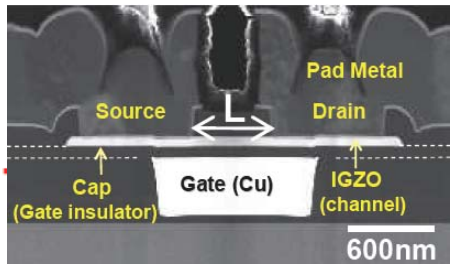


Core Logic



S.M. Jung, VLSI (2004)

K. Kaneko, VLSI (2011)

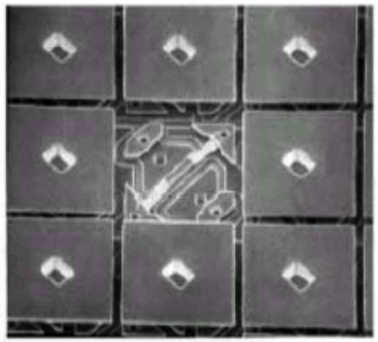


Applications:

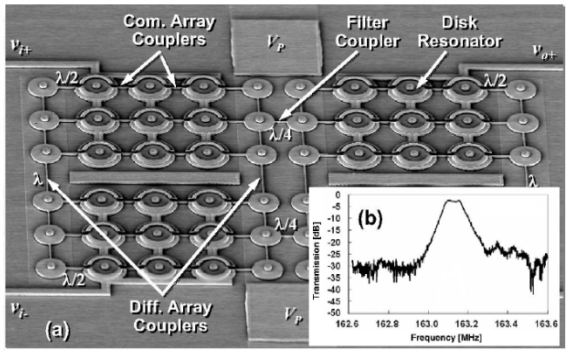
- Replacement for some existing MOSFETs (I/O devices, etc.)
- High precision, low noise resistors
- Display and Image technologies: LED, LCD and CCD

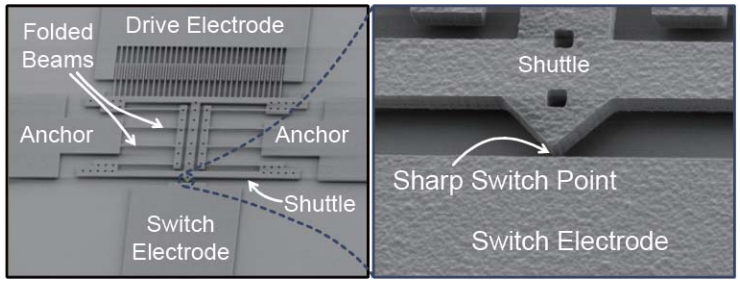
Micro-electromechanical Systems (MEMS)

TI's DMD Chip



S.S. Li, Transducers (2007)





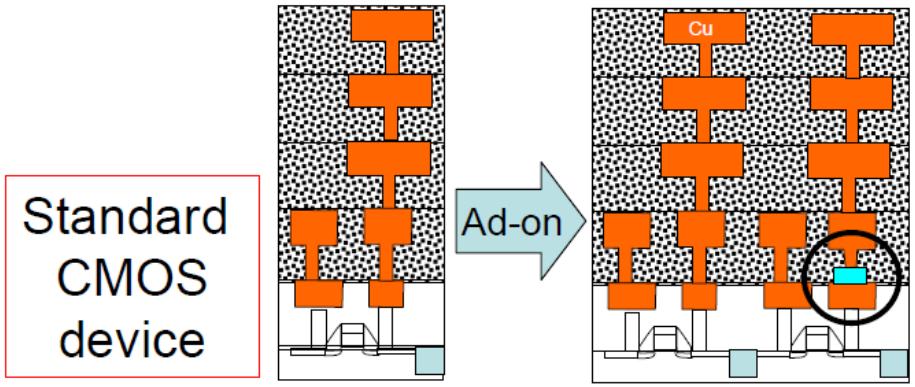
Y. Lin, VLSI (2013)

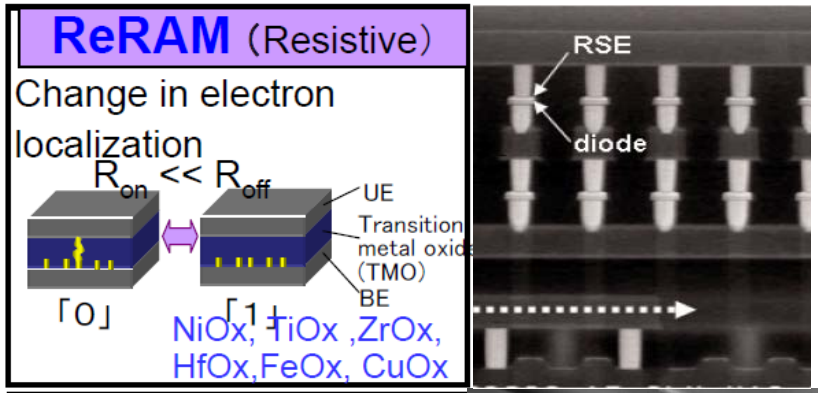
Applications:

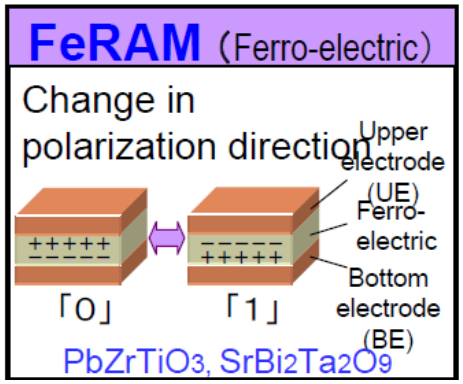
- Accelerometers, gyroscopes
- Optical MEMS
- Resonators, RF switches
- Power devices (PAs, charge pumps)

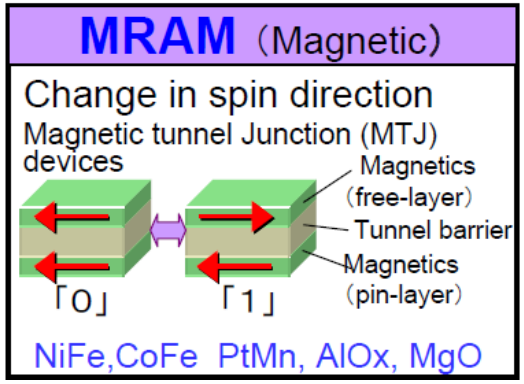
BEOL Non-Volatile Memories

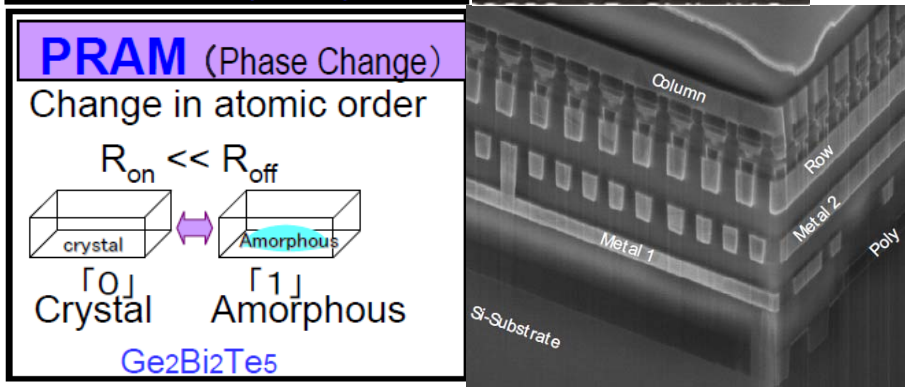
A. Kawahara, ISSCC (2012)









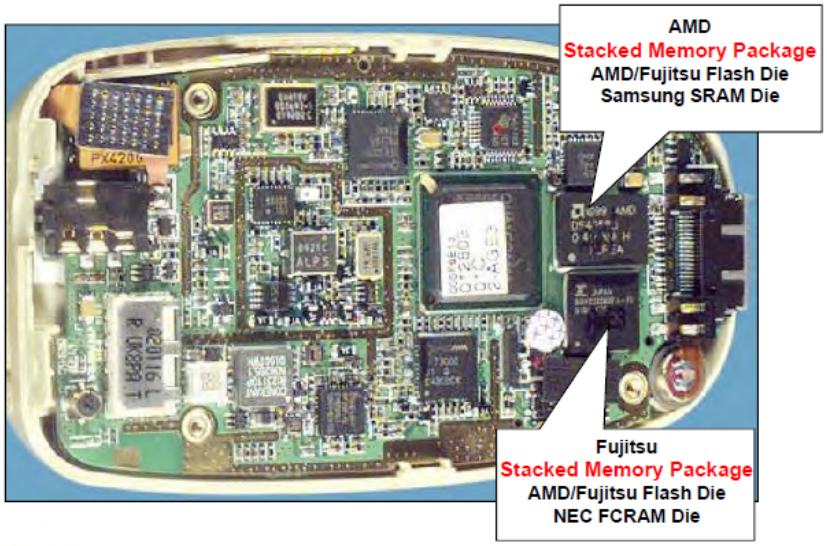


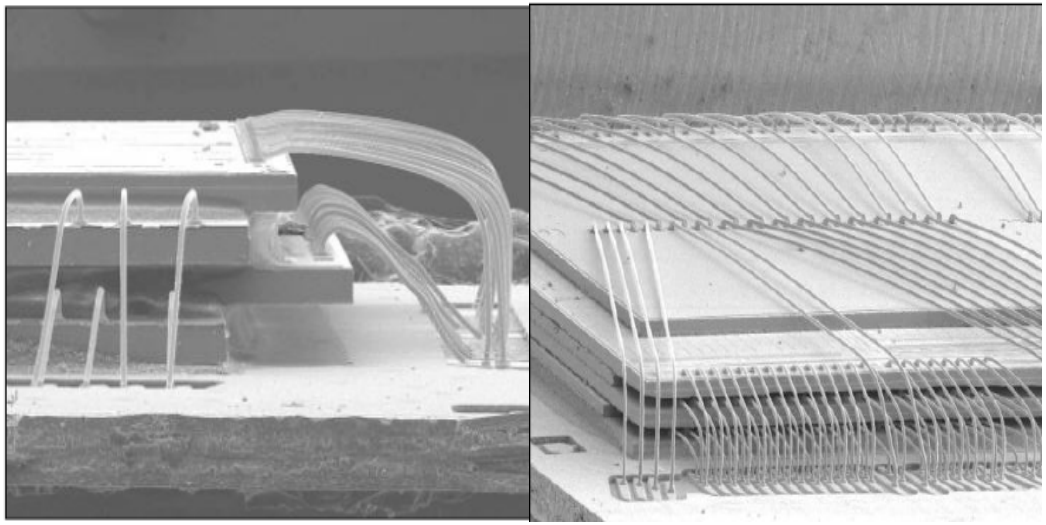
D.C. Kau, IEDM (2009)

- **CMOS-compatible NVMs can be fabricated using BEOL process.**
- **Possibility to extend into 3-D for high density (small F^2) integrations**

System-in-Package (SiP) Integration

- SiP: a number of integrated circuits enclosed in a single module (package).
- Chips are stacked vertically and interconnected by fine wires that are bonded to the package.
- Mainly used for off-chip memories (flash, DRAM)…
- Limitations: parasite inductance (~ few nH); thermal budget (soldering)





3D Integration: Not a New Topic

Akasaka, Y., and Nishimura, T., "Concept and Basic Technologies for 3-D IC Structure"
IEEE Proceedings of International Electron Devices Meetings, Vo. 32, **1986**, pp. 488-491.

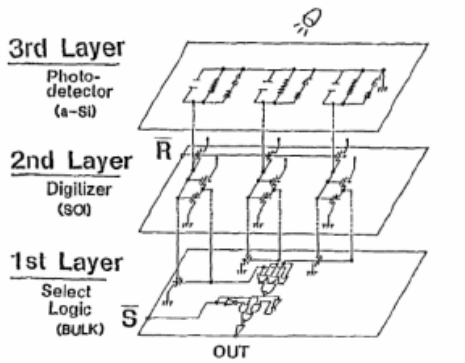


Fig.8 a-Si photo sensor and processing circuits in 3-staked layers (after Mihashi)

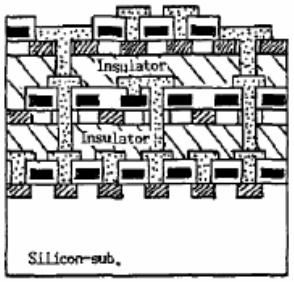


Fig.1 Schematic drawing of 3-D IC consisting of monolithic multi-layer structure.

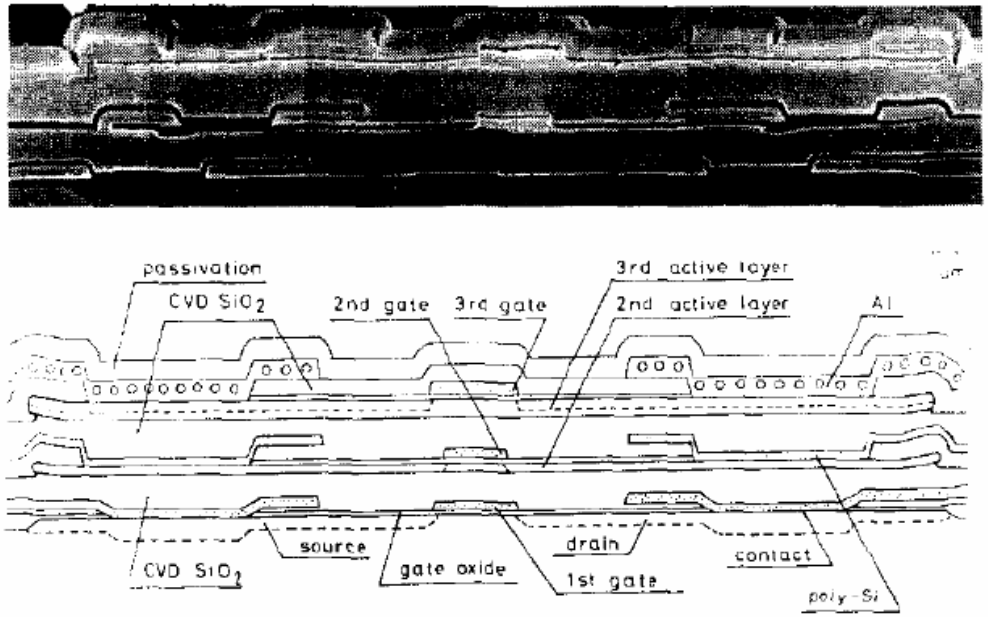
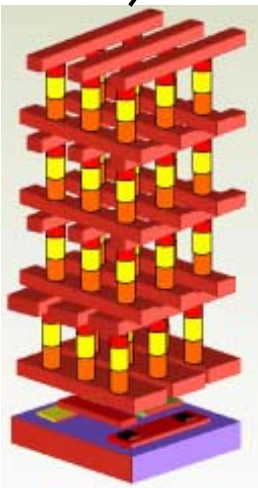


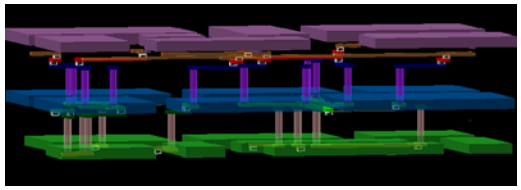
Fig.4 SEM cross sectional photograph and schematic drawing of planarized tripply-stacked IC structure.

Horizons for 3D Integration Technology

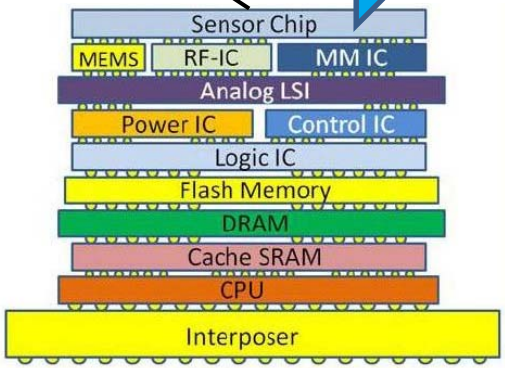
FEOL/BEOL → **Die on Die** → **Die on Wafer**



Monolithic



Through Silicon Vias



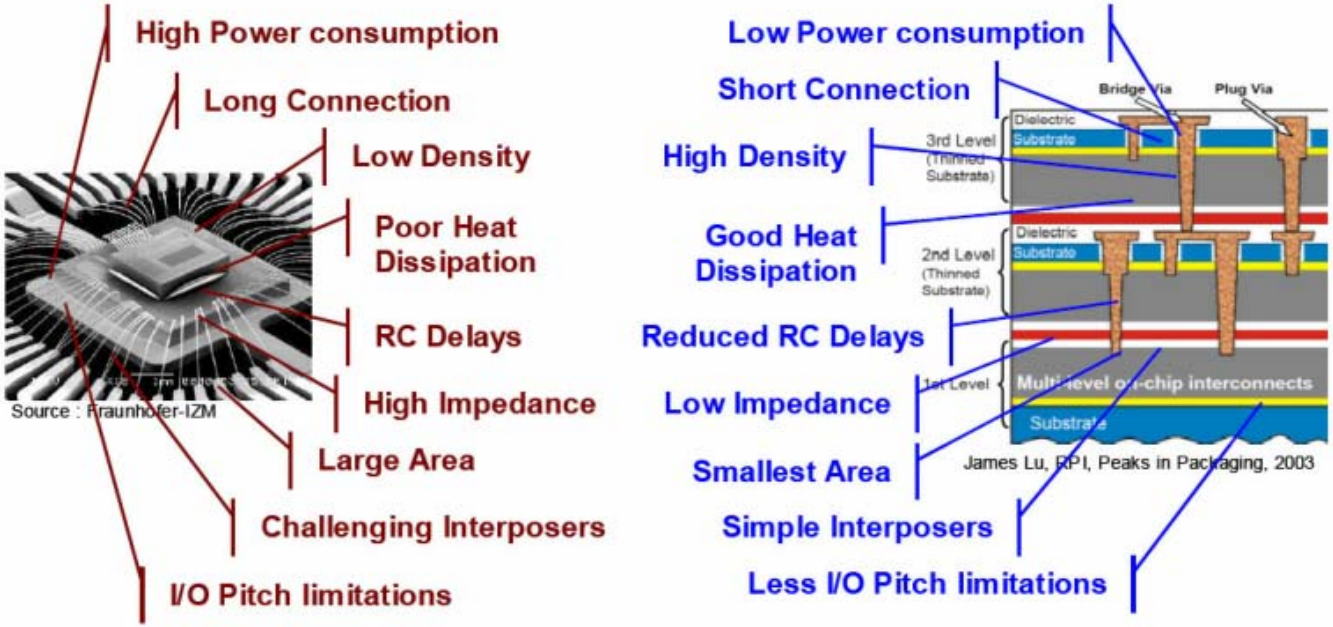
Si Interposer

Density Factors	PCB	Si Interposer	3D IC
Signal Pitch, P	1000 (~1mm)	10 (~10um)	10 (~10um)
Signal Length, L	1cm	1mm	1 (~50um)
Density Index (1/P*L, Normalized)	1	~1k	~20k
Product	Consumer	Server, FPGA	Mobile
Product attributes	Low cost	High-end, performance driven, power hungry	Small form factor, low power

3D Benefits: Not Only the Low Cost!

Why TSV Interconnection?

TSV (Through-Silicon-Via) electrodes can provide vertical connections that are both the shortest and the most plentiful.



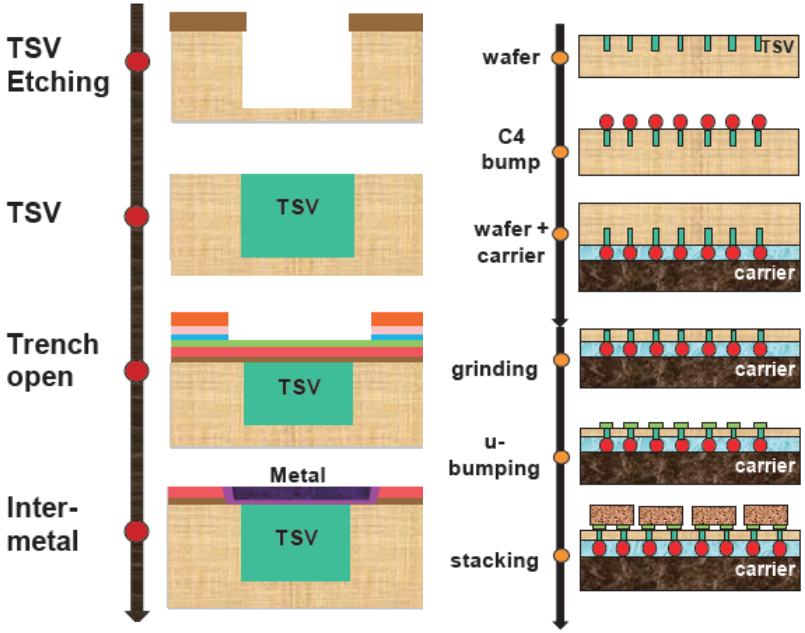
TSV interconnects provide solutions to many limitations of current SiP and Chip Stacking methods.

Ecole Polytechnique Paris - 3D Technical Symposium; November 2007

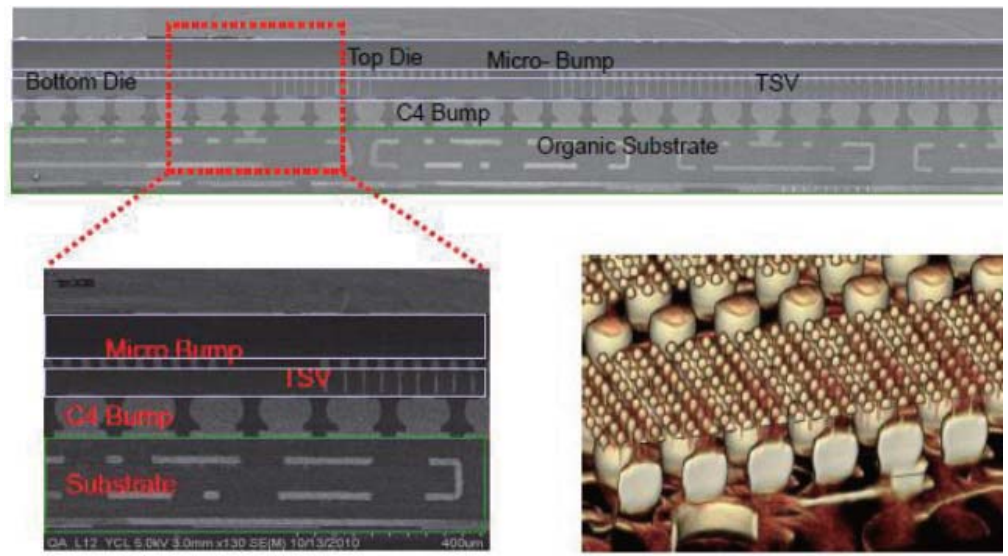
Page3

CMP annual users meeting, 25 January 2012, PARIS

Through Silicon Vias (TSV)



T. Lo, IEDM (2012)



- **TSV has ~30x diameter ratio over on-chip MLs, hence has limited applications.**

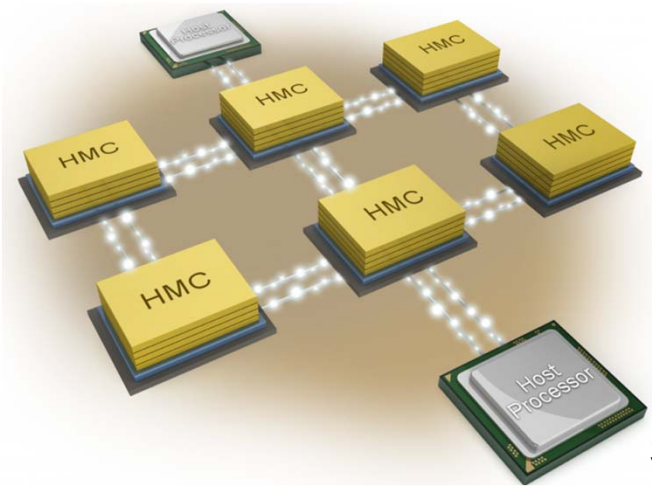
Industry Roadmap for TSV

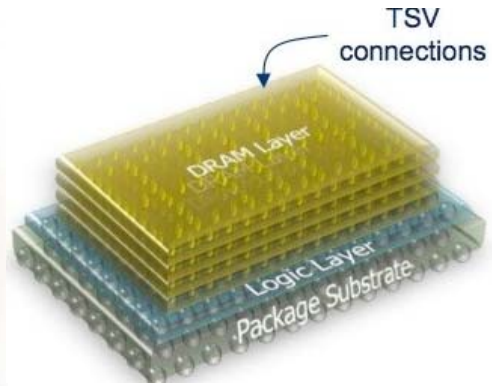
Intermediate Level, W2W 3D-stacking	*2009-2012*	*2013-2015*
Minimum TSV diameter	1-2 µm	0.8-1.5µm
Minimum TSV pitch	2-4 µm	1.6-3.0 µm
Minimum TSVdepth	6-10 µm	6-10 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1

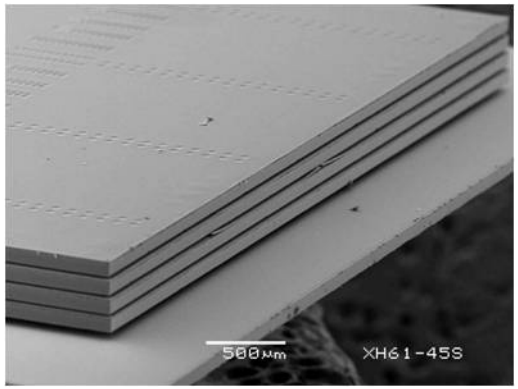
TSV Applications: 3-D DRAM

- **Allows heterogeneity in IC manufacturing:**
  - **Logic circuits no longer suffer from the inefficiencies of the DRAM process.**
- **Provides proximity to the memory for a small amount of logic circuitry;**
  - **Enables the light "Processing-In-Memory" style computation.**

<u>Hyper Memory Cube (HMC)</u>







Source: Intel & Micron (2011)

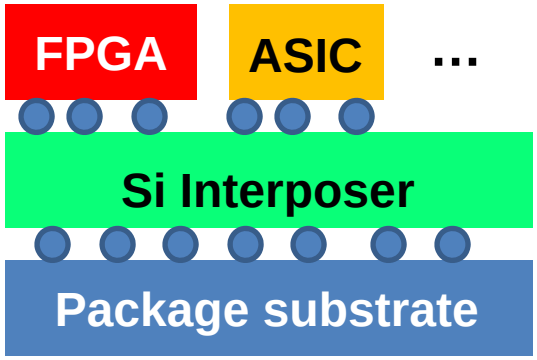
- **Data Transferring Rate: 15 times than DDR3**
- **Energy per Bit: 30% reduction from DDR3**
- **Chip Area: 90% reduction**

Chip-on-Wafer-on-Substrate (CoWos)

- **Motivation**: Full die stacking through TSV may not be mature in the near term, hence a Si interposer with TSV provides the option, which is the CoWos technology. FPGA requires advanced, high speed technologies, which can takes advantages of CoWos.
- **Technology Features**:

  The test chip comprises a 40nm high performance FPGA die (w/ 11 metal layers) and some other test dies, which are connected to the package substrate through the Si interposer. There are micro-bumps, TSVs, 3 metal layers, inductors and MIMs inside the Si interposer.

Illustration of CoWos

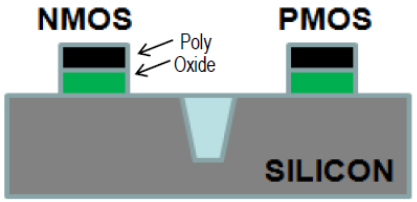


Top and Cross-sectional View of the Test Chip

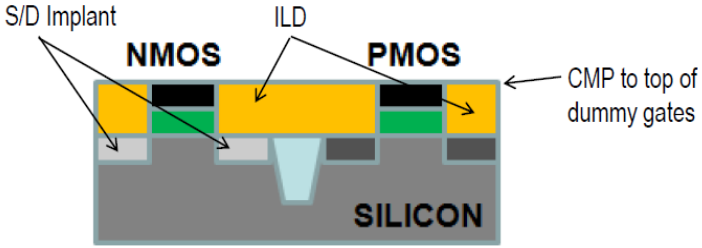
D. Ibbotson, VLSI (2013)

Monolithic Approaches: Wafer Bonding

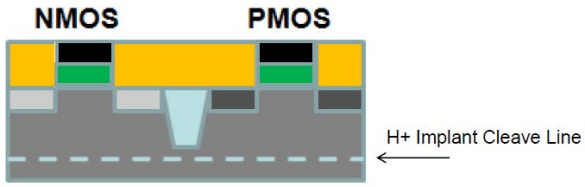
Step 1 (**std**): On donor wafer, fabricate standard dummy gates with oxide, poly-Si



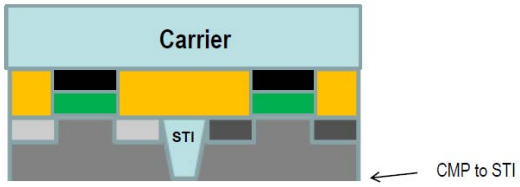
Step 2 (**std**): Std Gate-Last
- Self-aligned S/D implants
- Self-aligned SiGe S/D
- High-temp anneal
- Salicide/contact etch stop or faceted S/D
- Deposit and polish ILD



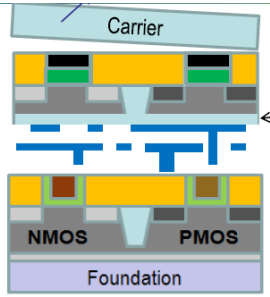
Step 3.
Implant H for cleaving



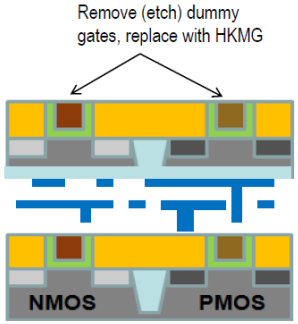
Step 4.
- Bond to temporary carrier wafer (adhesive or oxide-to-oxide)
- Cleave along cut line
- CMP to STI



Step 5.
- Low-temp oxide deposition
- Bond to bottom layer
- Remove carrier



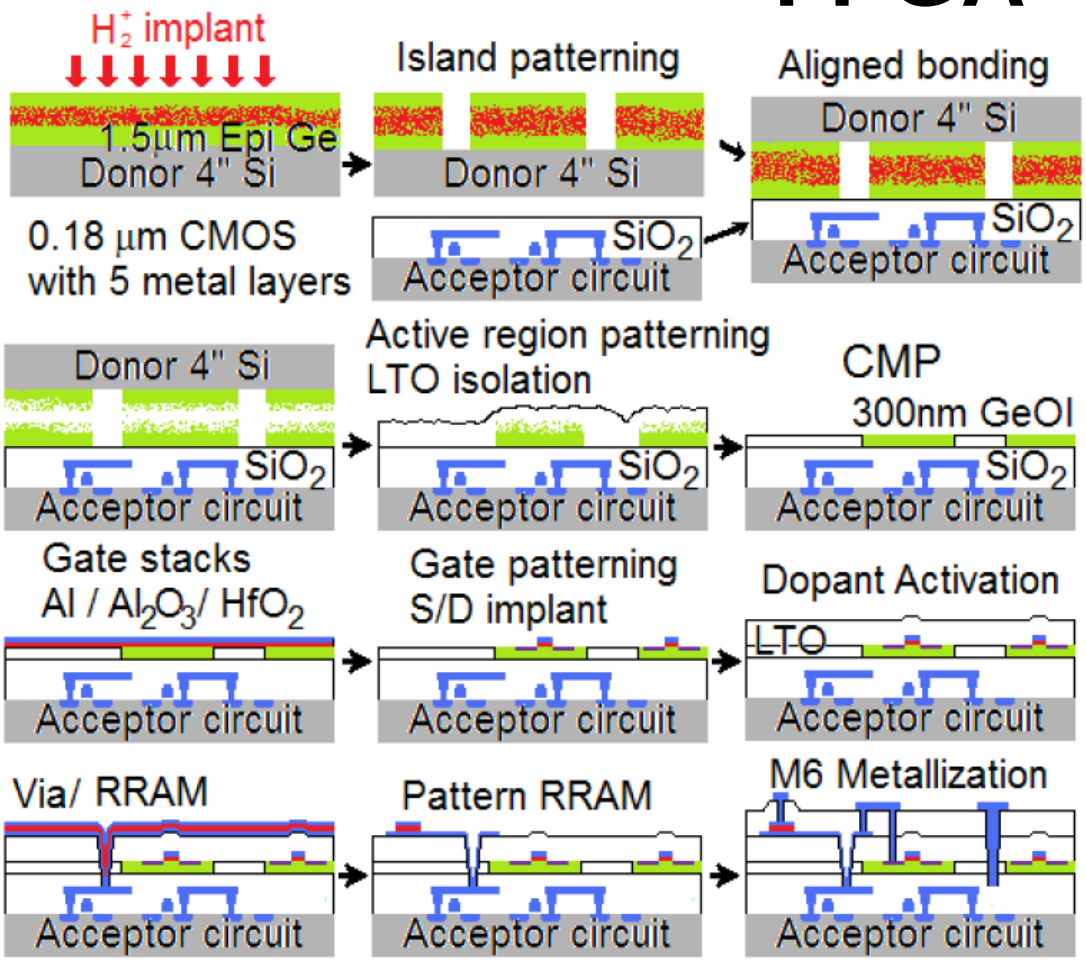
Step 6 (**std**): On transferred layer:
- Etch dummy gates
- Deposit gate dielectric and electrode
- CMP
- Etch tier-to-tier vias thru STI
- Fabricate BEOL interconnect

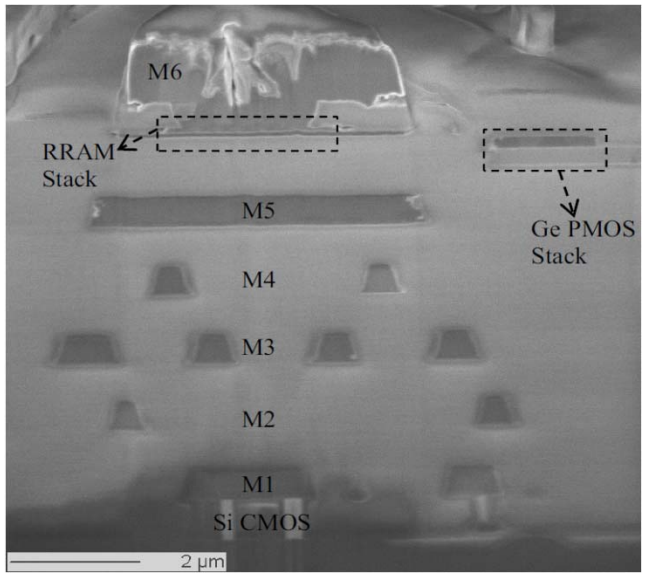


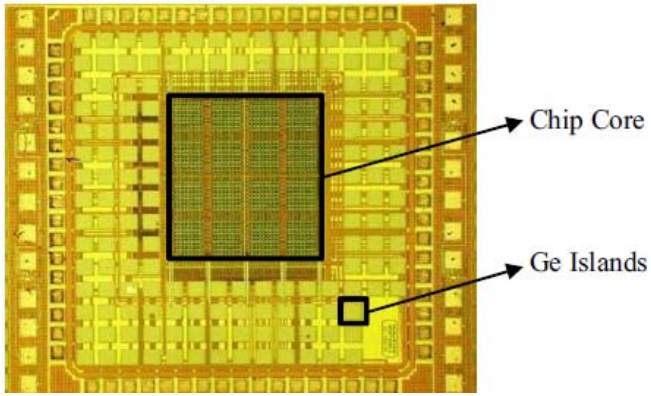
- **A crystalline Si layer transfer technology similar to "Smart Cut" used in previous SOI substrates.**
- **Thermal budget < 400 ^{o}C**

Courtesy of D. Sekar (Monolithic 3D)

Wafer Bonding Example: FPGA







Z. Zhang, EDL (2013)

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